SELF-POWERED BALUN LOW NOISE AMPLIFIER WITH DEGENERATION BALANCING AND THERMAL NOISE ANALYSIS

by

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Declaration of Authorship

I declare that this thesis is my own work and, to the best of my knowledge and belief, it does not contain material published or written by a third party, except where permission has been obtained and/or appropriately cited through full and accurate referencing.

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Date…May 10th, 2020.…

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Abstract

The Balun low noise amplifier (LNA) is an LNA that exploits a combination of a common-source (CS) and a common-gate (CG) transistor, which cancels the noise and distortion of the CG stage. And since the CG is known to be linear, only the CS needs to be carefully designed and optimized. In this thesis, the CS section will be fully analyzed, and shown how the condition set in the literature review still satisfies the balancing output and cancels the CS stage thermal noise as well as the CG thermal noise. Also, forward body biasing (FBB) is used to reduce the threshold voltage and in addition, CS degeneration resistor will be studied to balance the output and cancel the thermal noise of the transistors. The circuit is tested using UMC180nm on Cadence. The LNA achieves a gain of 19-16dB, NF<3.6 dB over the bandwidth 0.2-1.9GHz without a CS degeneration. A 17.8-14.8dB gain, a NF<3.8 dB over the bandwidth 0.2-2.1GHz and power consumption of 12mW in both cases. Although outside the bandwidth, at ISM 2.4GHz a gain of 14.5dB and a NF of 3.8 is achieved, making it suitable for wireless sensor node (WSN) applications. According to the authors' knowledge, this is the first time the degeneration resistor noise analysis on a Balun LNA is derived and simulated. Also, an RF harvester will be studied and used to power the Balun LNA. A two stage Dickson charge pump using MOSFET connected diode is chosen for this application. Although the efficiency is around 40%, the harvester was successfully integrated to the LNA, and its noise figure added to the output of the LNA.

Keywords: ***Low noise amplifiers; Balun; Noise analysis; Differential amplifiers; Degeneration; Harvester***

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List of Abbreviations

AC	Alternating current
CG	Common Gate
CMOS	Complementary-Channel Metal-Oxide-Semiconductor
CPR	Charge Pump Rectifier
CS	Common Source
dB	Decibels
DC	Direct current
DRC	Direct conversion
DSP	Digital Signal Processing
FBB	Forward Body Biasing
G	Gain
IF	Intermediate frequency
IIP3	Input referred IP3
IMD	Intermodulation distortion
IP3	Third order intercept point
LNA	Low-Noise Amplifier
LO	Local oscillator
LPF	Low pass filter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise figure
NMOS	N-channel Metal-Oxide-Semiconductor
OIP3	Output referred IP3

P1dB	1-dB compression point
PDK	Process Design Kit
PMOS	P-channel Metal-Oxide-Semiconductor
RF	Radio frequency
ULP	Ultra-Low Power
ULV	Ultra-Low Voltage
UMC	United Microelectronics Cooperation
WSN	Wireless sensor nodes
ZIF	Zero Intermediate frequency

Chapter 1. Introduction

1.1 Overview

The digital revolution in the wireless market has brought many changes in analog transceivers today. The wireless transceiver detects weak and high frequency signal, this requires high performance from RF and baseband analog circuits. The high performance required of the RF circuit working at high frequencies brings challenges to the circuit design. With the consideration of the price and power consumption, many researchers use Complementary MetalOxide Semiconductor (CMOS) technologies for Radio Frequency (RF) applications. CMOS Integrated Circuits (ICs) are low cost, low power consumption and better integration with DSP (Digital Signal Processing) chips. CMOS also allow a large amount of digital functions on a single die.

Energy Harvesting is defined as the practice of capture, accumulation and storage of unexploited energy from circumambient environmental sources. The field of energy harvesting is in rapid development and is the new hit in RF designs, as some devices are in positioned that are not easy to reach for battery replacements. RF wireless electronics perform a crucial role in gathering and analyzing information nowadays. To sustain the wireless data, many wireless infrastructures have been made and used, such as TV networks, GSM networks, etc. which can in theory be captured and stored. However, some circuits are being developed with certain efficiency which help them capture power from a source to charge them. This is a more realistic approach to energy harvesting, as a harvester can be optimized at certain power levels and frequency [1].

To have a Wireless sensor network (WSN), several different sensor nodes are energetically autonomous and wirelessly connected. They share information by communicating wirelessly. The transceiver connects the individual nodes together, thus a wireless sensoring network is made. WSN area and installation depend on their characteristics and range. Additionally, these nodes must be autonomous and individually power, the problem when installing batteries to make any sensor node autonomous is that these nodes are in harsh environments making battery replacement difficult, therefore energy harvesting devices are attractive to WSN applications to charge the battery or power the node directly. The idea of having a self-powered node also opens many possibilities for their geographical location.

After the transmitter modulates the signal, it is then transmitted. The process of modulation has the signal go from baseband frequencies to any higher desired frequency, usually the carrier frequency, this reduces the size of the antenna (antenna's length is typically wavelength/4). Also, as the signal propagates, it suffers from attenuations, thus, must be amplified by the receiver [2]. The frontend amplifier of the receiver known as the low noise amplifier (LNA) possess low noise properties, as the noise will propagate and get amplified going forward into the receiver, the LNA also has moderate gain to compensate for the propagation attenuation.

1.2 Organization

The thesis is broken down to several chapters as follows: Chapter 2 is background discussing types of receivers, compression point, Intercept points, scattering parameters and process, voltage and temperature (PVT) analysis. Chapter 3 is noise analysis, LNA topologies and noise derivation of the current design. Chapter 4 is harvester topologies, design method and harvester testing and simulation for the current design. Chapter 5 is the LNA and harvester integration with all simulation results. Chapter 6 is the conclusion and future.

1.3 Objective

The main objective of this thesis is to show how the Balun LNA thermal noise of the transistors can be completely canceled and not just the CG side. A degeneration resistor on the CS side of the Balun LNA is studied and shown how the degeneration balancing can cancel the thermal noise of the transistors completely.

A harvester is to be picked for the LNA to power it, while still maintaining the highest AC to DC conversion efficiency. Three transistors will be tested in terms of width, length, number of fingers and load to pick the most efficient one. The LNA will be directly connected to the harvester as a load, making the harvester directly power the circuit without any charge storing unit.

1.4 Contribution

Not only does the thesis show how the thermal noise of the CS side of the Balun LNA is canceled, it also adds to it by showing how a degeneration resistor can help cancel the transistor thermal noise of the LNA, adding one more degree of freedom to the design. Also, a Dickson charge pump is used to directly power the LNA without any storage unit with its noise successfully added to the system.

Chapter 2. Background

In this chapter three receiver architectures are discussed with the advantages and disadvantage of each. Additionally, some measuring parameters, such as P1dB, IMD3, S-parameters etc. are explained.

2.1 Receiver Architectures: Super-Heterodyne, Homodyne and Low-IF Receivers.

A receiver main purpose is to detect an RF signal at the antenna, down convert it into an intermediate frequency (IF), maintain the signal quality and deliver it to the baseband. Super-heterodyne, homodyne and low-IF receivers advantages, and disadvantages are shown.

2.1.1 Super-heterodyne receiver: The RF signal is captured by the antenna and filtered through a bandpass filter which removes unwanted frequencies. The signal is too weak at this stage, therefore an LNA is used to amplify the signal and add as little noise as possible. The second filter is there for image rejection, all it does is attenuate the signal at image band frequencies. The first mixer is to down convert the signal to the IF band, the reason the signal is converted to IF or baseband is to lower the bandwidth and therefore becomes much easier and faster to process. A high selectivity filter that removes any adjacent IF signals from the desired IF which helps avoid image frequency issues. Finally, the signal is sent to the analog to digital converter (ADC) [3].

The image frequency problem occurs when the input of the mixer has a signal image, which after multiplication generates two other signals with one laying inside the IF, resulting in overlapping between the desired signal and an unwanted signal, the image and the signal are impossible to separate at this point. Therefore, before entering the mixer, an image rejection filter is applied to remove the image signal [2] [4], this is the only way to avoid image frequency issue.

Figure (2.1) [5], is a schematic of the superhetrodyne receiver, showing all the components. Table 1 [3] lists the most important advantages and disadvantages of the superhetrodyne receiver.

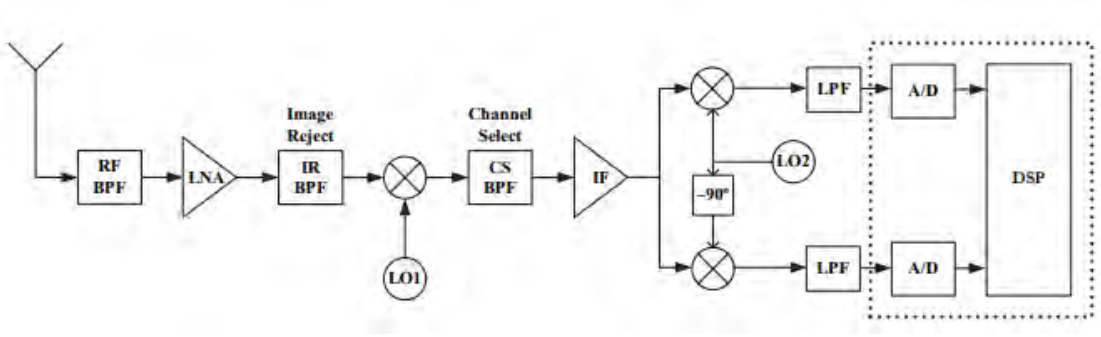


Figure 2.1: Super-heterodyne Receiver.

Table 1. Advantages and Disadvantages of the super-heterodyne receiver.

Advantage	**Disadvantages**
Well established	Image frequency
Superior performance	Difficult to integrate
Adjustable with discrete	Costly (money and power)
Good spurious suppression with filter	Requires quadrature generating complex mixer

2.1.2 Homodyne receiver. The homodyne receiver is also known as the direct conversion receiver or the zero-IF receiver (ZIF), converting the RF to baseband directly, with less components than the super-heterodyne. This is done with an LO with the same frequency of the RF. The main advantages over the super-heterodyne is that the homodyne receiver does not generate image frequency, therefore no extra techniques to deal with the image are needed. Also, it is simpler in design and implantation, hence the reason why integrating it on chip is easier than the super-heterodyne receiver.

Figure (2.2) [5], is a schematic of the homodyne receiver, showing all the components. Table 2 [3] lists the most important advantages and disadvantages of the homodyne receiver.

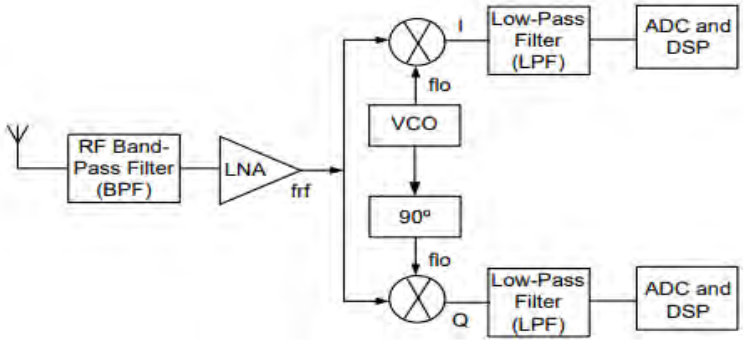


Figure 2.2: Homodyne Receiver.

Table 2. Advantages and Disadvantages of the Homodyne receiver.

Advantages	Disadvantages
No image, therefore, no need for a SAW filter	DC offset and flicker noise
Highly integrable	Significant LO leakage could create inband interference
Only one PLL is needed	Strong AM interference will create inband interference after the mixer, therefore a linear mixer is required
Low power	LO leakage to the antenna can be transmitted and reflected to self-mix with the oscillator creating a time varying wandering DC offset
Good multi-standard ability	Leakages from the transmitter may need a good filter
Increased ADC dynamic range. No IF, therefore limited filtering	I/Q match required to avoid imbalances which causes constellation distortion
Industry standard for mobile headsets	VCO requires multiple frequency of RF

2.1.3 Low-IF receiver: If one tries to combine the advantages of the previous two architectures, the Low-IF receiver is formed. The DC problem of the homodyne receiver can be avoided by relaxing the quality factor of the channel selective filter, particularly flicker noise is dealt with. The image problem from the super-heterodyne can be canceled using special mixing circuits or the polyphase quadrature filters. Image cancelation techniques are implemented to avoid using image rejection filters. Two architectures are used, Weaver and Hartley, these methods suppress the image by its negative replica. The idea is to process the RF signal after LPF and combine both outputs into one. Figure (2.3) [6] is two different Low-IF receiver architectures and Table 3 [3] list the main advantage and disadvantages of this architecture.

$$x_{RF}(t) = V_{RF}\cos(w_{RF}t) + V_{IM}\cos(w_{IM}t) \tag{2.1}$$

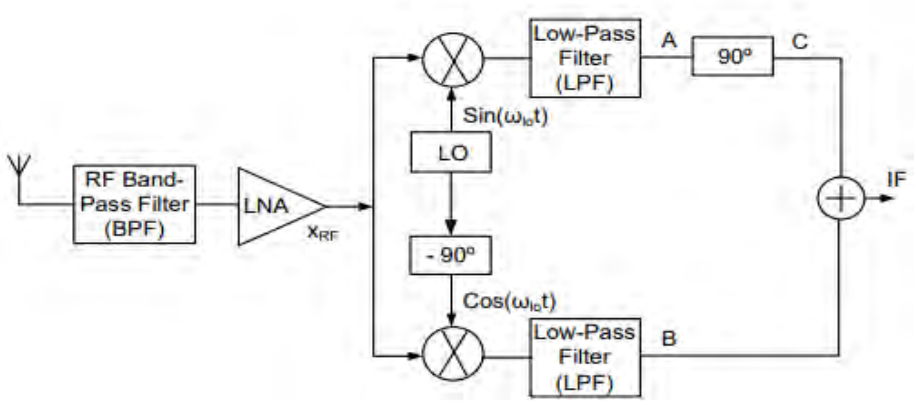
$$y_A(t) = \frac{V_{RF}}{2}\sin[(w_{LO} - w_{RF})t] + \frac{V_{IM}}{2}\sin[(w_{LO} - w_{IM})t] \tag{2.2}$$

$$y_B(t) = \frac{V_{RF}}{2}\sin[(w_{LO} - w_{RF})t] + \frac{V_{IM}}{2}\sin[(w_{LO} - w_{IM})t] \tag{2.3}$$

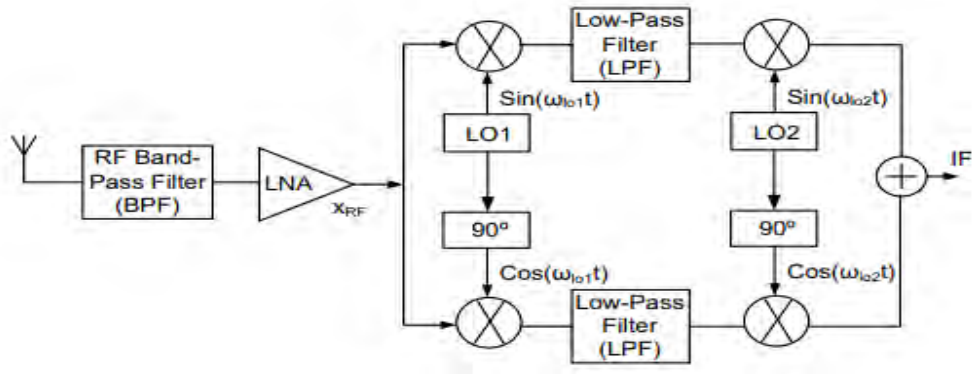
$$\sin\left(\theta - \frac{\pi}{2}\right) = -\cos(\theta)\,, with\ a\ 90^0\ shift$$

$$y_c(t) = \frac{V_{RF}}{2}\sin[(w_{RF} - w_{LO})t] - \frac{V_{IM}}{2}\sin[(w_{LO} - w_{IM})t] \tag{2.4}$$

One where x_{RF} is the RF signal, V_{RF} is the voltage level of the RF signal, w_{RF} is the carrier angular frequency, t is time, V_{IM} is the voltage level of the Intermediate frequency, w_{IM} is the Intermediate angular frequency, w_{LO} is the local oscillator angular frequency, and y is the output.



(a) Hartley



(b) Weaver

Figure 2.3: Low-IF Hartley and Weaver architectures.

When adding (2.3) and (2.4) the wanted signal is recovered and image is removed.

Weaver architecture has similar result but with a second mixer stage at IF. Both architectures can remove the image, depending on their quadrature signal precision. A draw back for these two designs is that having a quadrature error will result in gain/phase imbalances, making it difficult for the next stages to process the signal smoothly.

Table 3. Advantages and Disadvantages of the Low-IF receiver.

Advantages	**Disadvantages**
Eliminates the need for external SAW same as homodyne	Additional digital signal processing to cope with Non-ZIF, requires ADC twice the BW compared to ZIF or superhetrodyne
No DC offset problem	Uses an additional phased locked loop to get to I&Q
Suitable for CMOS as phased locked loop operates around 2GHz	Only marginal rejection with polyphase filters
Less RF filtering than homodyne receiver, but in-band image rejection	Complex filter implementation compared to homodyne receiver

2.2 Harmonics and Intermodulation Distortions

In a non-linear system its polynomials can be estimated as [3]:

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \cdots, \tag{2.5}$$

where x is the input signal and y represent the output signal. Systems are usually not extremely nonlinear therefore higher order disappear.

If $x = \sin(2\pi f t)$ is applied to a non-linear system input. The output result is approximately:

$$y = a_0 + a_1 A \sin(2\pi f t) + a_2 \frac{a_2 A^2}{2} \sin(4\pi f t) + \left(\frac{a_3 A^3}{4}\right) \sin(6\pi f t) \tag{2.6}$$

The expression in (2.6) has harmonic distortions at multiple fundamental frequencies. Harmonics can lead to reduction in filtering or can interfere with other channels. The second problem is intermodulation distortion (IMD). IMD is the amplitude modulation of multiple different frequencies caused by non-linearity of a system. If the 2nd unwanted signal is not filtered out, the receiver will produce 2nd order IMD and 3rd order IMD which are $f_2 \pm f_1$ and $2f_2 \pm f_3$ respectively. Adding the coefficient of each f_n will give the order of the IMD. The most dangerous modulation is the 3rd order, as it is near the operating frequency.

Harmonics and IMD are unavoidable phenomenon's and cannot be completely removed from a system. Harmonics might be harmful to a wideband system, but most importantly to other channels that the harmonics will be projected onto, therefore they cannot be ignored. IMD's, specifically IMD3, fall very close to the desired frequency of operation and can cause unwanted interfere if not properly dealt with, a very sharp filter can help reduce the IMD3 for an extra cost to the system. Figure (2.4) shows what harmonics and IMD are in graph format for a two-tone input (f_1 and f_2). Harmonics are integer multiple of the main frequency (or frequencies) they are infinite, but since the harmonic's magnitude is very low after the third harmonic they can be ignored. Although the second order harmonics have the highest magnitude, they are far away from the operation frequency and can be ignored. The same idea for ignoring the higher order of harmonics apply for IMD, where the IMD of higher order than three are either far away or too small and can be ignored.

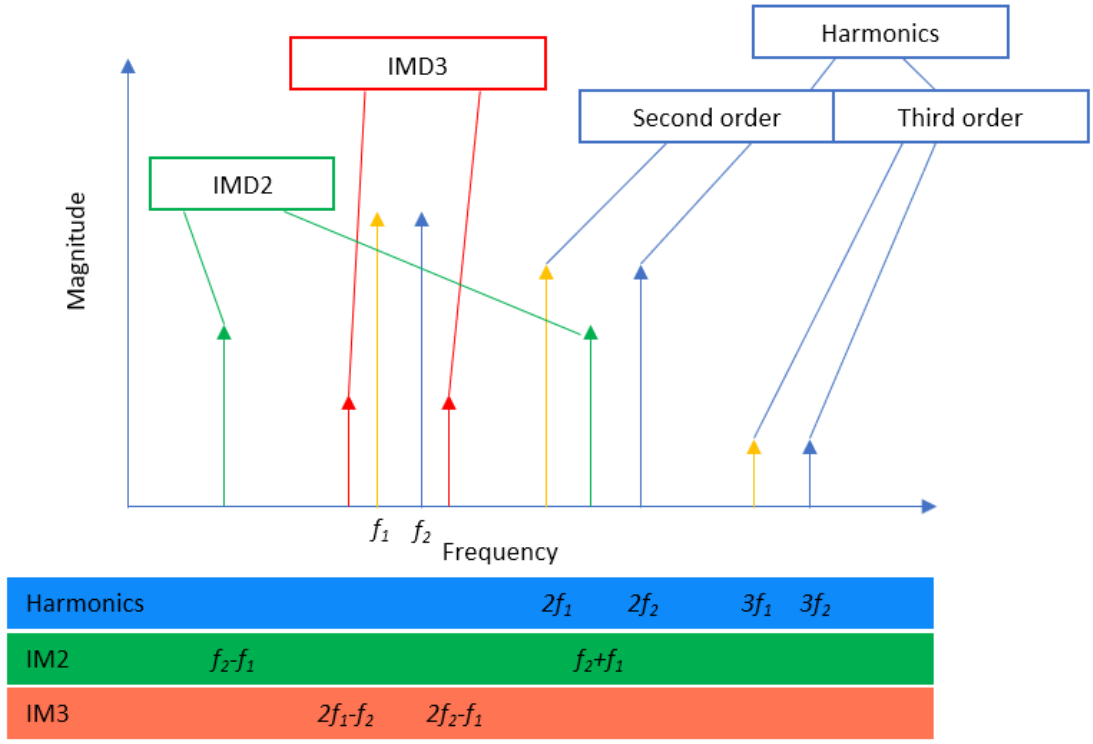


Figure 2.4 Two-tone harmonics and IMD.

2.3 1-dB Compression Point (P1dB)

Even if one can eliminate IMDs and harmonics, a non-linear term known as P1dB will appear. P1dB is considered as a loss of power. In linear operation of an amplifier, increasing the input by 1 dB or 10 dB should not result in any change in the gain, however at the P1dB the amplifier no longer acts linearly, rather starts to get saturated and the amplifier experiences a loss of 1 dB in gain. Similarly, PXdB is when the amplifier loses X-dB of the output gain. At this point the amplifier has left the linear operation region.

2.4 3rd Order Intercept Point (IP3)

Another important figure to test is the third order intermodulation intercept point (IP_3), which is a measure of the linearity of the system. IIP_3 is the input referred IP_3 and OIP_3 is the output referred IP_3. The IP_3 is the intersection of the idealized output power of the first and third order, at this point the first and third order are of equal power. IP_3 typically occurs after the P1dB, estimated to be P1dB+10dB. A two-tone input signal

is commonly used for the IP_3 test. (2.7) is a system overall IIP_3, it is a measure of every elements IIP_3.

$$\frac{1}{IIP_3} = \frac{1}{IIP_{3,1}} + \frac{G_1}{IIP_{3,2}} + \frac{G_1 G_2}{IIP_{3,3}} \tag{2.7}$$

Where $IIP_{3,1}$ is the input referred IP_3 of the first stage, $IIP_{3,2}$ is the input referred IP_3 of the second stage, $IIP_{3,3}$ is the input referred IP_3 of the third stage, G_1 is the gain of the first stage and G_2 is the gain of the second stage.

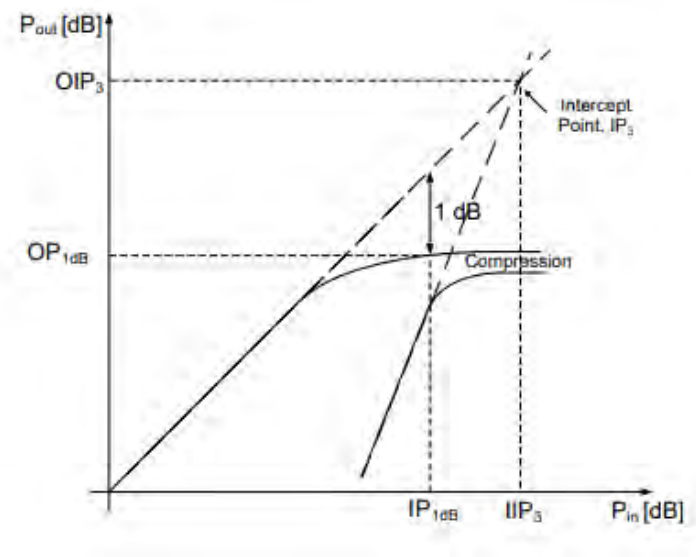


Figure 2.5 Graphical representation of the third-order intercept point and P1dB [6]

From (2.7), it is seen that the gain of the preceding stages effects directly the IIP3 of the next stages, but a low noise figure demands high gain. Here there is a tradeoff between noise and linearity [2] [7].

2.5 Scattering Parameters (S-parameters)

System characterization is done differently for low frequency and high frequency. At the low frequencies, the system is characterized by measurement of open and short circuit tests, which determine the admittance and hybrid parameters. At high frequencies, the signal is dealt with as a wave, therefore low frequency methods are not possible. S-parameters are used at the high frequencies to characterize the input and output variables to measure input impedance, gain, reflections and output impedance. The S-parameters relate the input and output of electromagnetic waves as a_1, a_2, b_1 *and* b_2 when the system is viewed as a two-port network. Knowing the S-

parameters is enough to aid in designing a system without knowledge of the components it consists of.

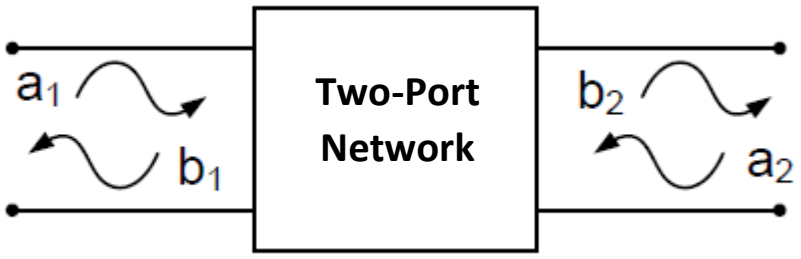


Figure 2.6 Two-Port network incident and reflected waves.

Figure 2.7 S11, S12, S21, and S22

The S-parameters are calculated as:

$$S_{11} = \frac{b_1}{a_1} \tag{2.8}$$

$$S_{12} = \frac{b_1}{a_2} \tag{2.9}$$

$$S_{21} = \frac{b_2}{a_1} \tag{2.10}$$

$$S_{22} = \frac{b_2}{a_2} \tag{2.11}$$

Where S_{11} is the input reflection coefficient, S_{12} is the reverse gain if the input and output where swapped, S_{22} is the output reflection coefficient, and S_{21} is the gain.

2.6 Process, Voltage and Temperature Variations (PVT).

PVT; sometimes called corner analysis; is done to check the fabrication quality of a circuit. Process refers to the circuit elements fabrication, each different component undergoes a different process and therefore will have different dimension than that on the schematic. Even identical transistor cannot be expected to be the same size after fabrication due to errors. Voltage variation test the circuit ability to handle a supply voltage swing, an example of such variation is a battery whose supply voltage drops with use. Temperature variation are done to test the circuit under different temperatures, these temperature changes can be due to heating of the circuit component due to operation or environmental temperature changes. In this thesis the industry standard temperature is taken into consideration (-40°C ➔85°C).

Process variation mean that elements in the circuit have a maximum, minimum, and typical values depending on the length and width when fabricated. Resistor corner analysis apply for capacitors and inductors. MOSFET corner analysis apply for BJT and diodes.

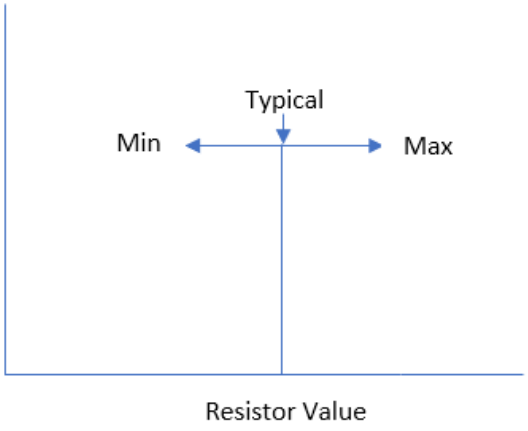


Figure 2.8 Resistor corner analysis

The resistor will take any value between Min and Max. Min, Max and Typical values are given by the foundry. If the resistor takes the min value, then its value is less than the typical, the current through the resistor increases, therefore power consumption increases (min is sometimes called “wp” meaning worst power)

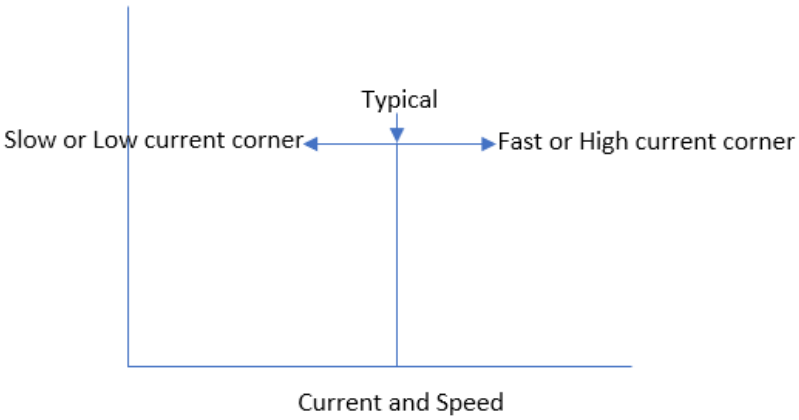


Figure 2.9 Fast, typical and slow corners

For a MOSFET process, the oxide thickness, doping concentration, length and width can vary, resulting in a change of Vth. For a MOSFET the corner analysis is: TnTp, SnSn, SnSp, SpSn, SpSp, FnFn, FnFp, FpFn and FpFp. T stand for typical, S stand for slow, F stand for fast, n and p stand for NMOS and PMOS respectively.

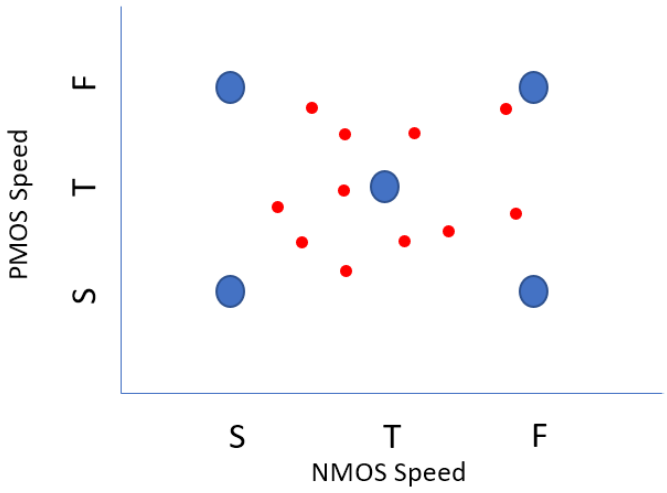


Figure 2.10 Corner analysis possible combinations

At the start of the design, a voltage source will be used to bias the circuit. This helps simplify the design procedure. After a biasing point has been picked, the voltage source will be replaced with transistor current mirrors and corner analysis done with the current mirrors as biasing.

2.7 Forward Body Biasing (FBB).

By connecting the body of the MOSFET to the gate or a DC voltage source FBB is achieved. In the case of CG, the body is directly connected to the gate, as no AC signal is present on the gate. However, for the CS, the body cannot be connected to the gate as an AC signal is present, the body is connected to its own biasing voltage or before the biasing resistor.

In [8] an 130nm ultra-low power (ULP) and ultra-low volt (ULV) was achieved using FBB and a huge circuit of 0.39mm^2 , it used a CG in a current-reuse structure, implied an inductor gm boosting techniques, low-power input matching was achieved by an active shunt-feedback while the current of the feedback was reused by the input of the transistor, a BW of 0.6-4.2Ghz using 0.5V and 500uA, achieving 4 NF and 14db gain. The auxiliary amplifier power was not included in the power measurement. The design of this thesis will adopt the FBB technique. In [9] an UWB 3-10Ghz CG was design with 1.1V and 2.15mW using body biasing a gain of 10.4dB, NF of 4.9 on 180nm, his paper is a letter discussing matching of CG and his chip fabrication, this letter is related to [10]. In [11] using FBB and 3 coupling inductors to achieve ULP and ULV LNA but a narrow band 400-900Mhz, voltage gain of 18.5-20.7, NF of 2.95, 0.385mW and 0.5V in 180nm.

From low power application, where power is a main concern, [8], [10], [9], [11] all have used FBB to improve the power consumption. Since the LNA will be connected to an RF harvester, any reduction in power consumption is a bonus to the design.

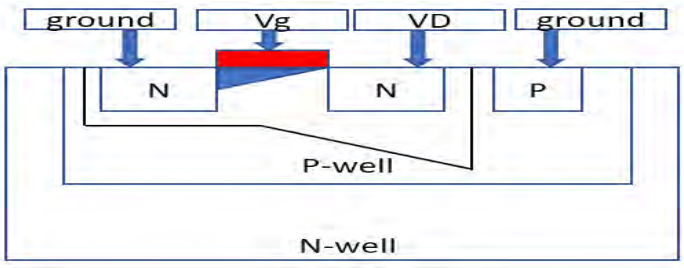


Figure 2.11 Cross section view of NMOS without FBB.

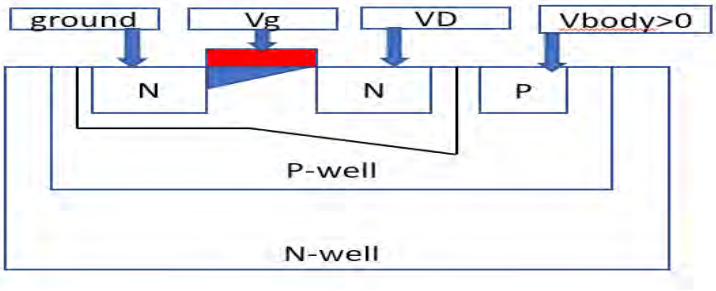
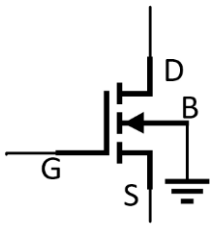
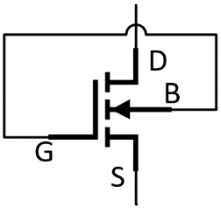


Figure 2.12 Cross section view of NMOS with FBB.

"DC print" option opens a window that display the transistors operating parameters at the given biasing conditions. This was used to display Vth and compare Vth with FBB vs Vth without FBB.

Table 4. FBB Vth value

	No FBB	FBB
Diagram		
Vth	442m	391m

**Vth values extracted from cadence "DC Print"*

From Table 4 both a transistor with FBB and without FBB are shown, the only problem with FBB occurs when the body is connected to the gate and an AC input is at the gate (such as common-source configuration) making an AC signal to the body which is undesired. One way to solve this issue is to have a separate biasing to the body, another way to connect an RF choke to the body to prevent an AC signal from passing through. An RF choke can be a resistor or an inductor. Having a separate biasing to the body is not desired as it adds another pin to the chip. The Common-gate configuration does not suffer from this issue as the gate does not have an AC input applied to it, the AC input is applied to the transistor source terminal.

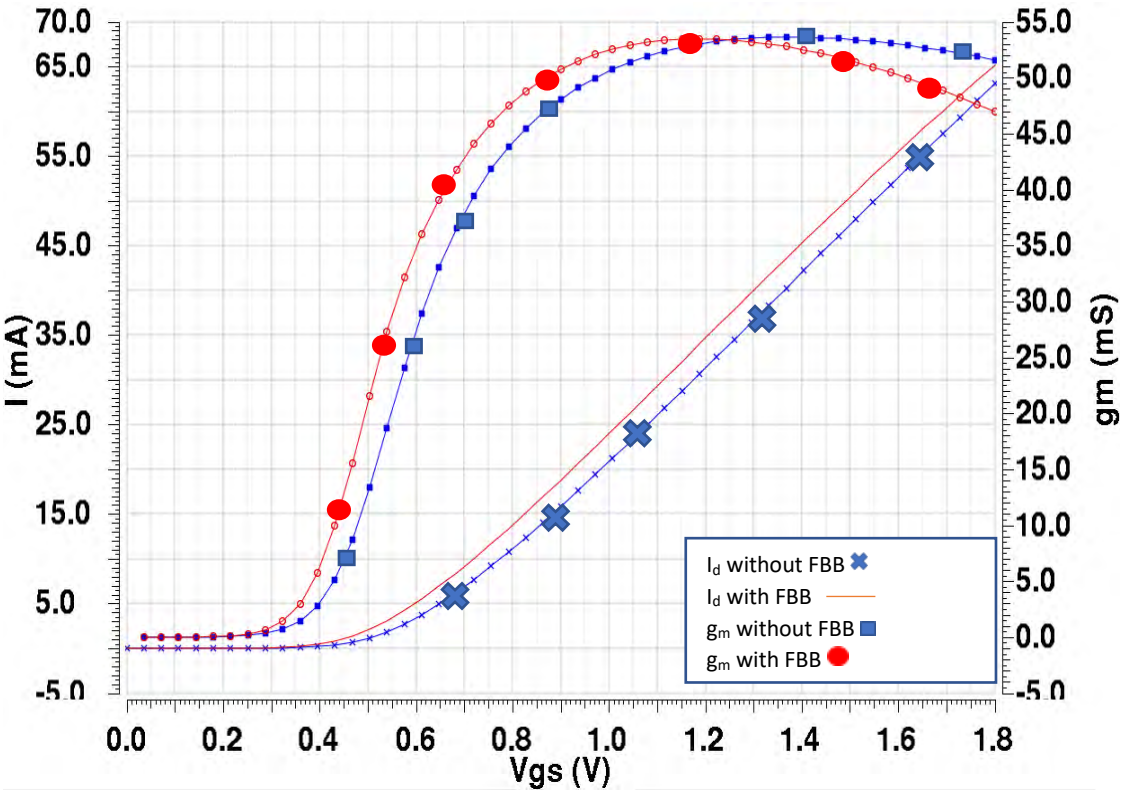


Figure 2.13 Drain current (I) vs Vgs and gm vs Vgs for FBB and without FBB

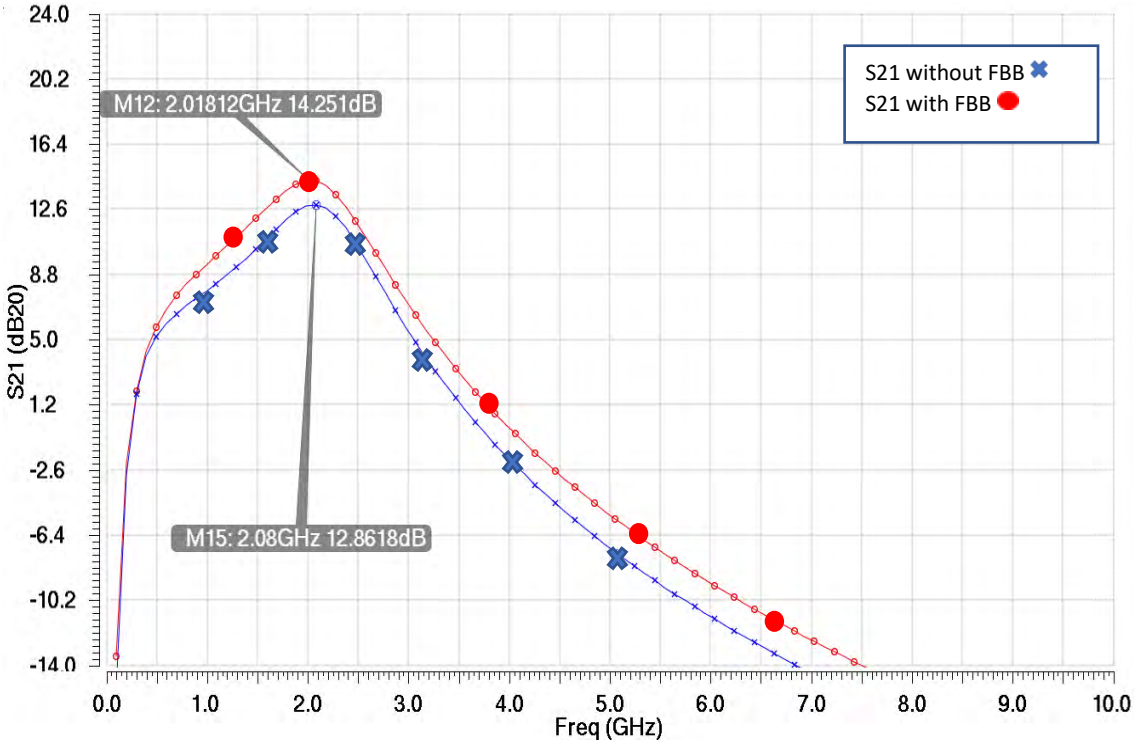


Figure 2.14 Gain with and without FBB.

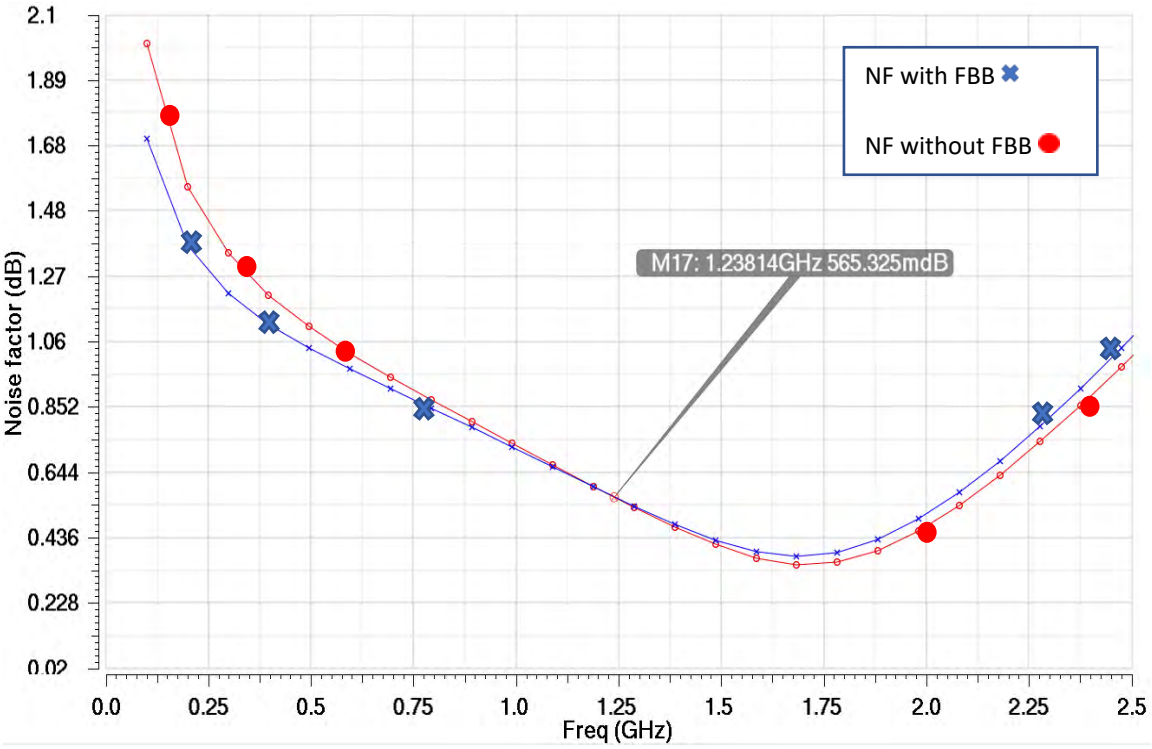


Figure 2.15 NF with and without FBB.

Figure (2.14) is the gain of the CS with FBB and without, an increase in gain of about 1.5dB due to FBB is noticed. Figure (2.15) NFmin for the CS with and without FBB. FBB reduced the noise at low frequencies and increased it in high frequencies. By connecting the gate to the bulk, Vth is decreased, hence the voltage required to turn on the device is decreased [8].

Chapter 3. Low Noise Amplifiers

3.1 Noise

Noise factor (F) or noise figure (NF) is used to characterize the noise performance of an RF system. It represents the ratio of output noise power to the input noise power; the NF and gain are the main figure of merit for an LNA. An ideal noiseless system will add no noise, meaning F=1 or NF=0dB. In general, NF is a function of the source impedance, where the noise power is normalized and divided by source resistance, R_s. Since most RF system are designed with an input and output impedance of 50Ω, this eliminates the ambiguity of the NF definition.

The Friis equation (3.42) indicates that the noise from the block following the LNA (usually the mixer) is reduced by the gain of the LNA when referred to the input. The LNA should be placed as close to the antenna as possible so the weak RF input is first amplified with the addition of a little noise as possible before further processing. That is why the NF and gain are the two most important figure of merit of the LNA.

3.1.1 Thermal noise of resistors: The thermal noise of a resistor can be modeled as a voltage noise source in series with a noiseless resistor.

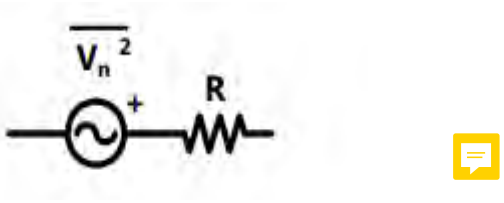


Figure 3.1 Resistor thermal noise model.

The resistor thermal noise is:

$$\overline{V_n^2} = 4KTR\Delta f \tag{3.1}$$

where K is Boltzmann's constant, T is the absolute temperature given in kelvin, and Δf is the bandwidth of interest in Hz.

3.1.1 Drain current noise (thermal noise) of MOSFETs: The drain current noise in the MOSFET is can be modeled as current source connected in parallel between the drain and source with the g_m of the transistor. Its power is given as [12]:

$$\overline{i_n^2} = 4KT\gamma g_{do}\Delta f \tag{3.2}$$

where γ = McWhorther tunneling parameter (2/3 for long channel) and $g_{do} = g_m/\alpha$

Common gate noise due to drain noise when the output is connected to ground:

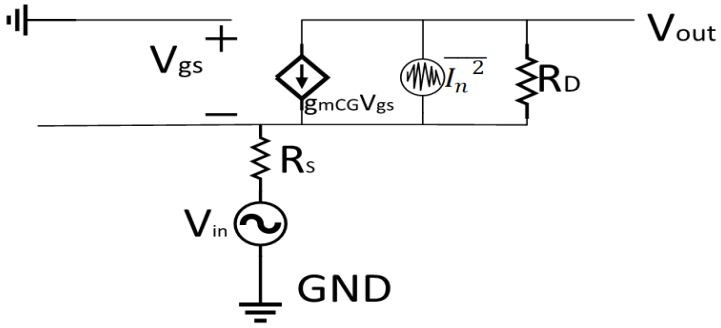


Figure 3.2 Common gate small signal model with thermal noise

$$I_s = g_m v_{gs} + \overline{I_n} \tag{3.3}$$

$$I_s = -g_m I_s R_s + \overline{I_n} \tag{3.4}$$

$$I_s = \frac{\overline{I_n}}{1 + g_m R_s} \tag{3.5}$$

$$\overline{I_{out}} = I_s \tag{3.6}$$

$$\overline{I_{out}}^2 = I_s^2 \tag{3.7}$$

$$\overline{I_{out}}^2 = \left(\frac{\overline{I_n}}{1 + g_m R_s}\right)^2 \tag{3.8}$$

$$\overline{I_{out}}^2 = 4KT\gamma g_{do}\left(\frac{1}{1 + g_m R_s}\right)^2 \tag{3.9}$$

Noise due to source resistance when the output is connected to ground:

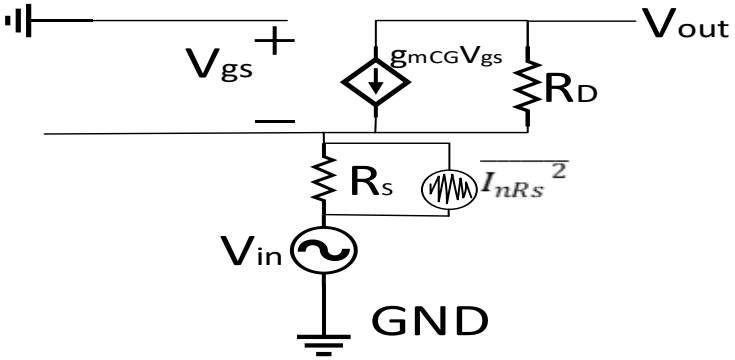


Figure 3.3 Common gate small signal model with source resistor thermal noise

$$\overline{I_{s-out}} = g_m V_{gs} \tag{3.10}$$

Using voltage division:

$$V_{gs} = \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_s} \overline{V_n} \tag{3.11}$$

Therefore:

$$\overline{I_{s-out}} = (g_m) \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_s} \overline{V_n} \tag{3.12}$$

Squaring:

$$\overline{I_{s-out}^{\,2}} = (g_m^2) \frac{\frac{1}{g_m^2}}{\left(\frac{1}{g_m} + R_s\right)^2} 4KTR_s \tag{3.13}$$

$$= \frac{g_m^2}{(1 + g_m R_s)^2} 4KTR_s \tag{3.14}$$

Dividing the drain noise by the source noise:

$$\frac{\overline{I_{out}^{\,2}}}{\overline{I_{s-out}^{\,2}}} = \frac{4KT\gamma g_{do} \left(\frac{1}{1 + g_m R_s}\right)^2}{\frac{g_m^2}{(1 + g_m R_s)^2} 4KTR_s} = \frac{\gamma g_{do}}{g_m^2 R_s} \tag{3.15}$$

Finally, the known equation of F is derived:

$$F = \frac{\overline{I_{s-out}^{\,2}}}{\overline{I_{s-out}^{\,2}}} + \frac{\overline{I_{out}^{\,2}}}{\overline{I_{s-out}^{\,2}}} = 1 + \frac{\gamma g_{do}}{g_m^2 R_s} \tag{3.16}$$

$$= 1 + \frac{\gamma}{\alpha g_m R_s} \tag{3.17}$$

*If $1/g_m = R_s$,

$$F = 1 + \frac{\gamma}{\alpha} \tag{3.18}$$

where γ is excess noise factor (2/3 in long channel devices) and α is g_m/g_{do} (g_{do} is the channel resistance when $V_{ds} = 0$).

Common gate noise due to drain noise, when the output is connected to ground and channel length modulation (r_o) is considered ($r_o = 1/g_d$):

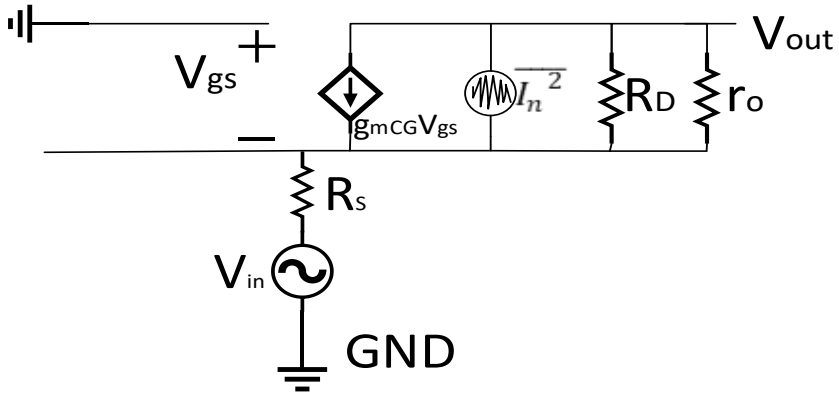


Figure 3.4 Common gate small signal model with thermal noise and channel length modulation

$$I_s = g_m v_{gs} + \overline{I_n} - v_s g_d \tag{3.19}$$

$$I_s = -g_m I_s R_s + \overline{I_n} - I_s R_s g_d \tag{3.20}$$

$$I_s = \frac{\overline{I_n}}{1 + g_m R_s + R_s g_d} \tag{3.21}$$

$$\overline{I_{out}} = I_s \tag{3.22}$$

$$\overline{I_{out}}^2 = {I_s}^2 \tag{3.23}$$

$$\overline{I_{out}}^2 = \left(\frac{\overline{I_n}}{1 + g_m R_s + R_s g_d}\right)^2 \tag{3.24}$$

$$\overline{I_{out}}^2 = 4KT\gamma g_{do}\left(\frac{1}{1 + g_m R_s + R_s g_d}\right)^2 \tag{3.25}$$

Equation (3.25) is the CG thermal noise equation when the channel length modulation is taken into consideration. Since g_d is in the denominator, increasing it will result in less noise, this means the lower the channel length modulation parameter (r_o) is, the larger g_d is and less noise is produced. Lowering r_o is also desirable for its negative effect on the gain of the transistor.

Noise due to source resistance, when the output is connected to ground and channel length modulation (r_o) is considered ($r_o = 1/g_d$):

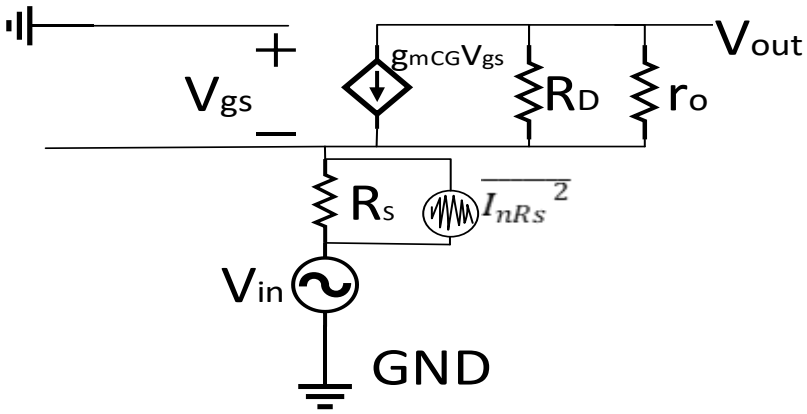


Figure 3.5 Common gate small signal model with source resistance thermal noise and channel length modulation

$$\overline{I_{s-out}} = g_m V_{gs} + V_{gs} g_d = V_{gs}(g_m + g_d) \tag{3.26}$$

Using voltage division:

$$V_{gs} = \frac{\frac{1}{g_m} \parallel r_o}{\frac{1}{g_m} \parallel r_o + R_s} \overline{V_n} \tag{3.27}$$

$$= \frac{r_o}{r_o + g_m r_o R_s + R_s} \overline{V_n} \tag{3.28}$$

$$= \frac{1}{1 + g_m R_s + R_s g_d} \overline{V_n} \tag{3.29}$$

Therefore:

$$\overline{I_{s-out}} = \frac{(g_m + g_d)}{1 + g_m R_s + R_s g_d} \overline{V_n} \tag{3.30}$$

Squaring:

$$\overline{I_{s-out}{}^2} = \left(\frac{(g_m + g_d)}{1 + g_m R_s + R_s g_d} \right)^2 4KTR_s \tag{3.31}$$

Dividing the drain noise by the source noise:

$$\frac{\overline{I_{out}{}^2}}{\overline{I_{s-out}{}^2}} = \frac{4KT\gamma g_{do}\left(\frac{1}{1+g_m R_s + R_s g_d}\right)^2}{\left(\frac{(g_m+g_d)}{1+g_m R_s + R_s g_d}\right)^2 4KTR_s} \tag{3.32}$$

$$= \frac{\gamma g_{do}}{(g_m+g_d)^2 R_s} \tag{3.33}$$

Finally, F is derived:

$$F = \frac{I_{s-out}{}^2}{\overline{I_{s-out}{}^2}} + \frac{\overline{I_{out}{}^2}}{\overline{I_{s-out}{}^2}} \tag{3.34}$$

$$= 1 + \frac{\gamma g_{do}}{(g_m+g_d)^2 R_s} = 1 + \frac{\gamma g_m}{\alpha(g_m+g_d)^2 R_s} \tag{3.35}$$

*if $r_o$is large, then g_d is small and $1/g_m = R_s$. Equation (3.42) becomes:

$$g_m + g_d \approx g_m \tag{3.36}$$

$$F = 1 + \frac{\gamma g_m}{\alpha(g_m)^2 R_s} \tag{3.37}$$

$$F = 1 + \frac{\gamma}{\alpha} \tag{3.38}$$

Equation (3.18) is the same noise equation as (3.38) if channel length modulation resistance is assumed to be large. Meaning whether channel length modulation is considered or not, the same noise can be derived.

3.1.2 Noise figure: Noise Figure indicates the noise deterioration of a block. It is defined as the ratio of input signal-to-noise ratio (SNR_{in}) to output signal-to-noise ratio (SNR_{out}).

$$NF(dB) = 10\log(NR) = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) \tag{3.39}$$

where NF is the Noise Figure and NR is the Noise Ratio.

One can approximate the NR of the receiver using Friis Formula as:

$$NR_{RX} = NF_{LNA} + \frac{NF_{rest} - 1}{Gain_{LNA}} \tag{3.40}$$

NF_{rest} is the noise factor of the following stages.

3.1.3 Flicker noise: Flicker noise is associated with MOSFETs only, also known as pink noise. The flicker noise equation is:

$$\overline{i_n^2} = Kg_m^2 \frac{1}{f} \frac{1}{WLC_{ox}^2} \tag{3.41}$$

where K is a process dependent constant, W is the channel width and L is the channel length

Flicker noise heavily appears in low frequencies, around the DC point, thus acting as a DC offset. This will damage the signal after mixing, since the signal after mixing is down converted to low frequencies. Therefore, some DC blockage is needed. Reducing flicker noise can be done by increasing gate voltage.

3.2 Low Noise Amplifiers

The LNA, Low Noise Amplifier, is an essential building block for receivers of wireless circuit. The signals received at the antenna are weak and must be amplified so that they can be processed. This amplification must be done with care to add as little additional noise as possible, this way the signal proceeds to the rest of the circuit in the best possible conditions. According to the Friis' formula, which shows the relation between the signal-to-noise ratio (SNR), the noise factor (F) of a system can be represented in cascade as:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_m - 1}{G_1 G_{2 \ldots G_{m-1}}} \tag{3.42}$$

where F_m and G_m are the noise factor and power gain of the m^{th} stage. Looking at (3.1), the dominant factor of the noise is the first stage, which is usually the LNA.

To maximize the gain, the power transmission should be maximized. This is done by making sure no reflection of the signal occurs at the input or output of any elements, not just the LNA. The reflected signals are considered as noise. The absence of reflection can be insured with proper matching networks.

In addition to gain and noise requirements, the LNA must be as linear as possible, as mentioned in Chapter 2, nonlinearity results in IMD terms that degrade the selectivity

of the receiver. There is a tradeoff between noise and linearity in the design of an LNA. Figure (3.6) shows the LNA's design tradeoffs, where one parameter is reduced to increase another. Although the main priority is low noise, having little gain or an unstable LNA is not acceptable.

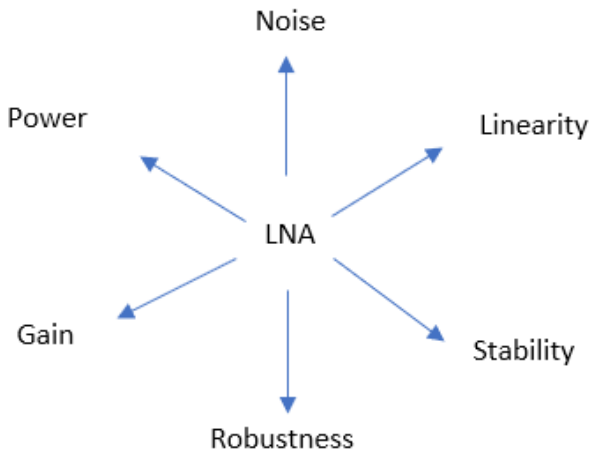


Figure 3.6 LNA trade-offs.

3.3 LNA Topologies

3.3.1 Common-source low-noise amplifier: The resistive input impedance can be achieved by adding an inductor in series with the gate (L_g) and an inductor in series with the source (L_s). Connecting a resistor or an inductor at the source of a CS is also known as degeneration. The CS LNA suffers from parasitic capacitors gate-drain capacitor C_{gs} and gate-source capacitor C_{gd}. C_{gd} provides a feedforward path from the input to output which decreases the reverse isolation, it can also interact with an inductive load making a negative resistance at the input, causing stability issues. To simplify calculations C_{gd} will be ignored, the impact of ignoring the capacitor C_{gd} in calculation is the increase of calculated bandwidth, gain and missing a pole of the circuit. The problem with missing a pole is if the pole itself is positive, the circuit becomes conditionally stable, poles do not need to be calculated as another stability test is chosen for the LNA. Figure (3.7) is the CS topology with the parasitic capacitors.

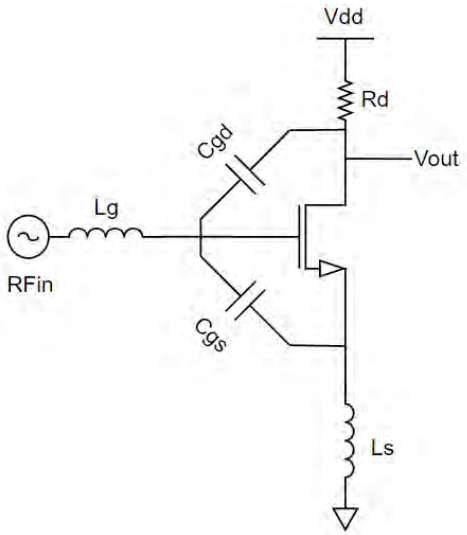


Figure 3.7 Common-Source with parasitic capacitors shown.

The input impedance of a CS with L_g and L_s:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L_s \tag{3.43}$$

In Z_{in} there is resistive components in the input impedance. To get purely resistive Z_{in}, L_g and L_s should take values to resonate out the C_{gs} at the operating frequency with $(g_m/C_{gs})L_s$ set to R_s (R_s *is usually set to* 50).

$$j\omega_o(L_g + L_s) + \frac{1}{j\omega_o C_{gs}} = 0 \tag{3.44}$$

$$\frac{g_m}{C_{gs}}L_s = R_s \tag{3.45}$$

$$\frac{g_m}{C_{gs}} \approx \omega_T \tag{3.46}$$

The main advantage of this topology is that the inductor synthesizes with the resistive component of the input impedance making it noiseless, unlike other topologies where a resistor is added in the signal path to provide the input impedance matching [13], this explains the low-noise performance and popularity of the inductive degenerated CS LNA. the main disadvantage is the extra cost of the circuit and the increase of size of the chip due to inductors generally being large.

3.3.2 Common-gate low-noise amplifier: In CG LNA the gate is AC shorted to ground and input signal is at the source terminal. The resistance looking into the source is $1/g_m$ when channel length modulation and body effect are ignored, this provides a simple input matching condition to R_s where $1/g_m = R_s$ satisfies the input matching. Unlike the CSLNA, there is no miller effect associated with the CG parasitic capacitance, this results in better isolation and a higher bandwidth. However, the CG suffers from a noisy channel conductance in the signal path, resulting in a higher NF. The F of the CG can be approximated to be, as derived in this chapter:

$$F = 1 + \frac{\gamma}{\alpha} \tag{3.47}$$

Although the CG offers a high bandwidth and an easier matching conditions, low power consumption and compact size (inductorless) [7], it suffers from higher noise and lower voltage gain than the CS [14].

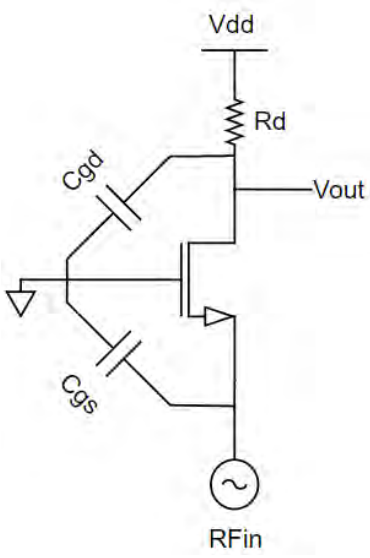


Figure 3.8 Common-Gate with parasitic capacitors shown.

Figures (3.7) and (3.8) show the two main parasitic capacitors of a transistor, C_{gs} and C_{gd}. They are responsible for the bandwidth limitation of transistors, unfortunately they are unavoidable and are due to the physical structure of the transistors.

3.3.3 Cascode structure: A cascode LNA structure is used with a CS. Instead of the drain of the CS connected to R_D, it is connected to the source of a second transistor which acts like a CG. The cascode structure reduces the miller effect of the CS stage which improves the bandwidth and improves input/output isolation. Having better input/output isolation improves stability and makes the input and output matching independent of each other.

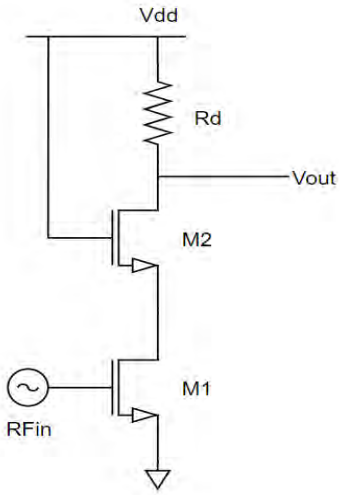


Figure 3.9 Cascode structure.

Unfortunately, the cascode structure does require more headroom voltage and increases the total noise of the LNA due to M2 noise contribution.

3.3.4 Differential LNA: Any single ended design can be transformed into a differential pair by adding a mirror copy of the original single stage and connecting the sources. The main advantage of a differential design is its ability to cancel any common mode noise, such as thermal and supply noise. A balanced LNA is a differential LNA but a differential LNA is not necessarily a balanced one. Balanced LNA referred to the differential LNA with both output nodes equal in voltage.

Figures (3.10) and (3.11) are CS and CG differential amplifiers respectively, each with its own set of uses. the CS amplifiers takes the AC input from the gate while the CG amplifier takes the AC input to the source.

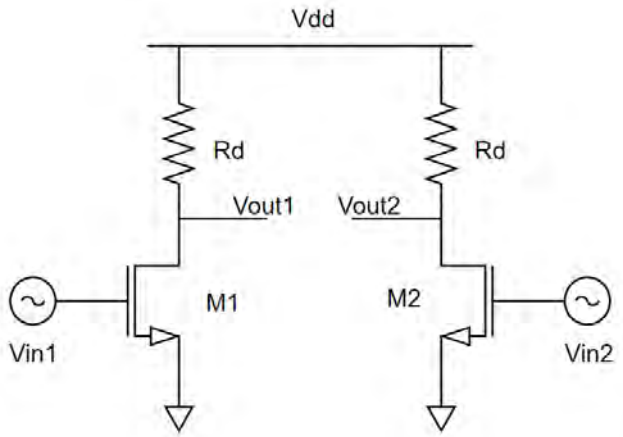


Figure 3.10 CS differential pair.

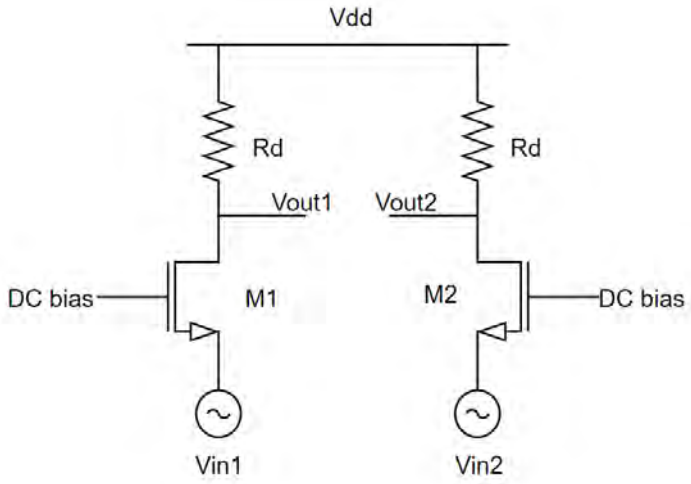


Figure 3.11 CG differential pair.

Differential signaling is preferred to reduce second-order distortion and to reject power supply, substrate, and thermal noise. Single input is preferred to save pins, but not necessarily area, as one bulky transistor might consume more power and chip area than two transistor working in differential pair [7].

Combining a CG and a CS differential amplifier will result in what is known as a Balun amplifier. The Balun amplifier is studied in this thesis, deriving a new noise figure, an improved noise figure and simulating it when powered by a harvester. It is known to be an unbalanced output design with a set condition to fix the unbalance issue while still maintaining a wideband.

3.3.5 Balun LNA: A differential amplifier that combines a common-gate and common-source acting as a differential pair is known as the Balun LNA, the input of the LNA is applied to both CS and CG at the same time. The Wideband Balun LNA with resistors represented in figure (3.12) has two stages: a common gate (CG) and a common-source (CS) stage. This circuit has the functionality of Balun because the entry of the LNA has a single-ended input and delivers a differential output, the resisters are used as current drivers, and can be replaced by MOSFETS, making it a MOSFET only Balun LNA, which makes the circuit smaller, reduces cost , process and supply variation [6].

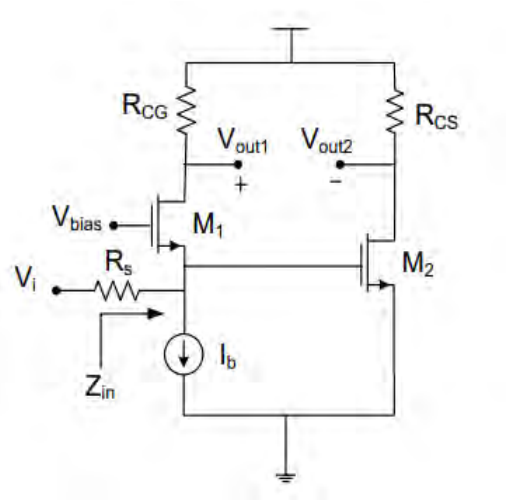


Figure 3.12 Balun LNA.

In [15], a thorough study on Balun LNA has been made and concluded with 3 main equation regarding the sizing of the transistor and how to make sure Balun effect is achieved. Also, it studied the gain imbalances that can appear if not sized properly. It also discusses how to achieve the maximum gain and least noise figure. Figure (3.13) are the graphs showing NF, gain and gain imbalance vs 'n' factor. The n factor represents a multiplier for the g_m and resistors. For the best noise performance, the third set of condition must be applied. And for purely more gain, second set is preferred.

In this chapter, a new noise figure is derived for the Balun LNA showing that the thermal noise can be completely canceled and an additional improvement on how to cancel the thermal noise and balance the output using a degeneration resistor at the common-source side.

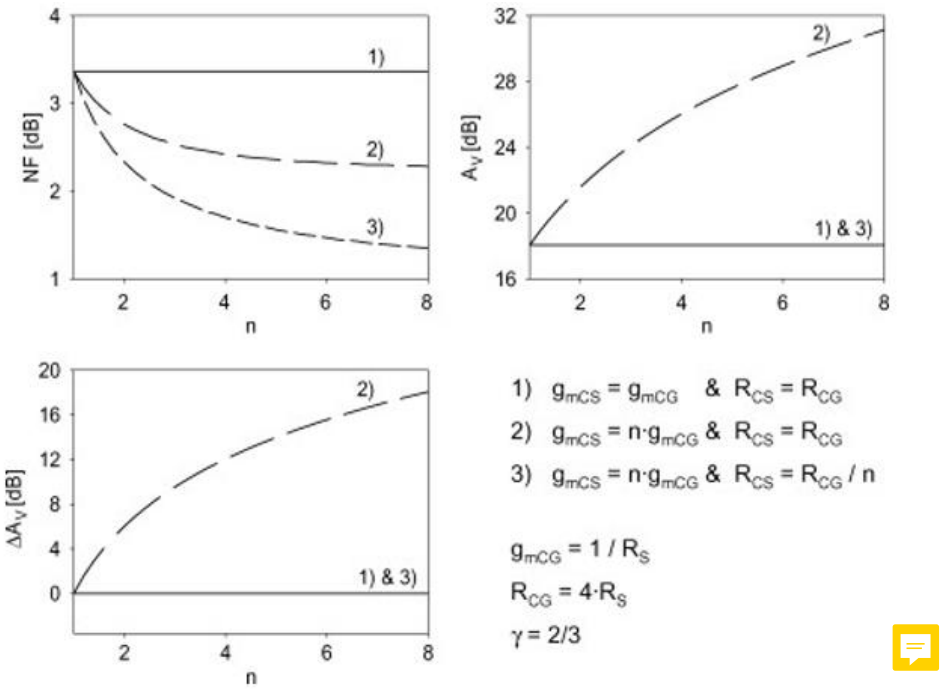


Figure 3.13 Balun LNA equations and graphs.

The output can be balanced if the magnitudes of the gains of the two stages are adjusted to an approximate value, because the common-source (CS) stage has the function of an inverter, while the common-gate (CG) does not, the differential voltage gain is taken between the drains of the two transistors. Their expression is as follow [16]:

$$A_{voutCG} = (g_{mCG} + g_{mbCG})(R_{CG} \parallel ro_{CG}) \tag{3.48}$$

where g_{mCG} is the transconductance of the CG, g_{mbCG} is the body effect of the CG, R_{CG} is the drain resistance of the CG and ro_{CG} is channel length modulation of the CG,

$$A_{voutCS} = (-g_{mCS})(R_{CS} \parallel ro_{CS}) \tag{3.49}$$

where g_{mCS} is the transconductance of the CS, R_{CS} is the drain resistance of the CS and ro_{CS} is channel length modulation of the CS

The differential gain is given by:

$$A_{vdiff} = A_{voutCG} - A_{voutCS} \tag{3.50}$$

The input impedance is [6]:

$$R_{in} = \frac{1 + (\frac{1}{ro_{CG}} R_{CG})}{g_{mCG} + g_{mbCG} + \frac{1}{r_{oCG}}} \quad (3.51)$$

To cancel the noise contribution of the first stage, the common-gate (CG) stage, is possible if both stages have the same voltage gain. This happens because the first stage's noise appears as a common-mode signal at the differential output [6] [15]. According to [15], if the (CS) linearity is assured, the circuit will have good linearity. Also, according to [15], the noise factor is (the CS noise referred to the input was ignored).

$$F = 1 + \frac{\gamma g_{mCG}(R_{CG} - R_S g_{mCS} R_{CS})^2}{R_s A^2{}_V} + \frac{\gamma g_{mCS} R_{CS}^2 (1 + g_{mCG} R_S)^2}{R_s A^2{}_V} + \frac{(R_{CG} + R_{CS}(1 + g_{mCG} R_S))^2}{R_s A^2{}_V} \quad (3.52)$$

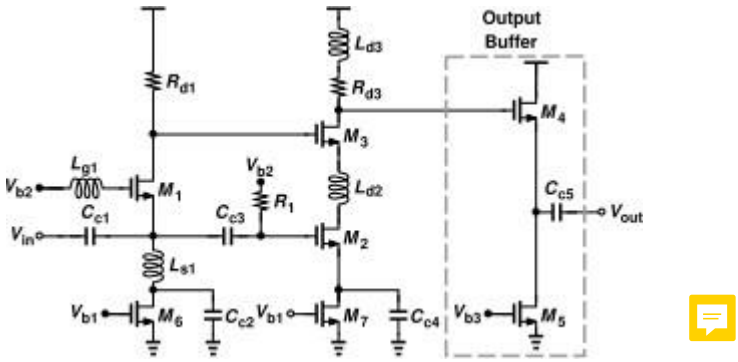


Figure 3.14 Improved Balun.

Figure (3.14), the design is a single input and single output improved Balun [17]. The output buffer is to avoid any loading effect and to have an output impedance as high as possible. The buffer power consumption was not included in the power measurement. The same idea will be applied to the design, where buffers will be added for isolation and their power consumption not taken into consideration. Also, no new noise figure was derived, which this thesis will do.

In [8] an 130nm ultra-low power (ULP) and ultra-low volt (ULV) was achieved using FBB and a huge circuit of 0.39mm^2 , it used a CG in a current-reuse structure, implied an inductor gm boosting techniques, low-power input matching was achieved by an active shunt-feedback while the current of the feedback was reused by the input

of the transistor, a BW of 0.6-4.2Ghz using 0.5V and 500uA, achieving 4 NF and 14db gain. The auxiliary amplifier power was not included in the power measurement. The design of this thesis will adopt the FBB technique.

In [18], a Balun LNA was used with a CG stage before the Balun itself for matching purposes, but no CS degeneration resistor was added. In [19], Balun LNA was used, with cascaded structure on the CG, but no new noise figure was derived and no CS degeneration was used. In [20], instead of a global negative feedback technique which helps in improving NF and matching at the price of stability, a feedforward noise-canceling technique was used allowing for noise and impedance matching, while canceling the distortion and noise of the matching amplifiers. In [21], a resistive feedback was used to increase the bandwidth, the NF was improved by adding a gm-enhanced cascaded amplifiers with a source follower feedback. In [22], a Balun LNA and a wide tuning range synthesizer is used to cover major frequency bands of use today, the design does include a mixer and a programmable integration sampler and clock discrete-time filters, although the emphasis of the measurement where the LNA, no new noise figure or degeneration source where used. In [23], an ESD-protected Balun LNA with an inductorless broadband input matching is offered, the amplification stage exploited double current reuse and a single-stage thermal noise cancellation to enhance the gain, NF and power consumption. In [24], an inductorless Balun LNA for low power multiband and multi-standard radios is proposed, the LNA uses dual shunt feedback to reduce the bias current needed by the CG while this current is reused in the CS stage, the NF is derived but for the whole system not just the Balun LNA. In [25], a new modified current-bleeding (CBLD) technique was used to cancel the noise of the Balun LNA, this method helps solve the issue of balancing the Balun with different resistors causing phase mismatch due to different RC constant. A comparison between the conventional and modified CBLD technique is tested, the modified CBLD uses an extra resistor at the drain of the MOSFET in the CBLD circuit, this increases the input impedance seen by the source of the CBLD circuit (due to channel length modulation), therefore reducing the overall noise, unfortunately, the Balun NF derived is a cascaded structure Balun and not useful for this papers analysis.

In this thesis, a complete noise analysis will be derived. Showing how the thermal noise of both the CG and the CS of the Balun LNA can be canceled. Also, a degeneration resistor will be added to the CS stage of the Balun

3.4 Balun LNA Noise Analysis

The thermal noise of the Balun LNA will be analyzed fully, with CS thermal noise taken into consideration and showing how balancing the LNA will completely remove the thermal noise of both the CS and CG. Then, an additional analysis of the Balun LNA with degeneration resistor is derived, where it is shown how the degeneration resistor can cancel the thermal noise of both the CS and CG stage.

3.4.1 Noise analysis without degeneration resistor: First, the thermal noise analysis of the Balun LNA with the thermal noise of the CS stage taken into consideration [26]:

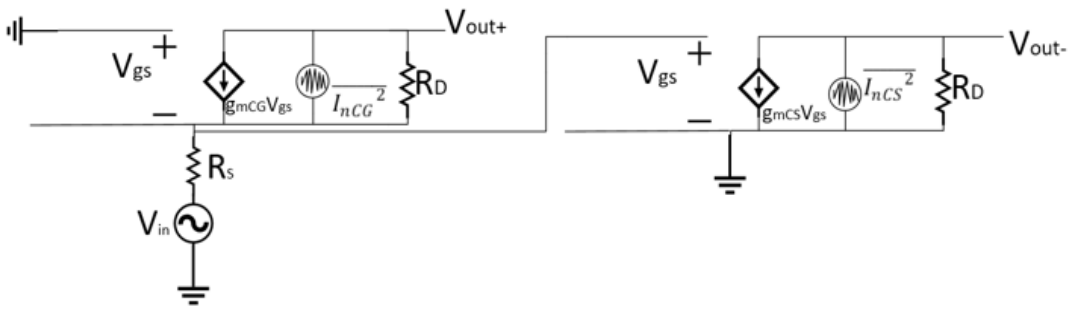


Figure 3.15 Balun LNA small signal model with thermal noise.

The gain of the CG is given by:

$$A_{vCG} = g_{mCG}R_{CG} \tag{3.53}$$

The gain of the CS is given by:

$$A_{vCS} = -g_{mCS}R_{CS} \tag{3.54}$$

The gain of the LNA is the difference between CG and CS gains:

$$A_{vLNA} = g_{mCG}R_{CG} + g_{mCS}R_{CS} \tag{3.55}$$

The voltage noise of the CG:

$$\overline{Vout_{CG}} = \overline{I_{nCG}}R_{CG} \tag{3.56}$$

CG noise referred to the input:

$$\overline{Vin_{CG}} = \frac{\overline{I_{nCG}}R_{CG}}{|A_{vCG}|} = \frac{\overline{I_{nCG}}}{g_{mCG}} \tag{3.57}$$

The output voltage noise of the CS:

$$\overline{Vout_{CS}} = \overline{I_{nCS}}R_{CS} \tag{3.58}$$

The CS noise referred to the input:

$$\overline{Vin_{CS}} = \frac{\overline{I_{nCS}}R_{CS}}{|A_{vCS}|} = \frac{\overline{I_{nCS}}}{g_{mCS}} \tag{3.59}$$

Total output noise of the CG when considering the input referred noise of the CS is:

$$\overline{Vout_{CG,total}} = \overline{I_{nCG}}R_{CG} + \frac{\overline{I_{nCS}}}{g_{mCS}} * g_{mCG}R_{CG} \tag{3.60}$$

The total output voltage noise of the CS when considering the input referred voltage noise of the CG is also given by:

$$\overline{Vout_{CS,total}} = \overline{I_{nCS}}R_{CS} + \frac{\overline{I_{nCG}}}{g_{mCG}} * g_{mCS}R_{CS} \tag{3.61}$$

The voltage noise of the source is:

$$\overline{V_{ns}} = \overline{V_n} * \left(\frac{R_{in}}{R_{in} + R_s}\right) \tag{3.62}$$

And $\overline{V_n}^2$ is the power of the noise given to be [6]:

$$\overline{V_n}^2 = 4KTR_S \tag{3.63}$$

Assuming, $R_{in} = \frac{1}{g_{mCG}}$, which is the low frequency matching condition of the CG

Therefore,

$$\overline{V_{ns}} = \overline{V_n} * \left(\frac{1}{1 + g_{mCG}R_S}\right) \tag{3.64}$$

where K is Boltzmann constant, T is temperature in kelvin and R is the source resistance

Total voltage noise of the LNA:

$$\overline{Vout_{LNA}} = \overline{Vout_{CG,total}} - \overline{Vout_{CS,total}} \tag{3.65}$$

Dividing by noise of the source resistance:

$$\frac{\overline{Vout_{LNA}}}{\overline{V_{ns}}} = \left(\overline{Vout_{CG,total}} - \overline{Vout_{CS,total}}\right) * \frac{1 + g_{mCG}R_S}{\overline{V_n}} \tag{3.66}$$

Substituting the proper terms and simplifying:

($\overline{V_n}$ *was moved to the left side to ease calculation*):

$$\frac{\overline{Vout_{LNA}}}{\overline{V_{ns}}} * \overline{V_n} =$$

$$\left(\begin{array}{c} \overline{I_{nCG}}R_{CG} + \dfrac{\overline{I_{nCS}}}{g_{mCS}} * g_{mCG}R_{CG} + \overline{I_{nCG}}R_{CG}g_{mCG}R_s \\ + \dfrac{\overline{I_{nCS}}}{g_{mCS}} * g_{mCG}R_{CG}g_{mCG}R_s \end{array}\right)$$

$$-$$

$$\left[\begin{array}{c} \overline{I_{nCS}}R_{CS} + \dfrac{\overline{I_{nCG}}}{g_{mCG}} * g_{mCS}R_{CS} + \overline{I_{nCS}}R_{CS}g_{mCG}R_s \\ + \dfrac{\overline{I_{nCG}}}{g_{mCG}} * g_{mCS}R_{CS}g_{mCG}R_s \end{array}\right] \tag{3.67}$$

Grouping terms containing $\overline{I_{nCG}}$:

$$\begin{array}{c} \overline{I_{nCG}}R_{CG} + \overline{I_{nCG}}R_{CG}g_{mCG}R_s - \dfrac{\overline{I_{nCG}}}{g_{mCG}} * g_{mCS}R_{CS} \\ - \dfrac{\overline{I_{nCG}}}{g_{mCG}} g_{mCS}R_{CS}g_{mCG}R_s \end{array} \tag{3.68}$$

Grouping terms containing $\overline{I_{nCG}}$ into two terms:

$$\overline{I_{nCG}}\left(R_{CG} - \frac{1}{g_{mCG}} * g_{mCS}R_{CS}g_{mCG}R_s\right) \tag{3.69}$$

$$= \overline{I_{nCG}}(R_{CG} - R_{CS}g_{mCS}R_s)$$

$$\overline{I_{nCG}}\left(R_{CG}g_{mCG}R_s - \frac{\bar{1}}{g_{mCG}} * g_{mCS}R_{CS}\right) \tag{3.70}$$

Grouping terms containing $\overline{I_{nCS}}$:

$$\frac{\overline{I_{nCS}}}{g_{mCS}} * g_{mCG}R_{CG} + \frac{\overline{I_{nCS}}}{g_{mCS}} * g_{mCG}R_{CG}g_{mCG}R_s - \overline{I_{nCS}}R_{CS} - \overline{I_{nCS}}R_{CS}g_{mCG}R_s$$

$$= \overline{I_{nCS}}\left(\frac{1}{g_{mCS}} * g_{mCG}R_{CG} + \frac{1}{g_{mCS}} * g_{mCG}R_{CG}g_{mCG}R_s - R_{CS} - R_{CS}g_{mCG}R_s\right) \tag{3.71}$$

After grouping the noise terms with their respective noise currents, next step is to add them back and square to get the noise power:

$$\frac{\overline{Vout_{LNA}}^2}{\overline{V_{ns}}^2} * \overline{V_n}^2 =$$

$$\overline{I_{nCG}}^2(R_{CG} - R_{CS}g_{mCS}R_s)^2 +$$

$$\overline{I_{nCG}}^2\left(R_{CG}g_{mCG}R_s - \frac{\bar{1}}{g_{mCG}} * g_{mCS}R_{CS}\right)^2 +$$

$$\overline{I_{nCG}}^2\left|(R_{CG} - R_{CS}g_{mCS}R_s)\left(R_{CG}g_{mCG}R_s - \frac{\bar{1}}{g_{mCG}} * g_{mCS}R_{CS}\right)\right| +$$

$$\overline{I_{nCS}}^2\left(\frac{1}{g_{mCS}} * g_{mCG}R_{CG} + \frac{1}{g_{mCS}} * g_{mCG}R_{CG}g_{mCG}R_s - R_{CS} - R_{CS}g_{mCG}R_s\right)^2 \tag{3.72}$$

Finally, dividing by the gain of the LNA squared to refer the noise to the input:

$$\overline{Vin_{LNA}}^2 =$$

$$\frac{\gamma g_{mCG}(R_{CG} - R_{CS}g_{mCS}R_s)^2}{R_s * A_{vLNA}^2} +$$

$$\frac{\gamma g_{mCG}\left(R_{CG}g_{mCG}R_s - \frac{\bar{1}}{g_{mCG}} * g_{mCS}R_{CS}\right)^2}{R_s * A_{vLNA}^2} +$$

$$\frac{\gamma g_{mCG}\left|(R_{CG}-R_{CS}g_{mCS}R_s)\left(R_{CG}g_{mCG}R_s-\frac{\bar{1}}{g_{mCG}}*g_{mCS}R_{CS}\right)\right|}{R_s*\ {A_{vLNA}}^2}+$$

$$\frac{\gamma g_{mCS}\left(\frac{1}{g_{mCS}}*g_{mCG}R_{CG}+\frac{1}{g_{mCS}}*g_{mCG}R_{CG}g_{mCG}R_s\right)^2}{R_s*\ {A_{vLNA}}^2} \quad (3.73)$$

The total NF is:

$$F=1+\ \overline{{Vin_{LNA}}^2}+\frac{(R_{CG}+R_{CS})(1+g_{mCG}R_S)^2}{R_s{A^2}_V} \quad (3.74)$$

$$g_{mCS}=\ ng_{mCG} \quad (3.75)$$

$$R_{CS}=\frac{R_{CG}}{n} \quad (3.76)$$

$$R_S=\frac{1}{g_{mCG}} \quad (3.77)$$

Substituting the balancing condition (3.75)-(3.77) from [15], into equation (3.73) will result in zero thermal noise.

3.4.2 Noise analysis with degeneration resistor: Another set of equations revolving around a CS degeneration resistor to balance the output and cancel the thermal noise is derived in **[27]**. If one would ignore condition set in **[15]**, and balance the Balun LNA with a degeneration resistor at the common source; assuming CS gain is higher than CG gain.

Balancing the LNA with R_{SCS}:

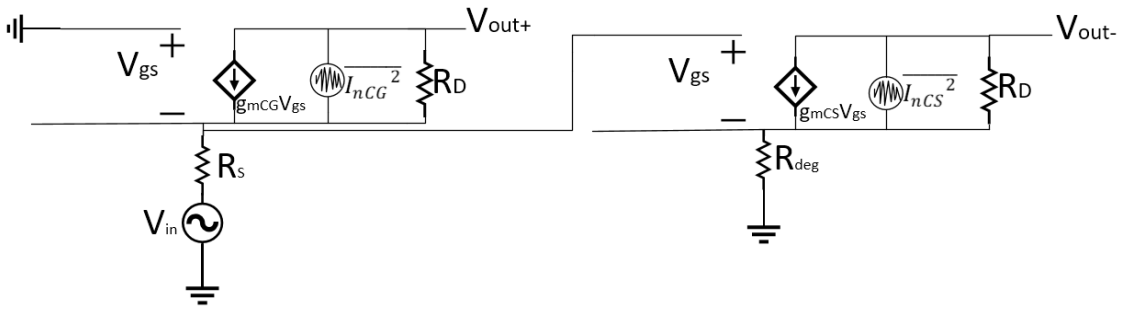


Figure 3.16 Balun LNA small signal model with thermal noise and CS degeneration resistor

The gain of the CG is given by:

$$A_{vCG} = g_{mCG}R_{CG} \tag{3.78}$$

The gain of the CS is given by:

$$A_{vCS} = -\frac{g_{mCS}R_{CS}}{1 + g_{mCS}R_{SCS}} \tag{3.79}$$

The voltage noise of the CG:

$$\overline{Vout_{CG}} = \overline{I_{nCG}}R_{CG} \tag{3.80}$$

CG noise referred to the input:

$$\overline{Vin_{CG}} = \frac{\overline{I_{nCG}}R_{CG}}{|A_{vCG}|} = \frac{\overline{I_{nCG}}}{g_{mCG}} \tag{3.81}$$

The output voltage noise of the CS:

$$\overline{Vout_{CS}} = \overline{I_{nCS}}R_{CS} \tag{3.82}$$

The CS noise referred to the input:

$$\overline{Vin_{CS}} = \frac{\overline{I_{nCS}}R_{CS}}{|A_{vCS}|} = \frac{\overline{I_{nCS}}(1 + g_{mCS}R_{SCS})}{g_{mCS}} \tag{3.83}$$

Total output noise of the CG when considering the input referred noise of the CS is (using the above equations):

$$\overline{Vout_{CG,total}} = \overline{I_{nCG}}R_{CG} + \frac{\overline{I_{nCS}}(1 + g_{mCS}R_{SCS})}{g_{mCS}} * g_{mCG}R_{CG} \tag{3.84}$$

The total output voltage noise of the CS when considering the input referred voltage noise of the CG is also given by:

$$\overline{Vout_{CS,total}} = \overline{I_{nCS}}R_{CS} + \frac{\overline{I_{nCG}}}{g_{mCG}} * \frac{g_{mCS}R_{CS}}{1 + g_{mCS}R_{SCS}} \tag{3.85}$$

The voltage noise of the source is:

$$\overline{V_{ns}} = \overline{V_n} * \left(\frac{R_{in}}{R_{in} + R_s}\right) \tag{3.86}$$

And $\overline{V_n{}^2}$ is the power of the noise given to be [6]:

$$\overline{V_n{}^2} = 4KTR_S \tag{3.87}$$

Assuming, $R_{in} = \frac{1}{g_{mCG}}$, which is the low frequency matching condition of the CG

Therefore,

$$\overline{V_{ns}} = \overline{V_n} * \left(\frac{1}{1 + g_{mCG}R_S}\right) \tag{3.88}$$

Where *K* is Boltzmann constant, *T* is temperature in kelvin and *R* is the source resistance

Total voltage noise of the LNA:

$$\overline{Vout_{LNA}} = \overline{Vout_{CG,total}} - \overline{Vout_{CS,total}} \tag{3.89}$$

Diving by noise of the source resistance:

$$\frac{\overline{Vout_{LNA}}}{\overline{V_{ns}}} = \left(\overline{Vout_{CG,total}} - \overline{Vout_{CS,total}}\right) * \frac{1 + g_{mCG}R_S}{\overline{V_n}} \tag{3.90}$$

Substituting the proper terms and simplifying:

($\overline{V_n}$ *was moved to the left side to ease calculation*):

$$\frac{\overline{Vout_{LNA}}}{\overline{V_{ns}}} * \overline{V_n} =$$

$$\left[\overline{I_{nCG}}R_{CG} + \frac{\overline{I_{nCS}}\,(1+g_{mCS}R_{SCS})}{g_{mCS}} * g_{mCG}R_{CG} + \overline{I_{nCG}}R_{CG}g_{mCG}R_s + \frac{\overline{I_{nCS}}\,(1+g_{mCS}R_{SCS})}{g_{mCS}} g_{mCG}R_{CG}g_{mCG}R_s\right.$$

-

$$\left.\left(\overline{I_{nCS}}R_{CS} + \frac{\overline{I_{nCG}}}{g_{mCG}} * \frac{g_{mCS}R_{CS}}{1 + g_{mCS}R_{SCS}} + \overline{I_{nCS}}R_{CS}g_{mCG}R_s + \frac{\overline{I_{nCG}}}{g_{mCG}} * \frac{g_{mCS}R_{CS}g_{mCG}R_s}{1 + g_{mCS}R_{SCS}}\right)\right] \tag{3.91}$$

Grouping $\overline{I_{nCG}}$ and $\overline{I_{nCS}}$:

$\overline{I_{nCG}}$:

$$\overline{I_{nCG}}\left[R_{CG} + R_{CG}g_{mCG}R_s - \frac{1}{g_{mCG}} * \frac{g_{mCS}R_{CS}}{1 + g_{mCS}R_{SCS}} - \frac{g_{mCS}R_{CS}R_s}{1 + g_{mCS}R_{SCS}}\right] \tag{3.92}$$

$\overline{I_{nCS}}$:

$$\overline{I_{nCS}}\left[\left(\begin{array}{c} \frac{1 + g_{mCS}R_{SCS}}{g_{mCS}} * g_{mCG}R_{CG} + \frac{(1 + g_{mCS}R_{SCS})}{g_{mCS}} * {g_{mCG}}^2R_{CG}R_s \\ -R_{CS} - R_{CS}g_{mCG}R_s \end{array}\right)\right] \tag{3.93}$$

After grouping the noise terms with their respective noise currents, next step is to add them back and square to get the noise power:

$$\frac{\overline{{Vout_{LNA}}^2}}{\overline{{V_{ns}}^2}} * \overline{{V_n}^2} =$$

$$\overline{{I_{nCG}}^2}\left[R_{CG} + R_{CG}g_{mCG}R_s - \frac{1}{g_{mCG}} * \frac{g_{mCS}R_{CS}}{1+g_{mCS}R_{SCS}} - \frac{g_{mCS}R_{CS}R_s}{1+g_{mCS}R_{SCS}}\right]^2$$

$$+$$

$$\overline{I_{nCS}{}^2}\left[\left(\begin{matrix}\frac{1+g_{mCS}R_{SCS}}{g_{mCS}} * g_{mCG}R_{CG} + \frac{(1+g_{mCS}R_{SCS})}{g_{mCS}} * g_{mCG}{}^2R_{CG}R_s \\ -R_{CS} - R_{CS}g_{mCG}R_s\end{matrix}\right)\right]^2 \quad (3.94)$$

An R_s is to be picked to cancel the thermal noise.

$$R_{scs} = \frac{g_{mCS}R_{CS} - g_{mCG}R_{CG}}{g_{mCS}g_{mCG}R_{CG}} \quad (3.95)$$

The R_s equation (7.41) is also the same equation found if $A_{vCG} = |A_{vCS}|$ and solving for R_s:

$$g_{mCG}R_{CG} = \frac{g_{mCS}R_{CS}}{1 + g_{mCS}R_{SCS}} \quad (3.96)$$

Substituting equation (3.95) in (3.94) results in zero thermal noise from the LNA.

Which means that canceling the transistors thermal noise using a degeneration resistor is possible.

Finally, dividing by the gain of the LNA squared to refer the noise to the input:

$$\overline{Vin_{LNA}{}^2} =$$

$$\frac{\gamma g_{mCG}\left(R_{CG} + R_{CG}g_{mCG}R_s - \frac{1}{g_{mCG}} * \frac{g_{mCS}R_{CS}}{1 + g_{mCS}R_{SCS}} - \frac{g_{mCS}R_{CS}R_s}{1 + g_{mCS}R_{SCS}}\right)^2}{R_s * A_{vLNA}{}^2}$$

$$+$$

$$\frac{\gamma g_{mCS}\left(\frac{g_{mCG}R_{CG}(1 + g_{mCS}R_{SCS})}{g_{mCS}} + \frac{(1 + g_{mCS}R_{SCS})g_{mCG}{}^2R_{CG}R_s}{g_{mCS}} - R_{CS} - R_{CS}g_{mCG}R_s\right)^2}{R_s * A_{vLNA}{}^2}$$

(3.97)

The total NF of the LNA with R_{SCS} is:

$$NF = 1 + \frac{\overline{Vin_{LNA}{}^2}}{} + \frac{(R_{CG} + R_{CS})(1 + g_{mCG}R_S)^2}{R_s A^2{}_V} + \frac{R_{SCS}}{R_s} \quad (3.98)$$

where the A_V is the gain of the LNA:

$$A_V = g_{mCG}R_{CG} + \frac{g_{mCS}R_{CS}}{1 + g_{mCS}R_{SCS}} \quad (3.99)$$

In addition to the condition set in [10], another balancing condition for the Balun LNA can be added by using a degeneration resistor. If the LNA is balanced, (7.42) will result in zero, meaning R_{SCS} does not need to be added.

If $g_{mCS} > g_{mCG}$ by a factor of "n" ,$R_{CS} > R_{CG}$ by a factor of "m" and the CG satisfies the matching condition $R_S = 1/g_{mCG}$ the following set of balancing condition can be derived:

$$g_{mCS} = ng_{mCG} \tag{3.100}$$

$$R_{CS} = mR_{CG} \tag{3.101}$$

$$R_S = \frac{1}{g_{mCG}} \tag{3.102}$$

Substituting equations (3.100), (3.101), (3.102) into equation (3.95):

$$R_{scs} = \frac{mng_{mCG}R_{CG} - g_{mCG}R_{CG}}{ng_{mCG}g_{mCG}R_{CG}} \tag{3.103}$$

Leads to

$$R_{scs} = \frac{mn - 1}{ng_{mCG}} \tag{3.104}$$

Leads to

$$R_{scs} = \frac{mn - 1}{n} * R_S \tag{3.105}$$

3.5 Simulation of Balun LNA with Degeneration

The LNA was design using UMC180nm technology on Cadence Virtuoso. Also, FBB was applied on the LNA. The simulation will compare an unbalanced output without a degeneration resistor and a balanced output with a degeneration resistor. PVT is done on the LNA to measure the change in gain, gain unbalance, noise, P1dB and phase. Figure (3.17) is the Balun LNA with degeneration resistor, the biasing is done using voltage source not current mirrors, current mirrors will be added later in the thesis once the overall circuit is designed. Table 5 are all the design variables and parameters of the transistors, resistors, capacitors, bias voltage and current through each of CS and

CG. The naming in Table 5 are the names of the elements in the UMC180nm PDK itself.

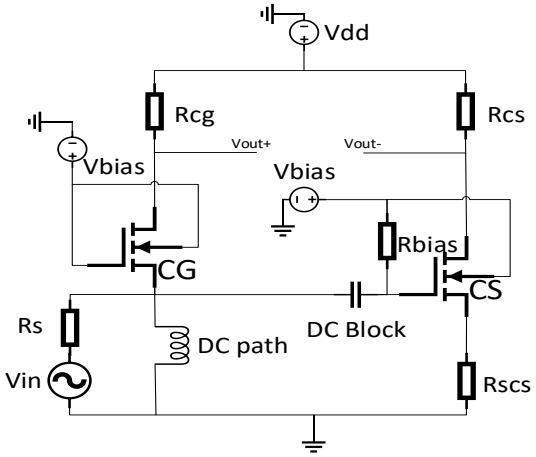


Figure 3.17 Balun LNA using UMC180nm NMOS with degeneration resistor.

Table 5. Balun LNA circuit details

Element	Description	CG	CS
N_L18W500_18_RF	Width (um)	120	315
N_L18W500_18_RF	Length (nm)	180	180
N_L18W500_18_RF	g_m (mS)	20	35
MIMCAPM_RF	DC block (pF)	-	10
RNNPO_RF	R_D (Ohm)	200	150
Resistor (Cadence library)	Degeneration (Ohms)	-	8
Vbias with R_{SCS}	Biasing (mV)	510	550
Vbias without R_{SCS}	Biasing (mV)	510	510
RNNHR_RF	Biasing (Ohm)	-	2K
Current	I_D (mA)	2.07	4.67

In Table 5 the width, length, biasing and R_D of the transistors where chosen to produce the least noise possible. The capacitor was used as an DC block for the CS and the biasing resistor was used as an RF choke to prevent AC grounding through the DC biasing of the RF input. The degeneration resistor was chosen from the analog library and not the UMC has two reasons; first is that the UMC PDK has the lowest resistor of value 136 ohms, meaning to get 8 ohm more than 16 resistors need to be in parallel, the second and most important reason is the analog library resistors have an option to disable the noise produced, disabling the noise is important to check the reduction of

noise due to balancing with degeneration. The currents of each CS and CG where the result of all other parameters. There are two different biasing voltages for the CS stage, the increase in biasing voltage when the degeneration resistor is added is to compensate for the lower current through the CS.

The Noise generated by the degeneration resistor was disabled to study if balancing with a degeneration source reduced the thermal noise. The thermal noise of the degeneration resistor is later enabled, this will have no effect on any other parameter other than noise.

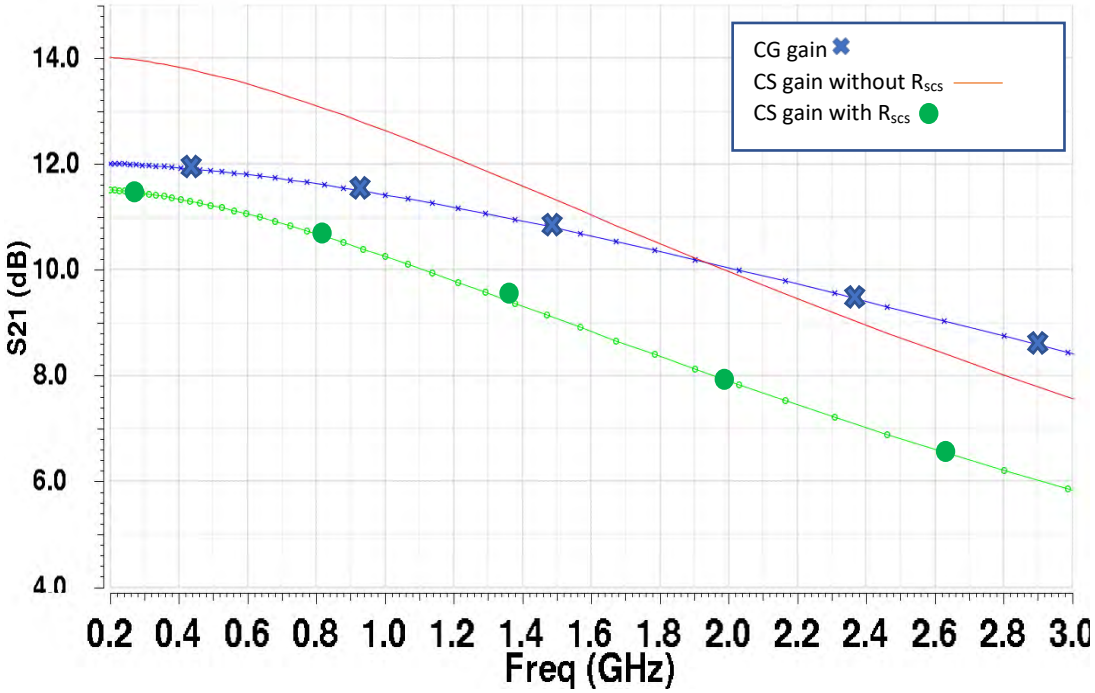


Figure 3.18 S21 of CG, CS without degeneration and CSS with degeneration

Figure (3.18) shows the gain of the CG, CS with degeneration and without. With the addition of a degeneration resistor to balance, the gain was reduced by 2.4dB. Also, from Table 5 the biasing voltage on the CS was increased from 510mV to 550mV to compensate for the lower current in the device due to the degeneration resistor. The change in biasing of CS did not affect the CG.

Before the addition of R_{SCS}, the gain unbalance at the low frequencies is 2dB. After the addition of the R_{SCS}, gain unbalance is reduced to 0.4dB. The noise was disable in the R_{SCS} to check the validity of whether the thermal noise can be canceled or reduced if balanced with a degeneration source.

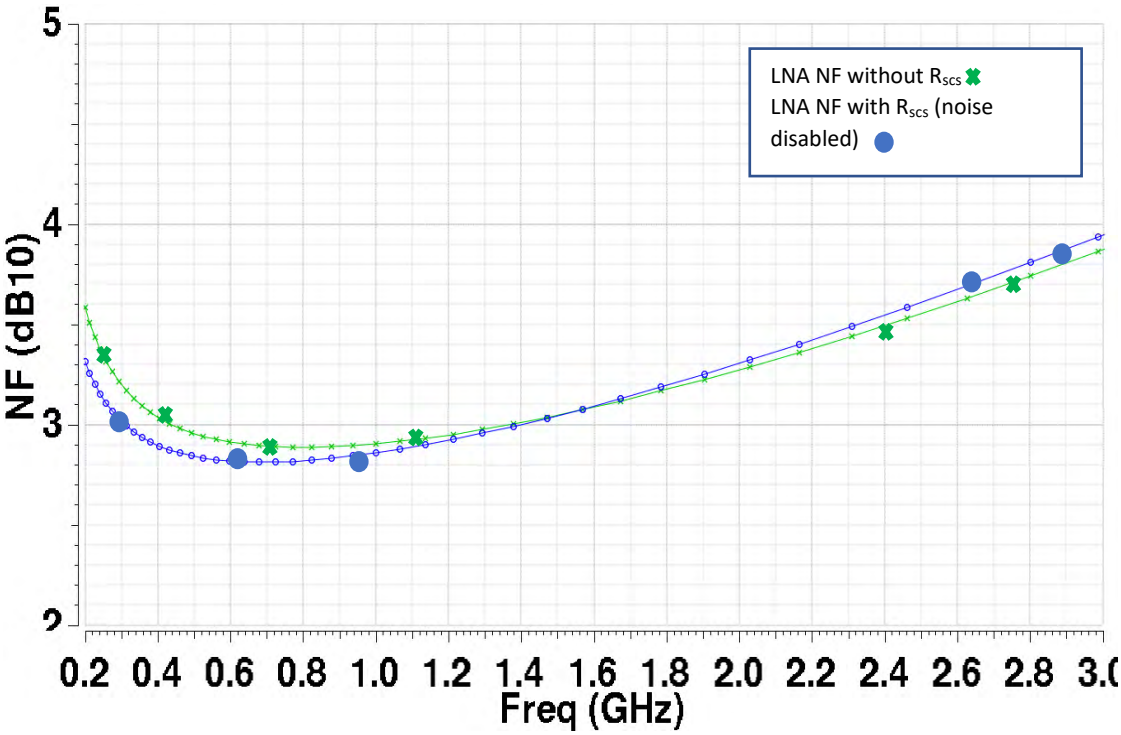


Figure 3.19 LNA NF with CS degeneration noise disabled and without CS degeneration.

The NF comparison between the LNA with and without R_{SCS} is shown in figure (3.19), a drop in NF at the low frequencies after balancing indicates that R_{SCS} can be used to balance and cancel the transistors thermal noise, meaning another degree of freedom has been added to the design of the Balun LNA. At higher frequencies, the gain unbalance is increased with the addition of a degeneration resistor, causing higher NF.

The addition of the degeneration resistor adds a degree of freedom to the design of the Balun LNA, although the overall noise is increased as shown in figure (3.20). Although the addition of the degeneration resistor increased the overall noise, the increase in P1dB and flexibility of the design is something to note. The P1dB will be tested at key frequencies (GSM and ISM) with and without the degeneration resistor. The gain is expected to decrease slightly as any degeneration element causes the gain equation to have a denominator (shown in (3.79)), decreasing the gain by a function of the value of the degeneration element. However due to the low value of the resistor added, the gain suffered a slight decrease.

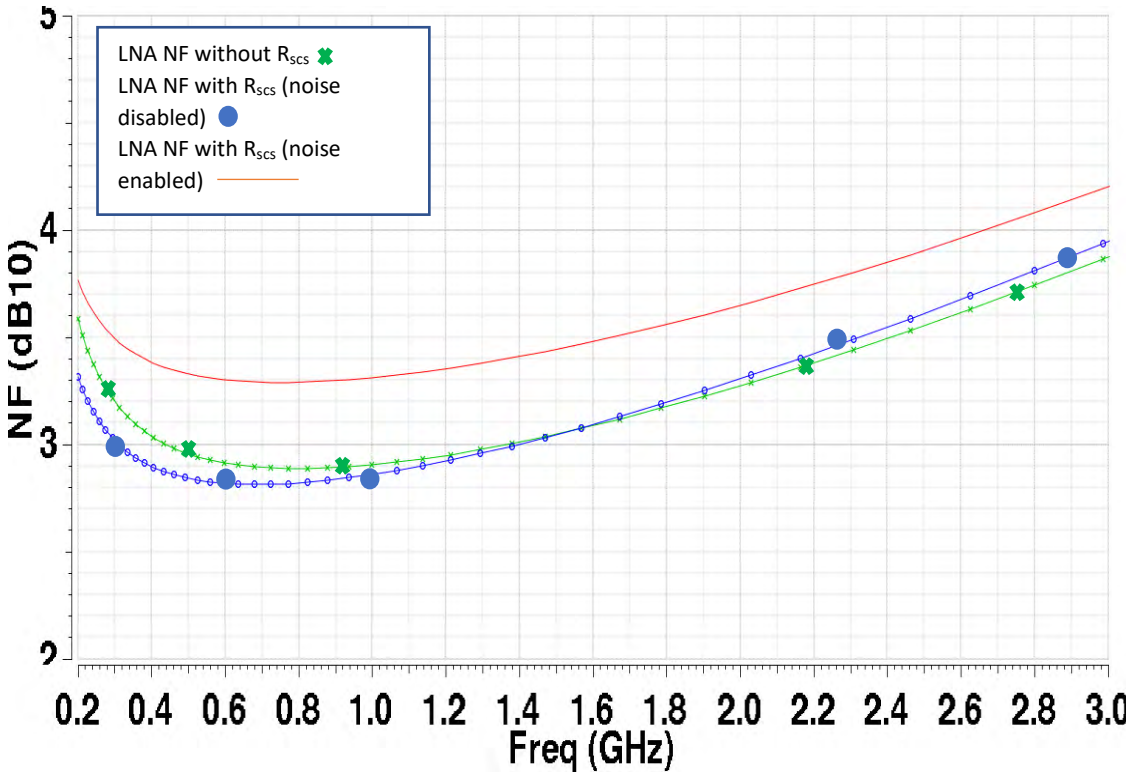


Figure 3.20 NF of the LNA without degeneration and with degeneration (noise enabled and disabled)

Figure (3.20) shows NF of the LNA when the noise of R_{SCS} was enabled, the overall NF of the LNA is increased by an average of 0.4dB due the resistors own thermal noise contribution. Also, the linearity increase due to addition of the degeneration source must be accounted for, figures (3.21) is the P1dB at 900MHz with degeneration and figure (3.22) is the P1dB at 900MHz without degeneration resistor, an increase of 1.4dBm input power to reach the p1dB is noticed due to the addition of the degeneration resistor. Figure (3.23) and figure (3.24) are the P1dB at 2.4GHz with and without a R_{scs} respectively, an increase in linearity is noticed with the addition of R_{scs} of around 0.6dBm.

Figure (3.25) is the LNA total voltage gain with R_{SCS}, and figure (3.26) is the total gain without R_{SCS}. Due to the degeneration resistor, the LNA lost 1.2dB in gain, but the bandwidth is increased by 200MHz, the loss is expected due to the degeneration resistor. Reducing the gain of the CS further will result in a higher bandwidth, this can be used to manipulate the bandwidth of the system.

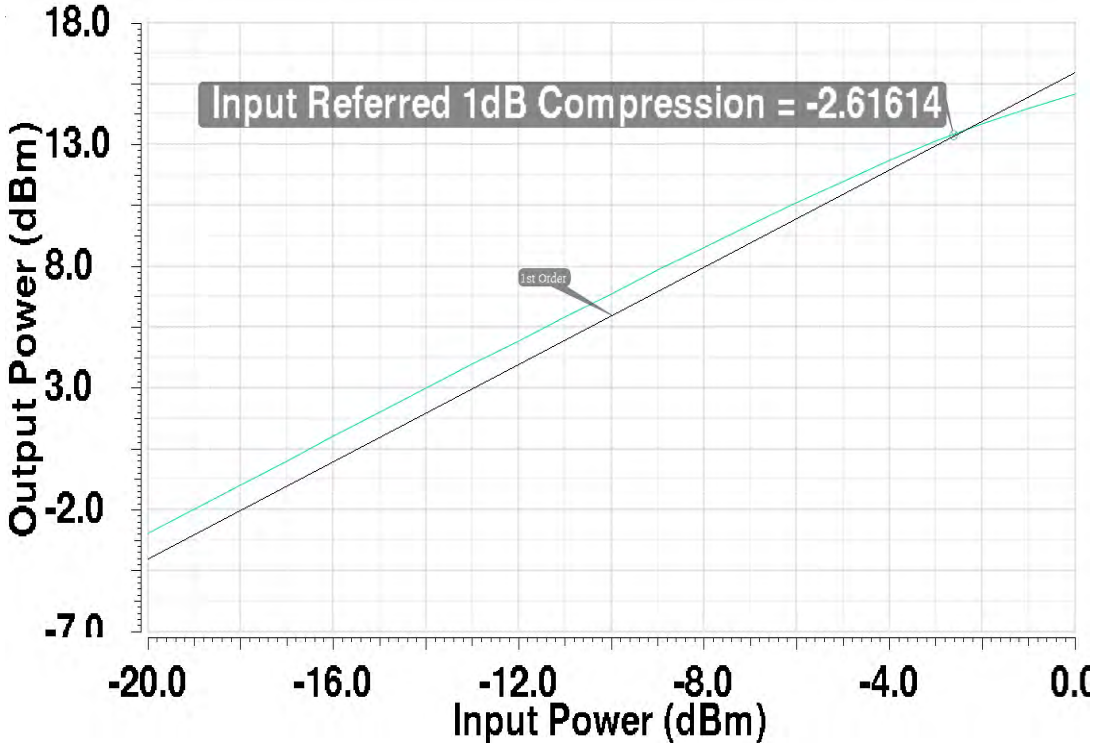


Figure 3.21 P1dB with Rscs, -2.6dBm @900MHz

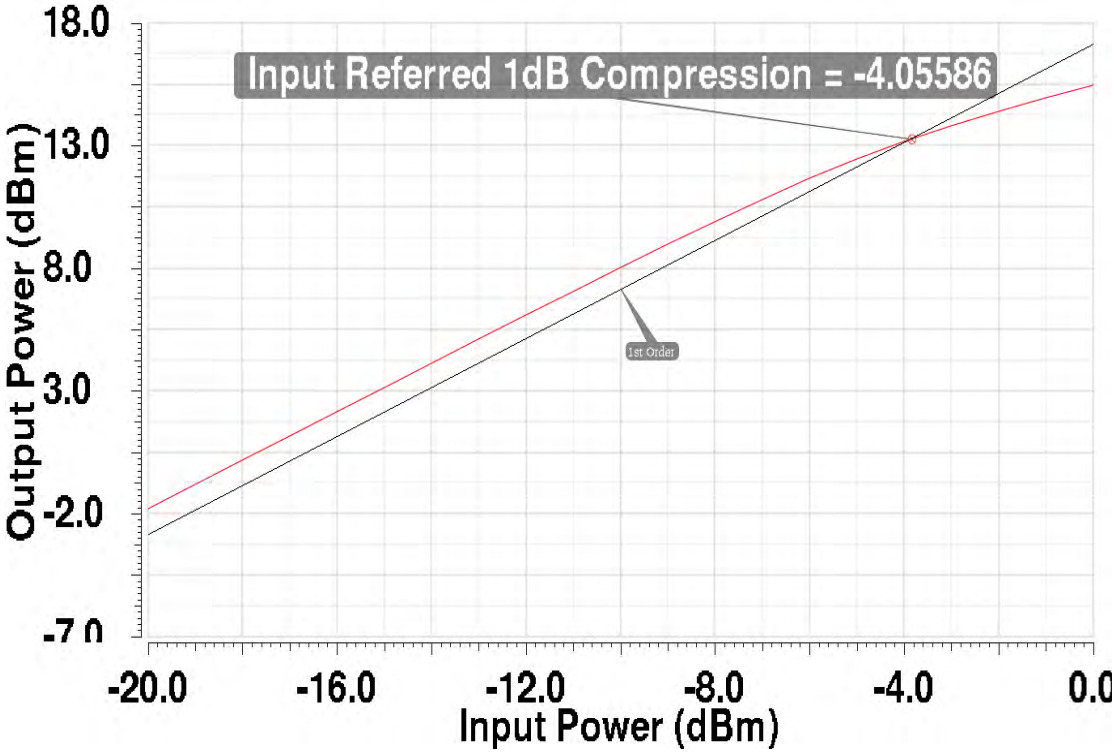


Figure 3.22 P1dB without Rscs. -4.05dBm @900MHz

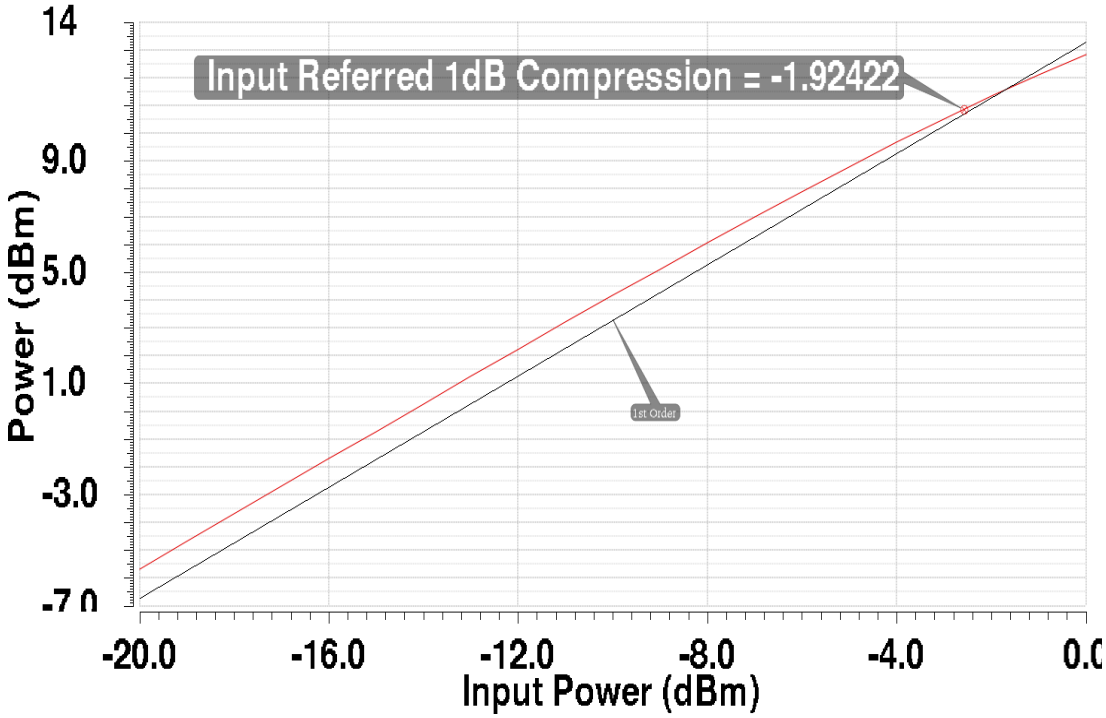


Figure 3.23 P1dB with Rscs. -1.9dBm @2.4GHz

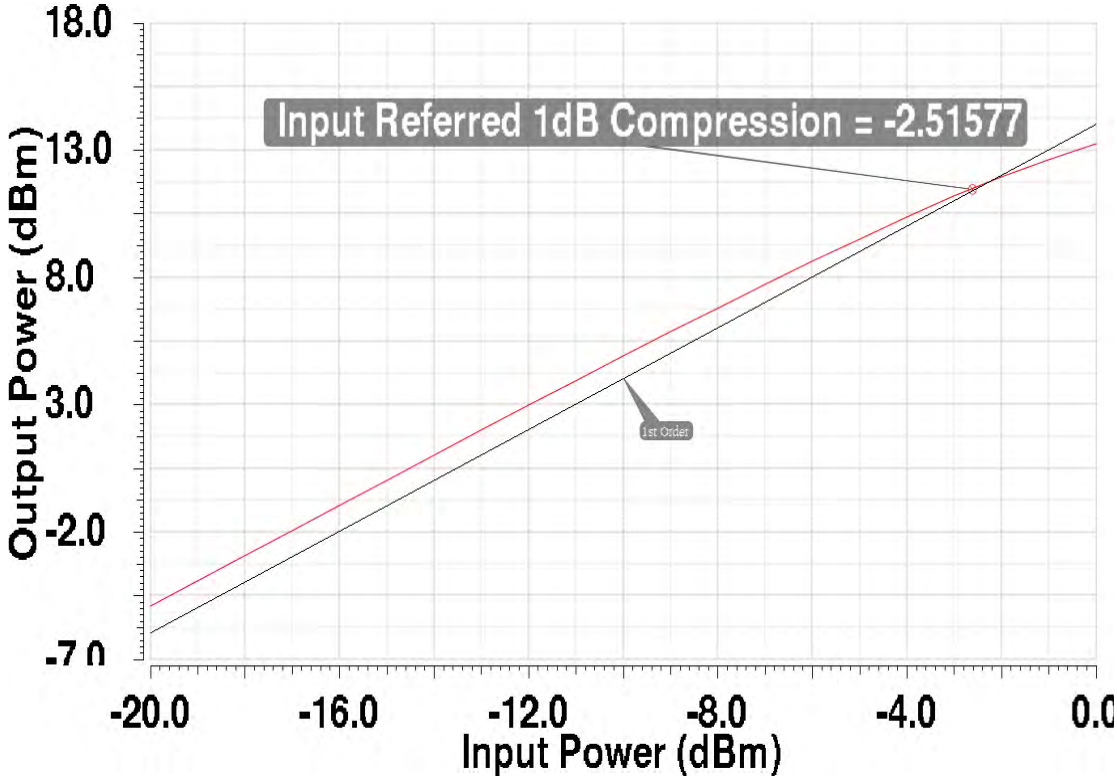


Figure 3.24 P1dB without Rscs. -2.5dBm @2.4GHz

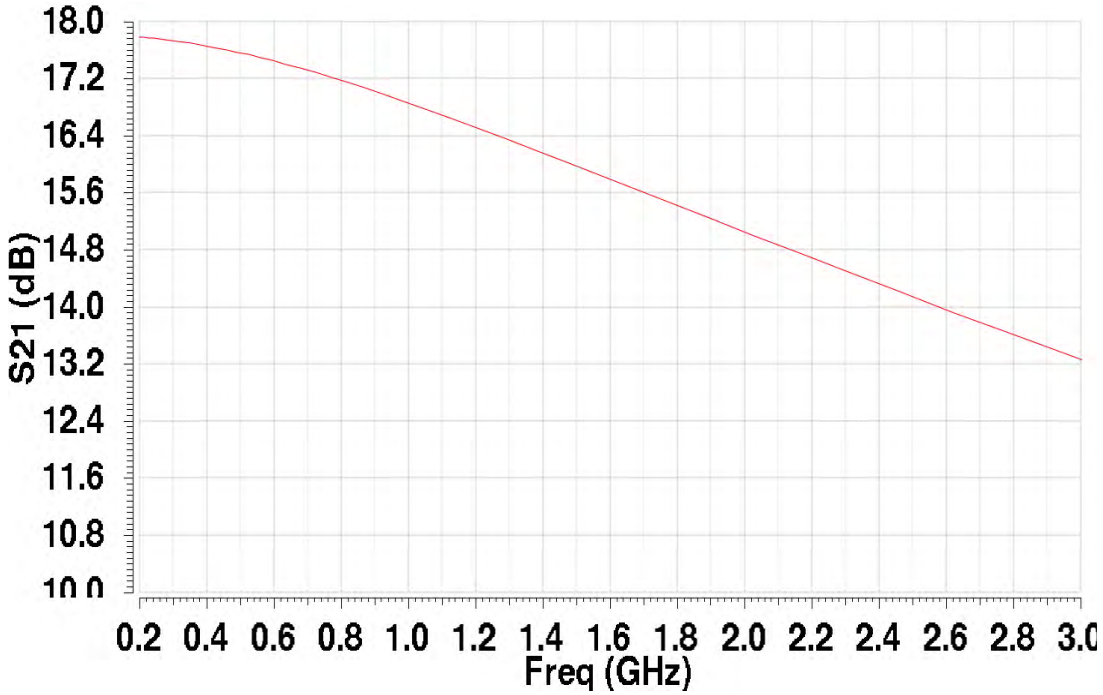


Figure 3.25 Total LNA gain with Rscs, BW=200M-2.1GHz

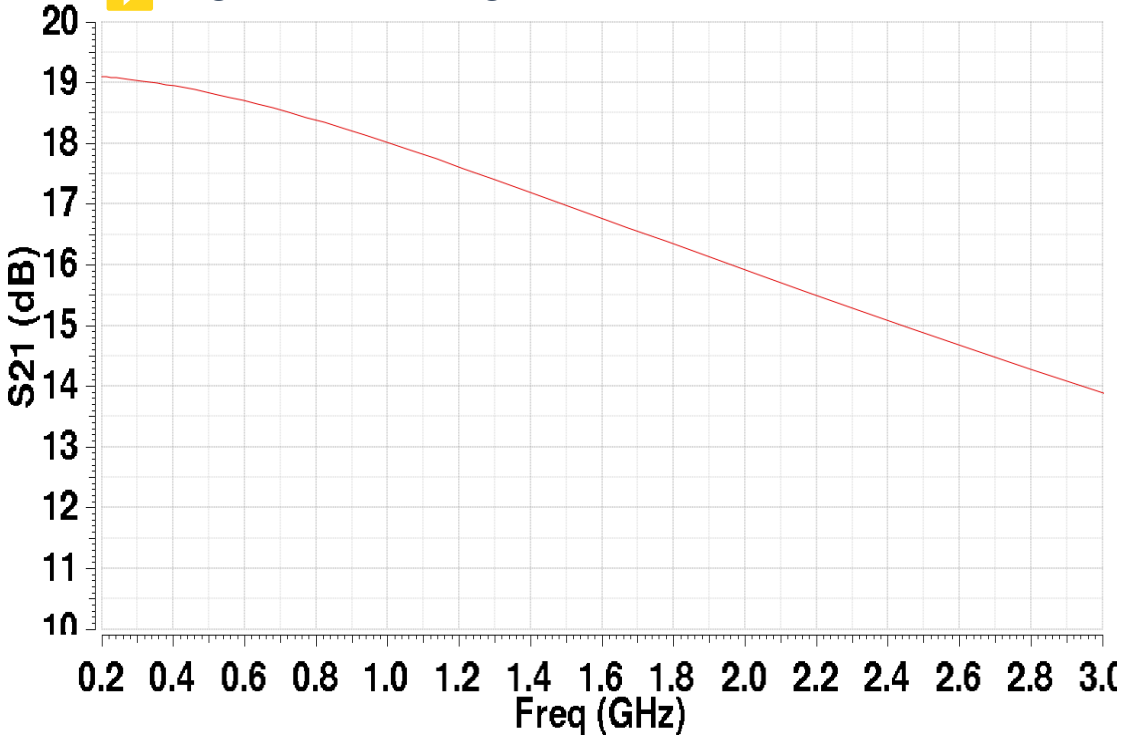


Figure 3.26 Total LNA gain without Rscs, BW=200M-1.9GHz

In addition to the condition set in [10], another balancing condition for the Balun LNA can be added by using a degeneration resistor. If the LNA is balanced, (3.105) will result in zero, meaning R_{SCS} does not need to be added.

Table 6. Comparison with the state of the art LNA

Ref	Tech (nm)	Band (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Balun
[20]* 2004	250	0.2-2.0	10-14	<2.4	0	35	NO
[21]* 2006	90	0.5-8.2	22-25	<2.6	-4/-16	42	NO
[22] 2006	90	0.8-6	18-20	<3.5	>-3.5	12.5	YES
[10]* 2008	65	0.2-5.2	13-15.6	<3.5	>0	14	YES
[23] 2009	90	0.1-1.9	20.6	<2.7	10.8	9.6	YES
[46] 2010	130	0.2-3.8	11.2	<2.8	-2.7	1.9	YES
[18] 2013	130	6-9	22	<3.2	-	5.5	YES
[28]* 2016	180	0.01-1.7	19.7	<2.8	1.13	25.2	YES
[25]* 2019	65	0.05-1	24-30	2.3-3.3	>-4	19.8	YES
[24] 2019	180	0.21-1.1	18.5-15.5	2.8-3.8	-13.4	5.58	YES
This work Without Rscs	180	0.2-1.9	19-16	<3.6	<8	12	YES
This work With Rscs	180	0.2-2.1	17.8-14.8	<3.8	<7.9	12	YES

References denoted by "" in Table 6 are measured results, other results are simulated.*

3.6 Process-Voltage-Temperature Variation with Degeneration and Voltage Source as Biasing

The PVT variations (Process-Voltage-Temperature) for the LNA with degeneration resistor are simulated in this section, where the voltage gain, voltage gain unbalance and output phase are plotted. An ideal DC block is used at the input when simulating the AC analysis, and the biasing was not changed. The fast corner was done at -40°C and +10% supply voltage (Vdd=1.98V), the typical corner was done at 27°C and +0% supply voltage (Vdd=1.8V), and the slow corner was done at 85°C and -10% supply voltage (Vdd=1.62V). The PVT has assumed the best and worst possible case scenario for the circuit, where the best case is the fast corners and worst case is the slow

corners. The gain unbalance was most obvious in figure (3.27) at the fast corners, this is due to the corners having a bigger impact on the CG than on the CS, this is a PDK property and nothing can be done about it.

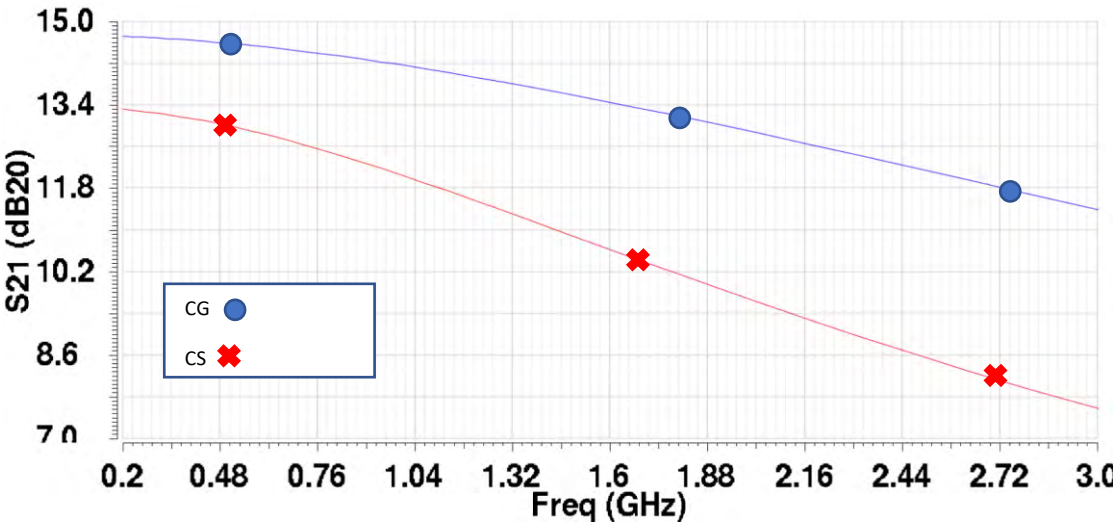


Figure 3.27 CS and CG gain at fast corners at -40°C

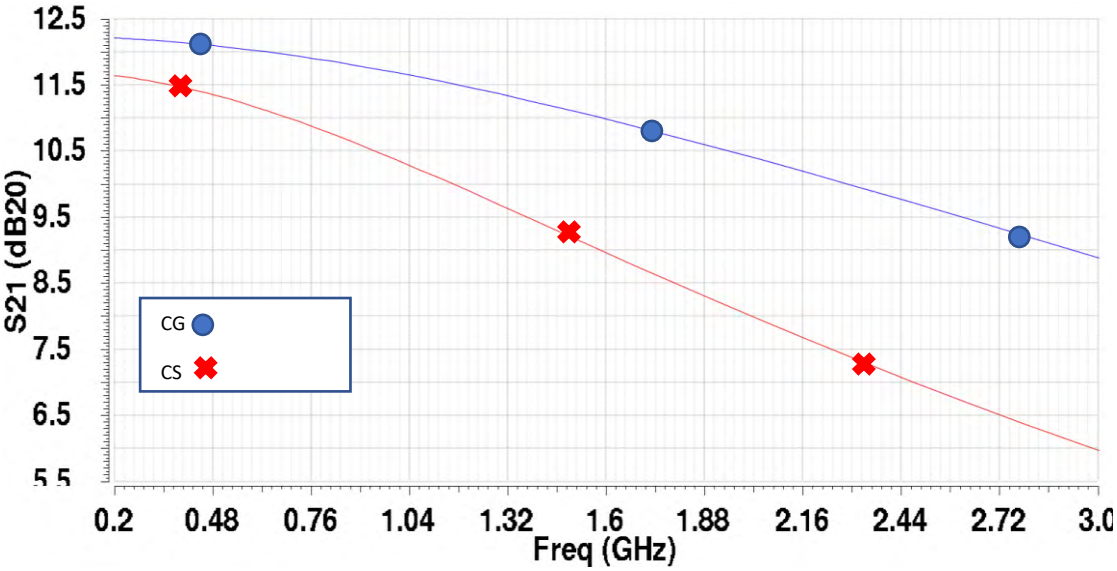


Figure 3.28 CS and CG gain at typical corners at 27°C

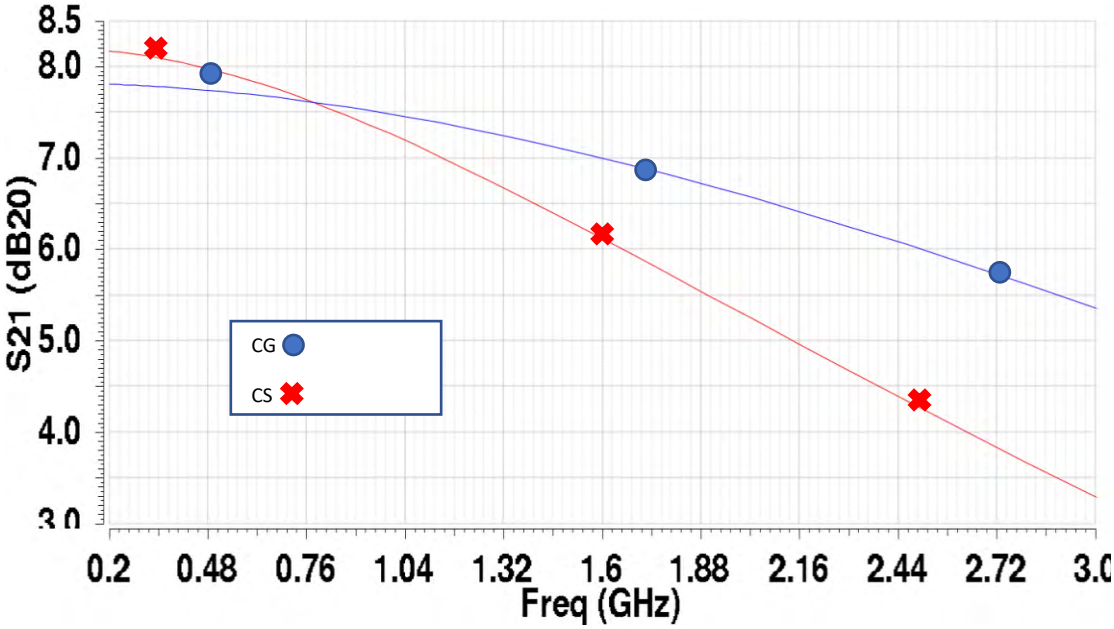


Figure 3.29 CS and CG gain at slow corners at 85°C

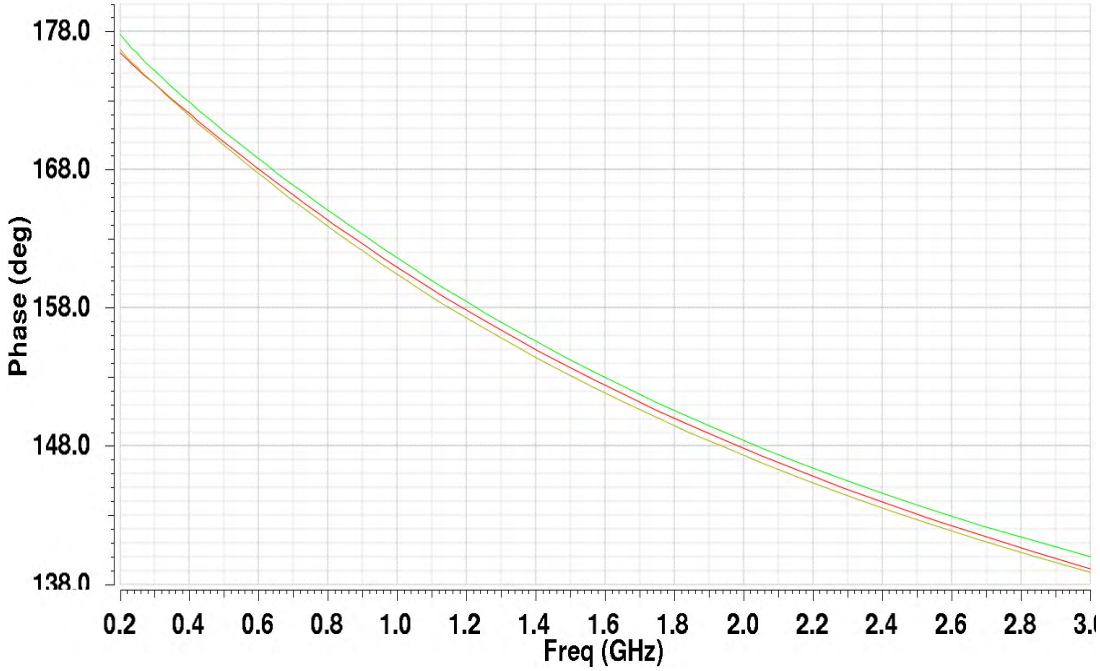


Figure 3.30 The LNA output phase at different corners, since the difference between fast and slow corner phases is only 2°, the output phase of the LNA at the three corners appear to be identical.

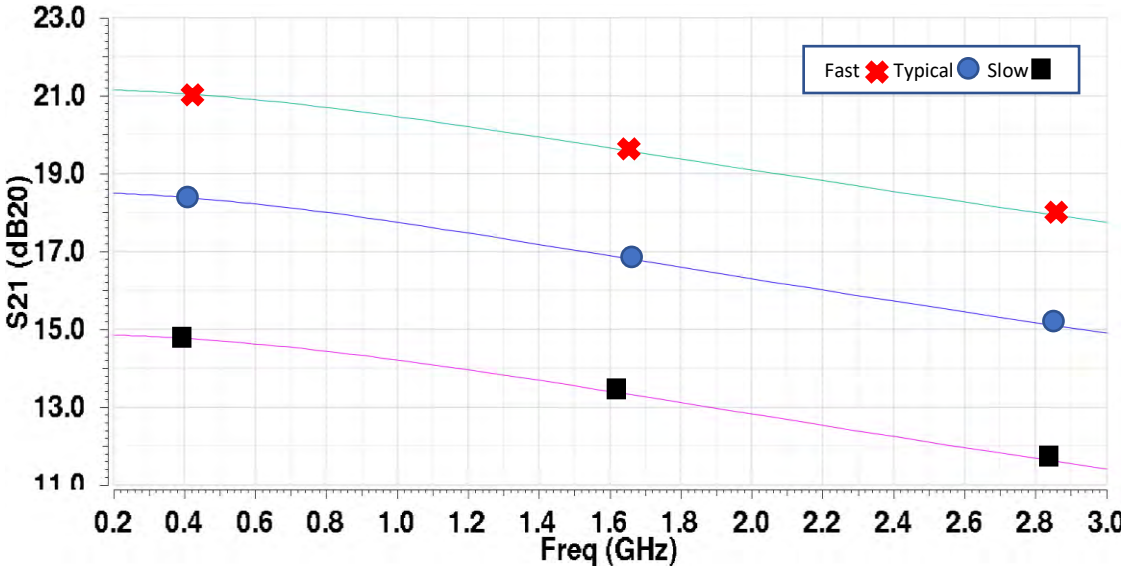


Figure 3.31 Total LNA gain at fast (-40°C), typical (27°C) and slow (85°C)

From figures (3.27-3.29), the CG has suffered the most variation due to the PVT, where the gain at 200MHz at the corners is 15.6dB at fast corners and 7.7dB at slow corner (7.9dB drop from fast to slow), while the CS is 13.4dB at fast corners and 8.2dB at slow corner (5.2dB drop from fast to slow). In figure (3.30) the different phase of the output of the LNA is plotted for the three corners, a phase difference of 2° is present between fast and slow corners, hence why figure (3.30) appears to have one plot.

3.7 Process Analysis without Degeneration and Current Mirror as Biasing.

Figure (3.32) is the Balun LNA with current mirror biasing from Cadence View. Figure (3.33) is the gain of the LNA at all possible corners and figure (3.34) is the NF of the LNA at all possible corners. As noticed in figure (3.34) the noise of the LNA before 400MHz is high, although from figure (3.33) the gain is at its highest, the LNA noise is more important than the gain and therefore the lower frequencies (<400MHz) are removed out of the operational bandwidth. The reason to start at 400MHz and not after is that there is an ISM band at 433MHz. The increase in noise at low frequency is due to the addition of flicker noise of the current mirror biasing shown in figure (3.32).

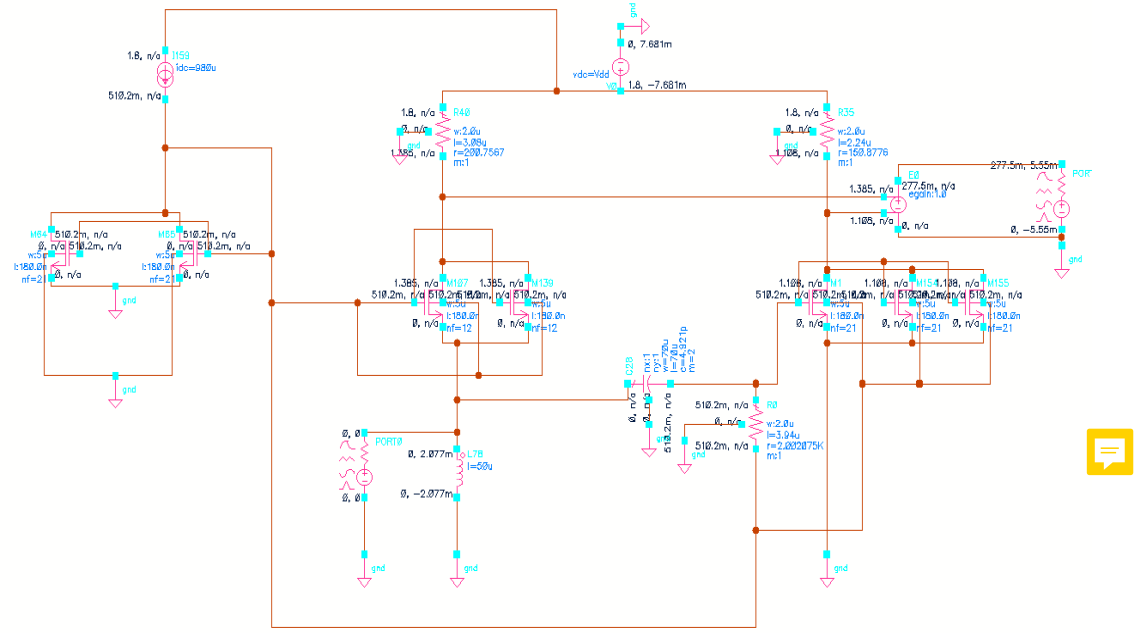


Figure 3.32 LNA schematic from Cadence (with inverted colors).

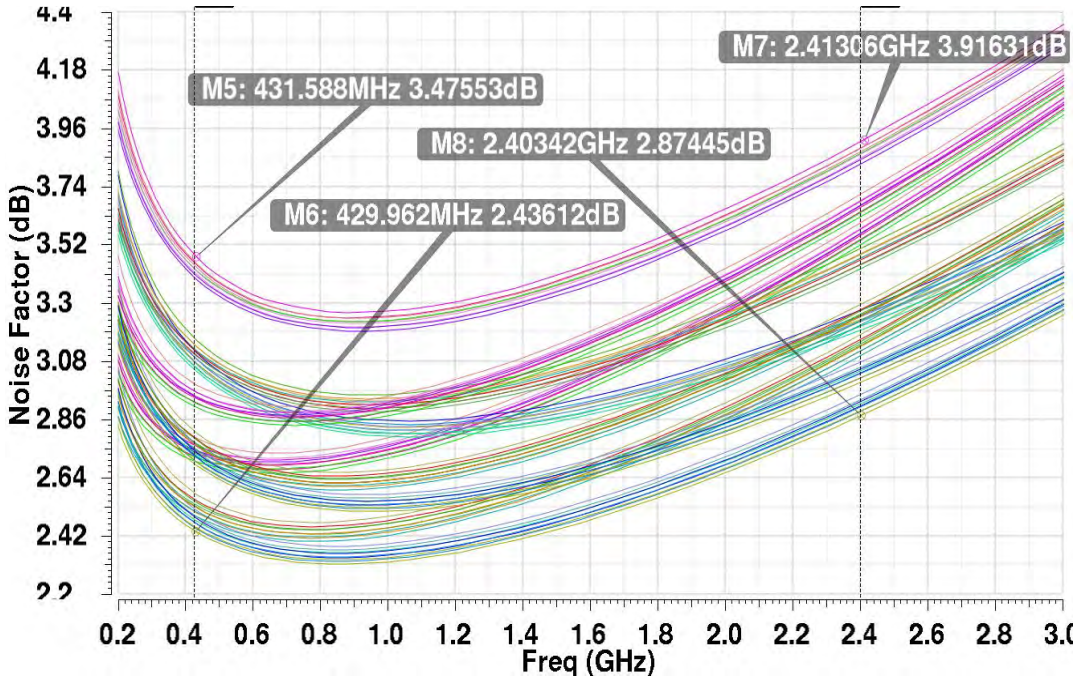


Figure 3.293 Noise of every single possible corner analysis at 27°C

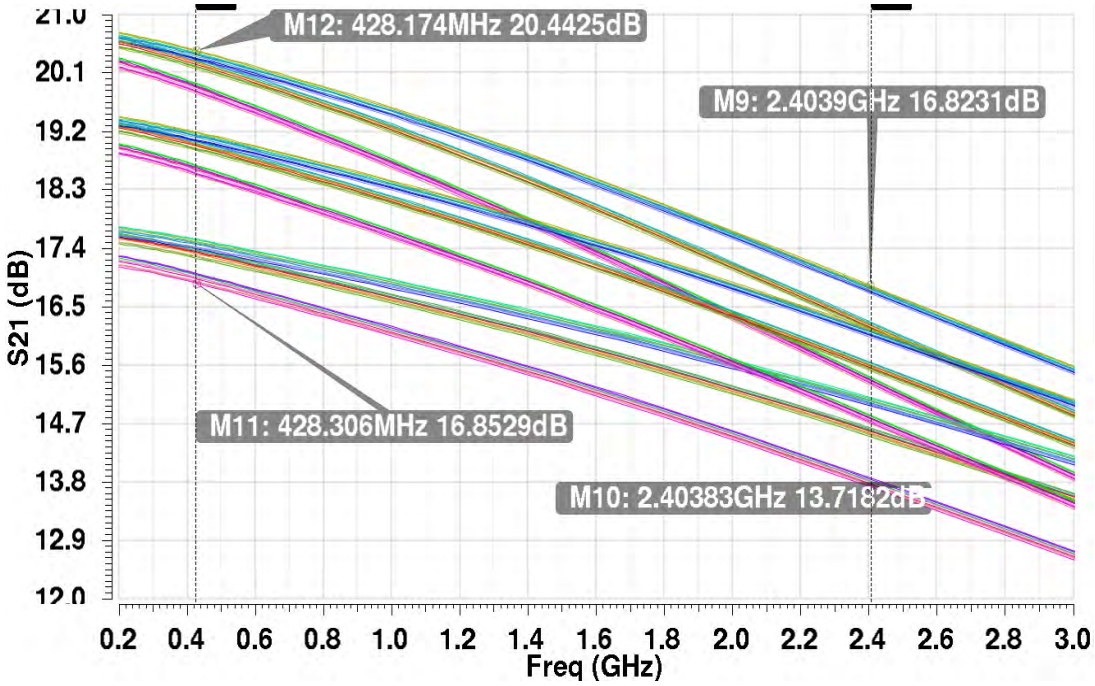


Figure 3.304 Gain of every single possible corner analysis at 27°C

Chapter 4. RF Energy Harvester

RF energy harvesting is capturing the energy available in the environment and converting it to usable electrical energy. Two types of power harvesting exist, far-field and near-field. Far-field uses electromagnetic waves, harvesting ambient RF sources such as TV signals, GSM, WIFI, and even dedicated signal. Near-field uses inductive coupling delivering electrical energy through coils tuned to resonate at the same frequency. The power delivered depends on the distance between the coils and degrades with increasing the distance between them, this limits the power transfer with distance [29]. Near-field operating range coupling is typically a few centimeters [29], while for far-field it can be few meters or kilometers depending on the harvester position and the transmitter, it also depends whether it is an intended (dedicated) or unintended (ambient) transmitter.

The bottleneck in mobile implementation is the frequent replacement of batteries used to supply the required electrical power for the circuits. Hence, ambient energy harvesting is a key technique to solve this problem by remotely providing the required power to electronic circuitry. Potential sources of ambient energy include solar, wind, light, thermal, vibration (piezoelectric), and electromagnetic waves (EM). TV, mobiles and radio broadcast all use RF signals, and since nowadays these devices are abundant in every household, so is the RF signal sent to them. An RF energy harvesting system consist of an antenna to receive the wave, matching network, RF-to-DC converter and a power management unit to store the power. RF signal, although very weak, can be captured and stored by, while efficiencies did reach 84% with 300uW harvested [30], very little amount of current is stored since a large resistive load must be used to achieve high efficiencies. After selecting the RF harvester frequency band, the rectifier is optimized at that frequency.

4.1 Controlled Energy Source

An intended/dedicated/controlled RF energy source is a dedicated transmitter that can radiate energy and transmit data. This configuration allows a power on-demand to be transmitted and captured by an RF harvester in the ISM bands, this is also known as simultaneous wireless information and power transfer (SWIPT). The transmitter is dedicated to a receiver, this allows for directed RF power flow (beamforming) which

leads to a higher power density, though it will suffer from path loses; depending on the distance; it still has higher efficiency than unintended RF energy sources [31]. SWIPT is based on the fact that any RF signal transmitting data will also have energy, if the information is of no use, then the power of the signal can be used for harvesting. According to [31], multiple input/multiple output (MIMO) SWIPT networks can yield better efficiency with multiple antennas and transmitters, since multiple antennas cause a sharper energy beam in certain direction [32]. Although multiple antennas produce higher efficiency, the cost and space required is the tradeoff.

4.2 Uncontrolled RF Energy Source

Anything that is not an intended/undedicated/uncontrolled RF energy source can be considered unintended/ambient this includes GSM, radio, Wi-Fi, etc. Any source that is not meant to be transmitted to a harvester is unintended. Unintended RF is the most prominent signal in urban areas and is constantly being transmitted, therefore capturing this energy that is rather wasted is the bases of most RF harvesters. The most important aspect of ambient RF harvesting knowing the availability and power density, this help in calculating the reliability of a device that is directly operating using the RF harvester instead of a power supply or a power management unit. Unfortunately compared to solar (100mW/cm2), thermal (60µW/cm2) and piezoelectric (200µW/cm3), the RF energy has the lowest density per unit area (0.0002-1 µW/cm2) [33].

However, RF energy is still desirable for its abundancy and other techniques either require large area, have highly variable output, are not always available or a combination of these disadvantages.

4.3 Charge Pump Rectifier

Rectifiers are devices or circuits that convert AC to DC, the signal captured by the antenna is an AC signal which needs to be converted to DC to be of use to power devices. The rectifier sometimes also boosts the voltage to achieve higher levels, hence the name charge pump rectifier (CPR). An example of a CPR is figure (4.1), it is the simplest form of rectifier made of two diodes and two capacitors. In the positive half-period of a sinusoidal signal, the diode conducts current and transfers the charge to the capacitor, which stores the charge, since the circuit has two diodes one activates at the positive half cycle and the other at the negative half cycle. All losses of the diode are

represented as V_D, which limits the output voltage and therefore the power conversion efficiency (PCE), the steady-state output of figure (4.1) is [1]:

$$V_{out} = 2V_{IN} - 2V_D \tag{4.1}$$

where V_{out} is the output voltage, V_{in} is the input peak voltage. V_D is an undesired factor that needs to be minimized for better PCE. V_D includes the turn on voltage of the diode.

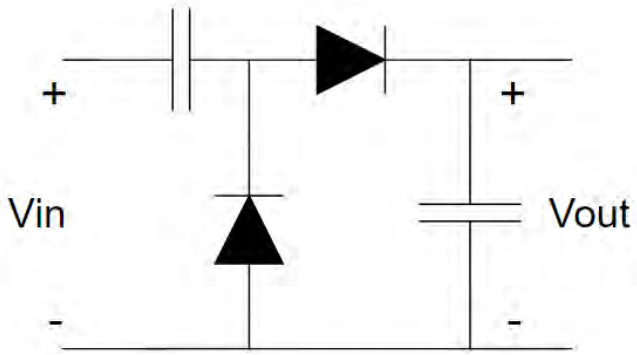


Figure 4.1 Rectifier circuit using diodes

Many techniques have been used to reduce V_D, the use of Schottky diode instead of normal diodes is one approach. A Schottky diode is a special diode built on metal-semiconductor substrate to lower V_D, the main drawback is the cost of Schottky diodes, which significantly increases the cost of CMOS circuits [1].

The replacement of diodes with diode connected MOSFETs is another technique to replace conventional diodes. MOSFETs have a voltage drop which depends on the threshold voltage (V_{TH}). In addition, the introduction of low-threshold and zero-threshold transistors makes the use of MOSFETs as diodes more appealing, UMC180nm PDK has both transistors.

Floating gate threshold voltage compensation is a simple threshold compensation techniques, rather than applying a DC voltage to the gate, a charged capacitor is connected between the gate and drain of a diode connected MOSFET, the capacitor acts as a voltage source to the gate, reducing losses since the threshold voltage needed to conduct is lowered by the capacitors voltage. However, the capacitor needs to be charged prior to installation which requires a battery, making this technique unattractive [34]. Also, if the capacitor is charged to exactly V_{TH} or more the CPR will

suffer from leakage currents, a problem also associated with zero-threshold transistors. Forward body biasing is also an available option to lower the threshold voltage which is discussed later.

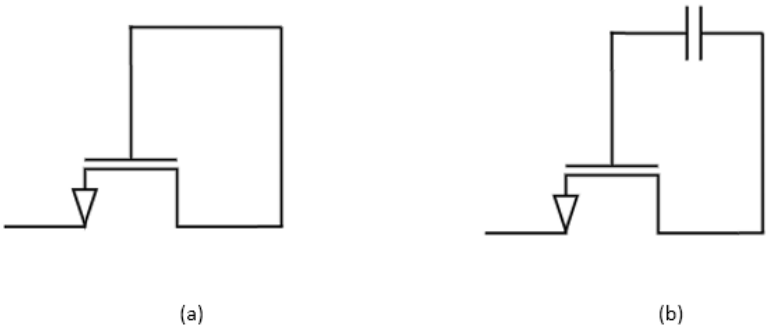


Figure 4.2 (a) Diode connected MOSFET (b) Floating gate configuration

4.4 Dickson Charge Pump

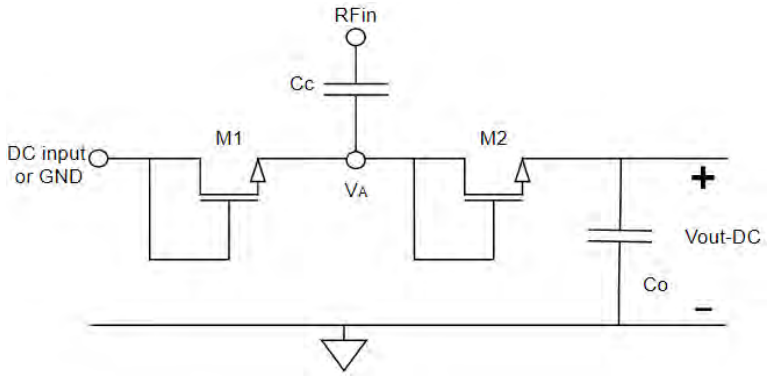


Figure 4.3 Dickson charge pump circuit

The Transistors of a Dickson charge pump will be identical. A single stage Dickson charge pump consist of two diodes connected MOSFET, a coupling capacitor (Cc) and an output capacitor (Co). The RF signal is applied at the RF_{in} terminal, rectified and stored in the output capacitor. The rectification occurs as follow [30]: During the negative half cycle ($V_{RF}<V_{TH}$) M1 turns on and Cc charges until the voltage across its terminals is equal to the amplitude of the RF input. M2 is reversed biased during the negative half cycle and is off. When the RF input is at the positive half cycle ($V_{RF}>V_{TH}$) M2 turns on and allows Co to charge from Cc and the RF input. The charged stored in Cc gets discharged into Co. At this point the voltage V_A is:

$$V_A = 2V_{RF} - V_{TH} \tag{4.2}$$

where V_{RF} is the amplitude of the input signal.

The total output voltage V_{out} is:

$$V_{out} = 2(V_{RF} - V_{TH}) \tag{4.3}$$

It is clear from (4.2) and (4.3) that the threshold voltage has a significant impact on the output voltage and is an undesired loss. The lower the threshold voltage, the higher the output voltage. However, the lower the threshold voltage, the more leakage current is presented. A zero-threshold transistor might seem to have an advantage in terms of V_{out}, but these transistor suffer from high reverse leakage current by turning on both transistors in each charging cycle [30]. Leakage current and parasitic are increased with the increase of the transistor size, large devices decrease the on resistance leading to higher output voltage, however, possess higher parasitics. Also, larger transistors can handle higher input power. Smaller devices have lower parasitics but higher on resistance, leading to lower efficiency [34]. Another important factor mentioned in [1] is that since the voltage-to-current ratio is highly non-linear, performing analytical analysis is possible, but when done so, many mathematical reduction and simplification are performed making the analysis not very accurate, here it is advised to rely on transient simulations or measurement to find the parameters of a CPR.

For multiple stages of a Dickson charge pump, the output voltage is multiplied by the number of diodes connected transistors. For M transistors, the Dickson charge pump is M/2 stages. The output voltage of N-stage rectifier is [35]:

$$V_{out} = N\left[V_p - V_{TH} - \left(\frac{15\pi}{8}\frac{I_{oeff}\sqrt{2V_p}}{\mu_n C_{ox}\left(\frac{W}{L}\right)}\right)^{\frac{2}{5}}\right] \tag{4.4}$$

where V_p is the effective peak input RF voltage, μ_n is electron mobility, C_{ox} is oxide capacitance, W is the width of the transistor, L is the length of the transistor and I_{oeff} is the effective load current. I_{oeff} is a function of leakage current and output current.

The PCE of a rectifier is defined as [36]:

$$PCE = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_{out} + NP_{SE}} \tag{4.5}$$

where P_{SE} is the power loss of the switching element in the rectifier.

From (4.5) it seems that increasing the number of stages N will increase the loss, since more stages result in more power loss, however factors such as optimizing the CPR , leakage current and the maximum power the rectifier can handle should be considered. The optimization of a CPR includes adjusting the number of stages, capacitors, load and sizing of the transistors.

4.5 Harvester Sizing and Stages Optimization.

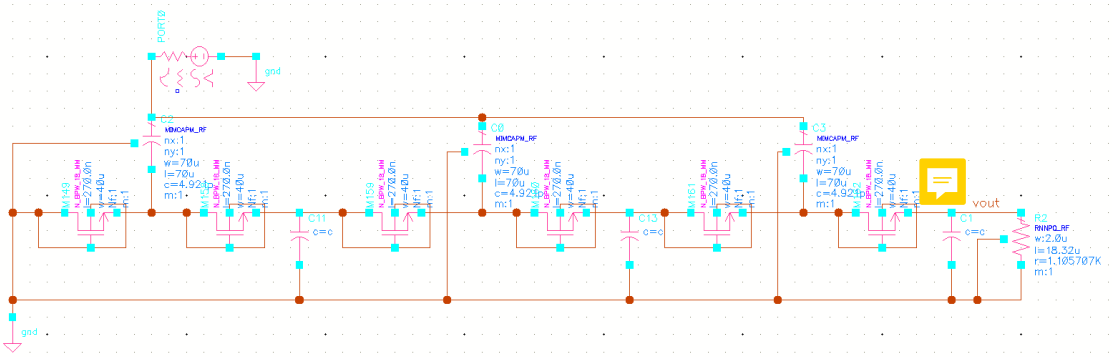


Figure 4.4 Cadence schematic image of three stage Dickson charge pump

A three stage Dickson charge pump with MOSFET connected diode is chosen for testing, as it did not encounter “imelt” issue as much as one or two stages and only needed a multiplier of 1. All the transistors in the UMC180nm PDK will be tested to ensure the most efficient transistor is picked. FBB is used in the circuit and compared with body grounded efficiency. After all the parameter values are chosen, the harvester will be directly connected to the LNA instead of a voltage supply. In each test, the minimum width and length to start the sweep was picked to avoid an “Imelt” warning from cadence. “Imelt” warning would appear when the size of the transistor is too small to handle the given input power. As the name suggest, the device is experiencing a very high current causing it to melt. The simulation will not stop, but rather cadence will linearize the result and continue the simulation, this is probably done as one might add a heat sinks to reduce the temperature and avoid this issue. All harvester testing is done at 900MHz. After sweeping width, length, number of fingers and load Table 7 is the

results of the three different transistors tested. *Since the Low threshold transistor has the highest efficiency, it is picked for the design*. After the most efficient transistor is picked, FBB will be applied to it and tested, finally the number of stages is tested.

Table 8 is the result of 1,2 and 3 stage Dickson charge pump testing. 1 stage is the most efficient, however it cannot supply enough power for the LNA, 2 stage has a lower efficiency than the 1 stage but is able to power the LNA, 3 stages handles the most input power without any errors but has the lowest efficiency. *2 stage Dickson charge pump is chosen to power the LNA.*

4.6 apacitors and FBB for the Harvester.

Different capacitors are tested for efficiency, the conclusion of this section is that the capacitors value have minor impact on the overall efficiency of the harvester, but the capacitor with the lowest value charge faster and reach steady state faster, however causes ripples which is an AC signal mixed in with the DC signal after rectification. The AC signal present is considered leakage. Figures (4.5) is three capacitor values tested and figure (4.6) is the same graph as figure (4.5) but zoomed in to show a small-time frame, figure (4.6) shows the ripples and a small overall DC shift in the signal.

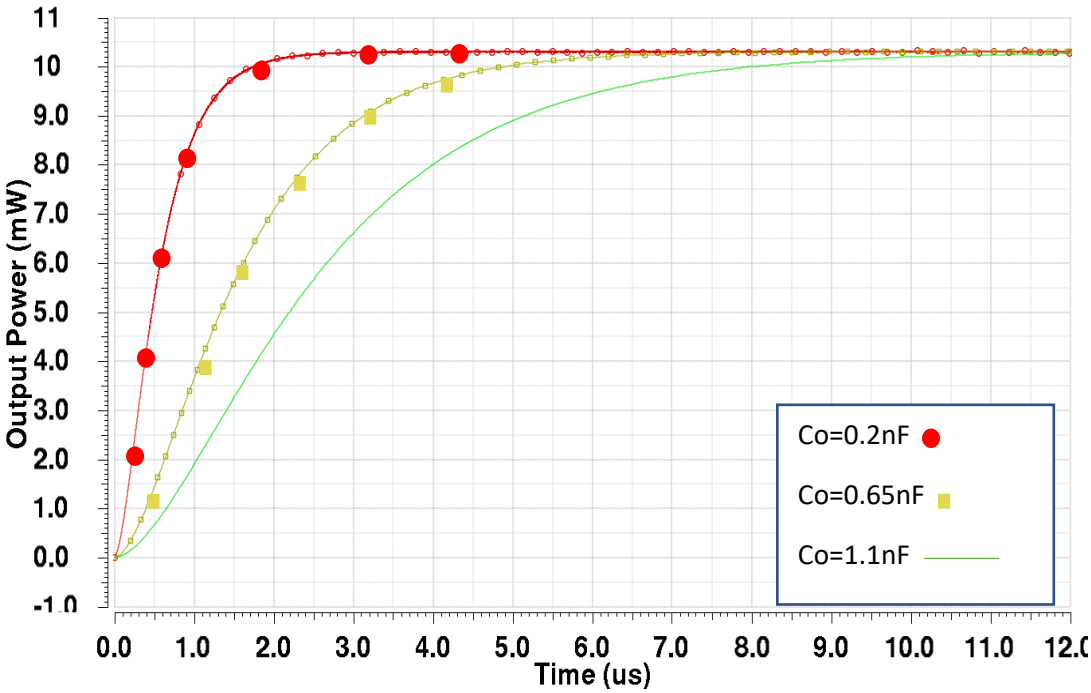


Figure 4.5 Different load capacitor value vs charge time

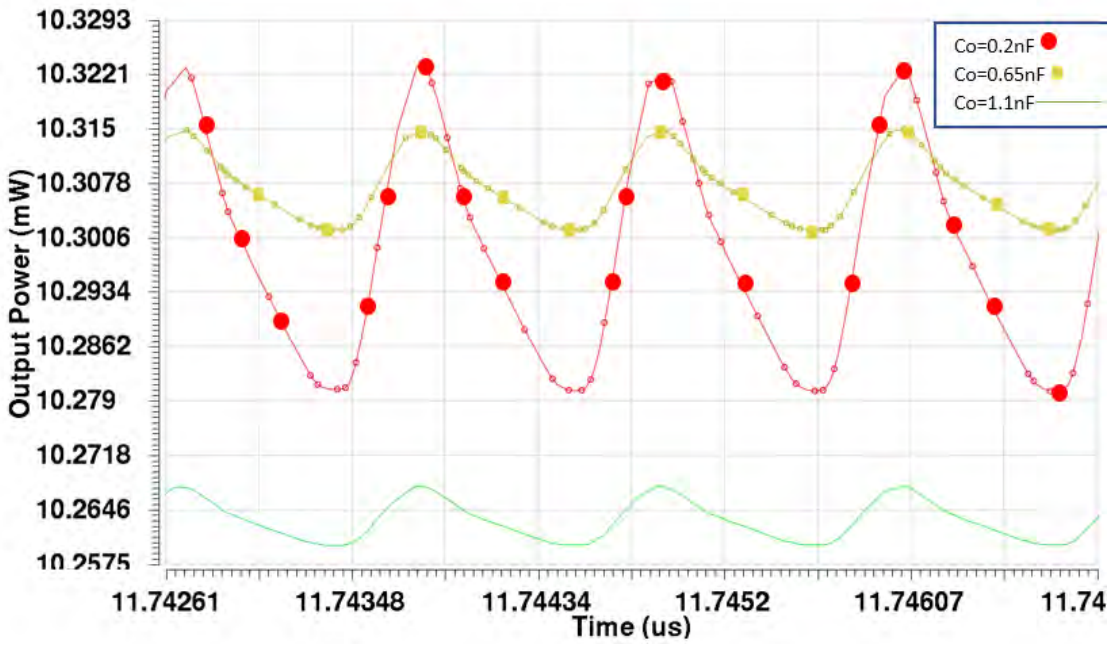


Figure 4.6 Capacitors ripple from figure (7.37)

From figure (4.5) and figure (4.6), a capacitor that charges faster, produces the most voltage swing which is considered as leakage current, if the leakage current is more important in the design then a slower charging capacitor is preferred and if speed is important then a faster charging capacitor is needed.

As for the FBB, figure (4.7) is the low threshold transistor output power with and without FBB, an increase of 9% in efficiency is noticed with FBB. Since the FBB reduces the threshold voltage, it is expected to increase efficiency, however the increase in efficiency of 9% might not justify the extra cost or complexity of the circuit specifically in the layout stage.

Table 8 summarizes all the harvester testing of the three viable transistors, after the most efficient transistor is picked, the effect of FBB is studied on it. The tables values are all simulated in Cadence after sweeping for the most optimum point. All have the same input power to have a fair comparison, the transistors are optimized for this arbitrary input power. Although the triple well had the least efficiency, it is the smallest size and can be used for higher power input harvesters. The zero-threshold and the low-threshold transistor were very close in efficiency, but the zero-threshold suffers from higher leakages. And since it is already zero-threshold, applying FBB on it will have no benefit, as the lowest threshold possible is zero.

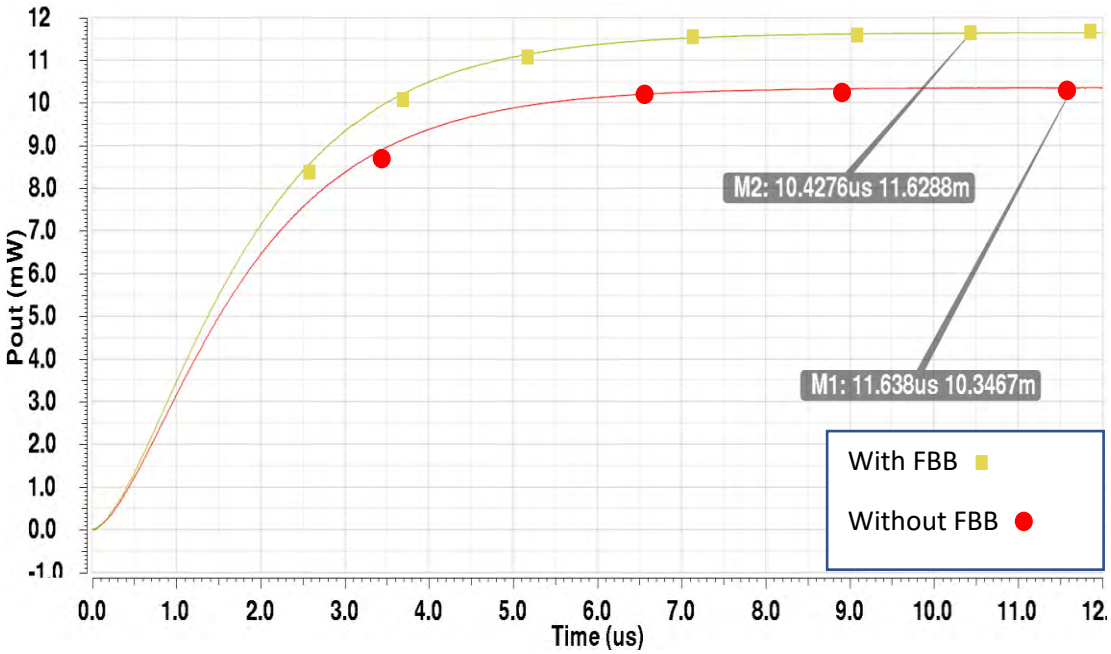


Figure 4.7 Low threshold transistor with FBB and without FBB. An efficiency increase is noticed with FBB.

Table 7. Zero threshold, Triple well and Low threshold transistors comparison

	Zero V_{th}	**Triple Well**	**Low V_{th}**	**Low V_{th} with FBB**
Optimum Width (um)	120	53	200	200
Optimum length (nm)	611	180	240	240
Optimum Load Resistance (k-ohms)	1.5	1.4	1.7	1.7
Optimum Fingers	4	1	400	400
Input Power (mW)	15	15	15	15
Output Power (mW)	10.1	6.7	10.33	11.63
Efficiency (%)	67.3	44.6	68.8	77.5

4.7 Harvester number of stages

For the number of stages testing, since the low threshold transistor is the most efficient, it is the only one tested. The load is constant because the LNA is the load from this point onwards. The LNA needs a Vdd of 1.8V and current of 6.6mA. The maximum input power will be 1dBm less than whichever input power gave an "Imelt" error, if "Imelt" error happens at 12dBm, the maximum input power will be chosen to be 11dBm, this is done to ease the selection of maximum input power. All testing was done at 900MHz. a lower frequency will result in higher efficiency, but 900MHz is the GSM frequency, the most abundant and reliable source to harvest.

4.7.1 One stage CPR testing:

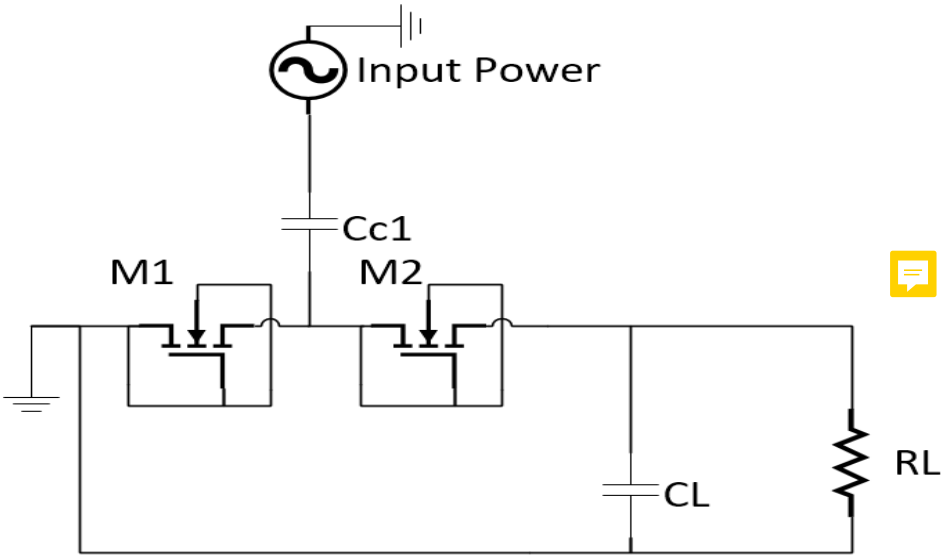


Figure 4.8 1-stage Dickson charge pump.

The problem with the one stage that occurred is the amount of input power the transistors can handle is 12dBm, although the efficiency was 48% (which is the highest), only 5.5mA of current and 1.38V was possible to achieve, which is not enough to power the LNA. Figure (4.9) is the one stage CPR output vs time (transient response), summary of all the values are in Table 8.

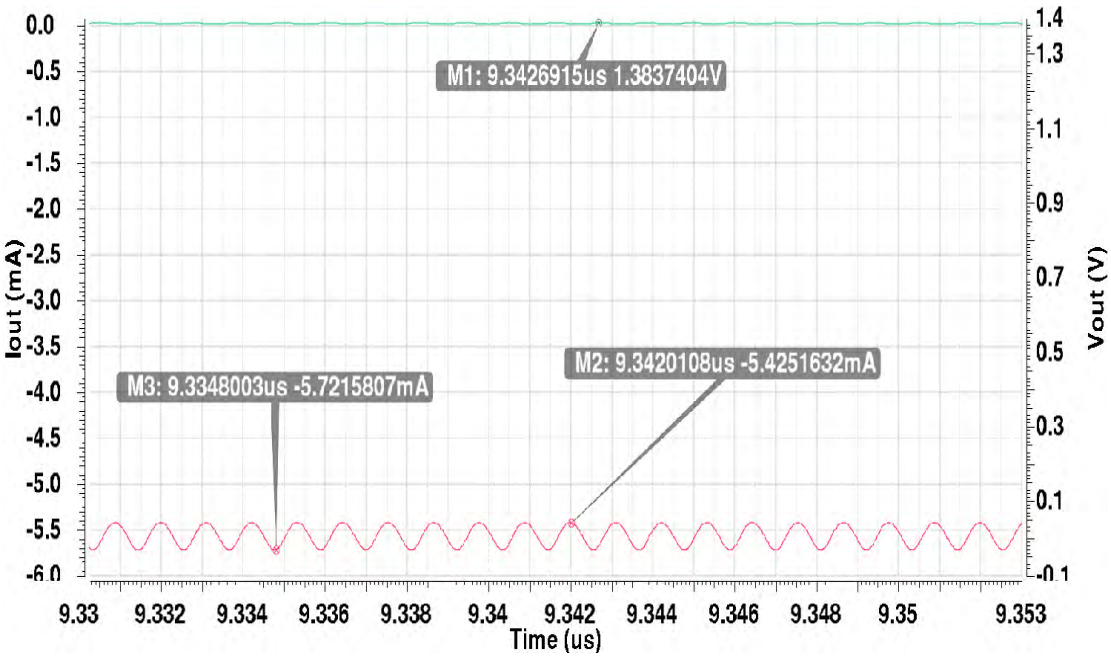


Figure 4.9 One stage harvester output with input of 15mW @900MHz

4.7.2 Two stage CPR testing:

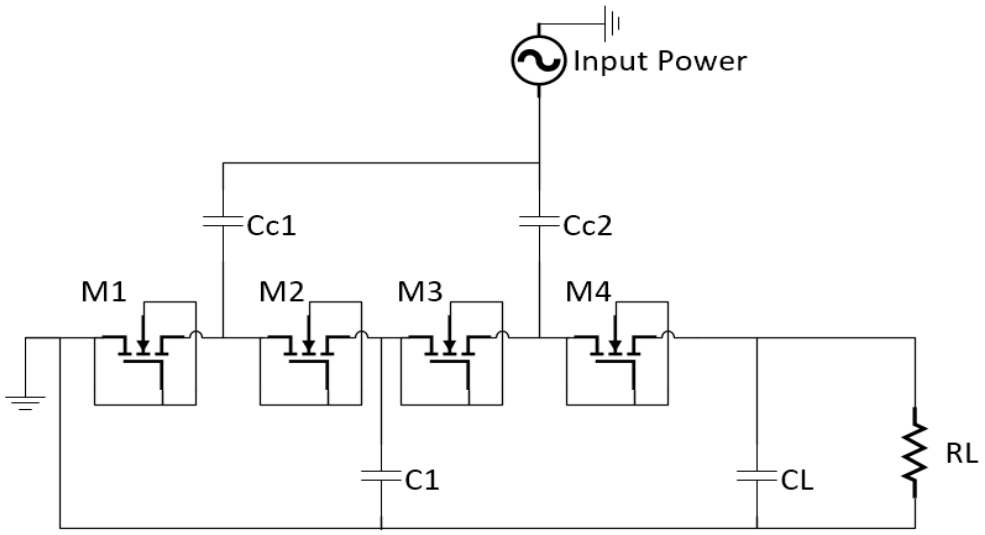


Figure 4.10 2-stage Dickson charge pump.

The two stage CPR achieved an efficiency of 40% with a maximum input power of 17dBm, an 8.5mA of current and 2.4V. Figure (4.11) is the two stage CPR output vs time (transient response), summary of all the values are in Table 8.

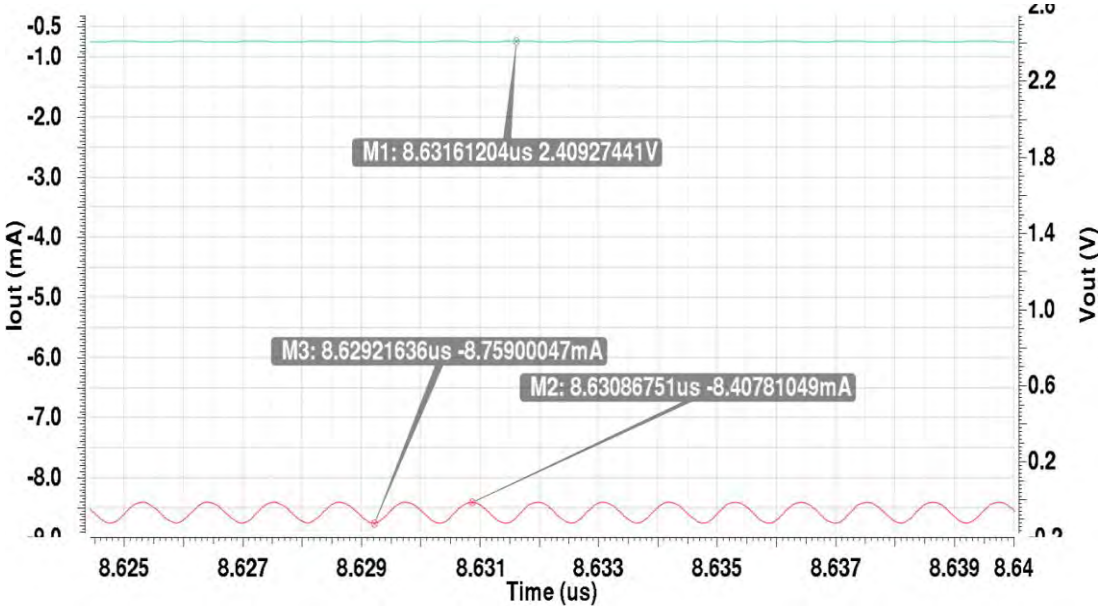


Figure 4.11 Two stage harvester output with input of 50mW @900MHz

4.7.3 Three stage CPR testing:

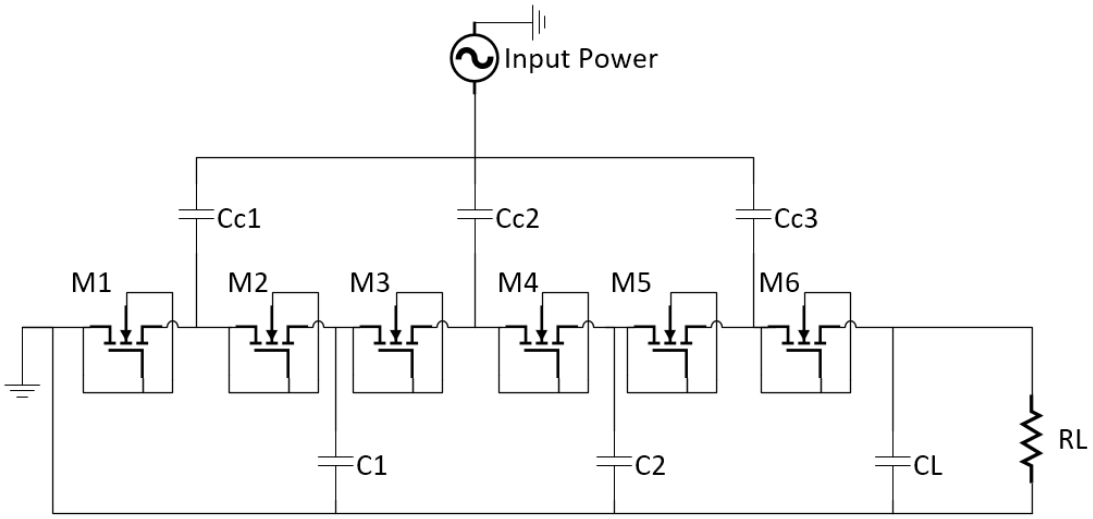


Figure 4.12 3-stage Dickson charge pump.

The three stage CPR achieved an efficiency of 28% with a maximum input power of 21dBm, an 11.1mA of current and 3.14V was possible to achieve. Since the 2 stage was able to supply the needed current and voltage, the 3 stage is only tested to check if the efficiency is higher or lower than the two stage. Figure (4.13) is the three stage CPR output vs time (transient response), summary of all the values are in Table 8.

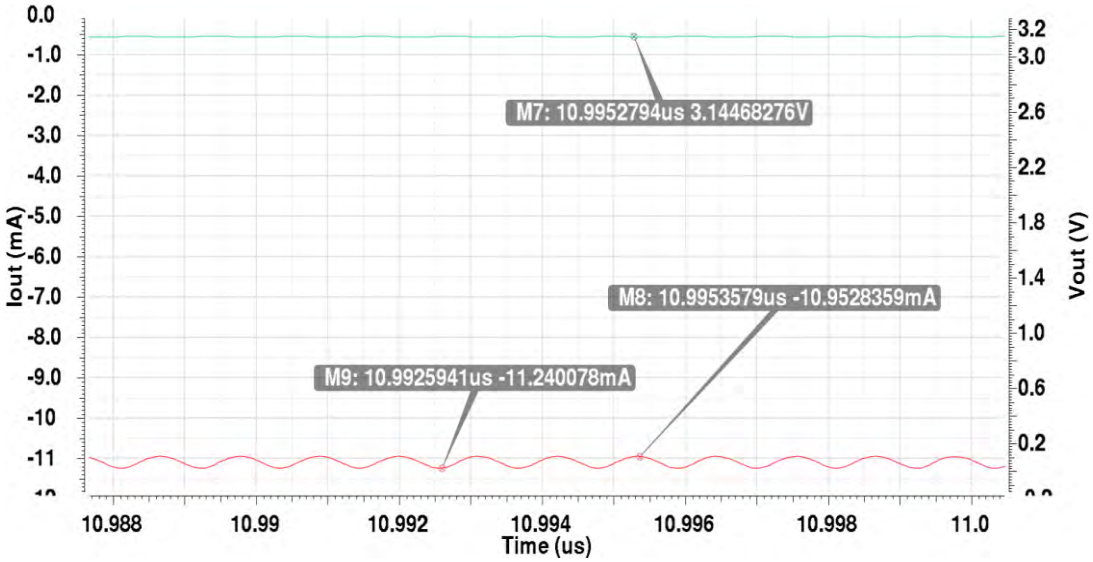


Figure 4.13 Three stage harvester output with input of 126mW @900MHz

Table 8. LNA and different stages of harvester power and efficiency

Low V_{th} with LNA as Load			
	1 Stage	**2 Stage**	**3 Stage**
Maximum Input Power (mW)	15.8	50.1	125.9
Maximum Output Voltage (V)	1.38	2.41	3.14
Maximum Output Current (mA)	-5.7	-8.75	-11.24
Maximum Output Power (mW)	7.88	21.1	35.3
Efficiency (%)	49.8	42.1	28.0
Viable	NO	YES	YES

The reason for the negative current is that the current is leaving the measuring node and not entering. It is kept negative as to be consistent with the figures.

Table 8 maximum input power is the power 1dBm less than whatever input power gives "Imelt" error, maximum output voltage and current is the output at the given maximum input power, maximum input power is the product of maximum voltage and current, efficiency is maximum output power divided by maximum input power, "Viable" is whether the given stage can power the Balun LNA given in chapter 3.

Chapter 5. LNA and Harvester Integration and Results

After connecting the LNA as a load to the harvester, the efficiency dropped since the load of the harvester is not the optimum load from the simulation. Two stage CPR was used as it can deliver the needed current and voltage for the LNA with an input power of 15dBm, a maximum input power of 17dBm is to account for track loses and other non-idealities. ***An independent power supply will be used for the biasing circuit and its power consumption will not be accounted for in efficiency calculations.***

5.1 Harvester Output Voltage, Current and Power

Figure (5.1) is the full circuit on Cadence, with all the components and biasing shown. Figure (5.2) is an extension of the highlighted area from figure (5.1) where the smoothing capacitor and measuring resistors are shown. Figure (5.3) is the simplified schematic using Visio, where only the core components are shown.

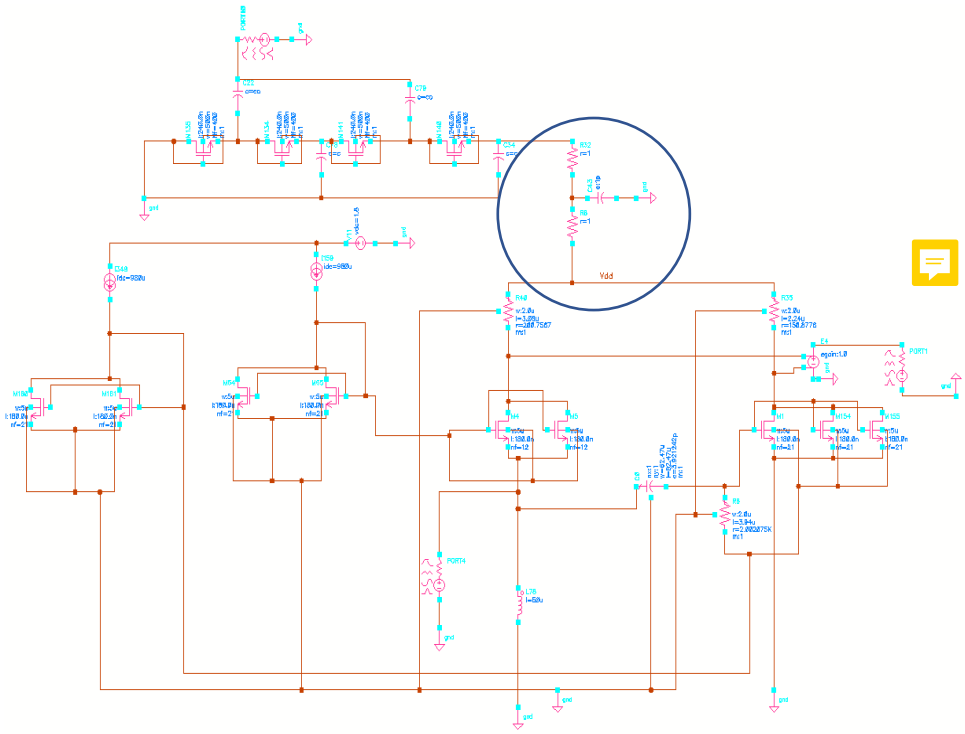


Figure 5.1 Full schematics of LNA and the harvester from Cadence view.

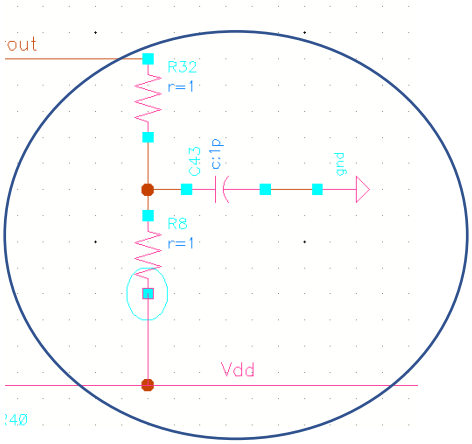


Figure 5.2 The two resistors are 1-Ohms each and only used to measure current. The capacitor is the smoothing capacitor

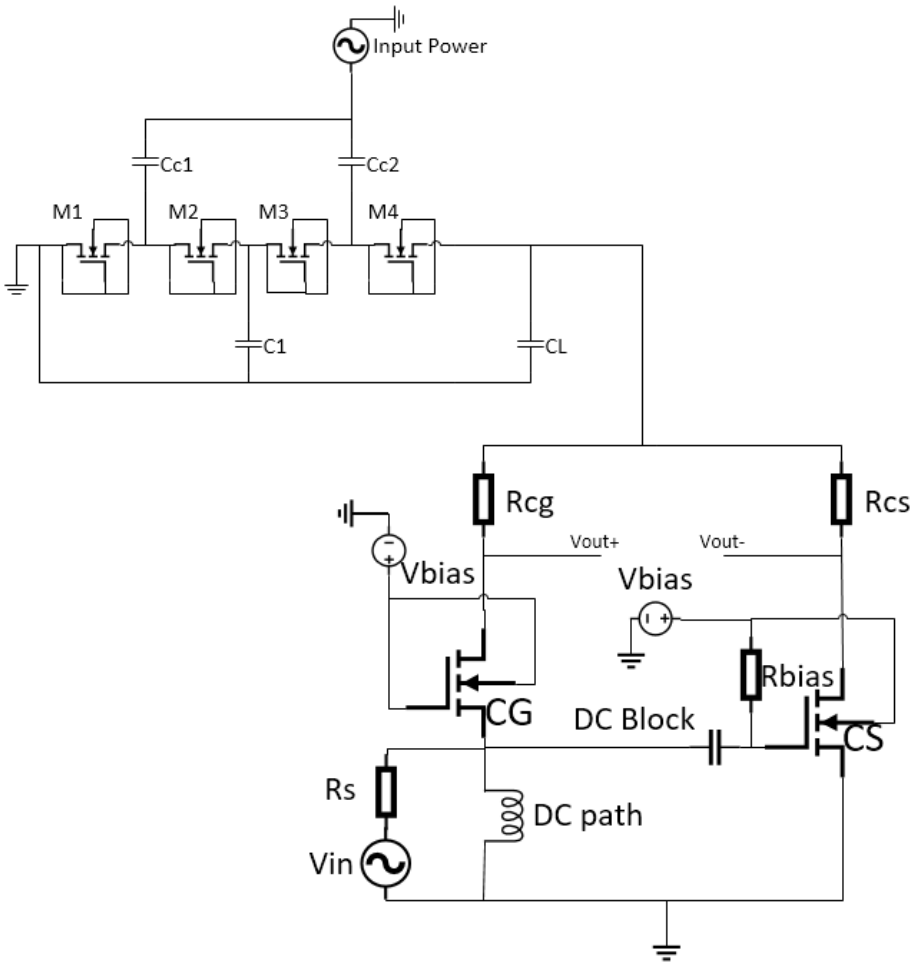


Figure 5.3 Simplified schematics of LNA and harvester using Visio.

Figure (5.4) is the output current before and after the addition of the smoothing capacitor from figure (5.2), a reduction in swing is noticed at the same frequency. The reduction in swing is needed to have a smoother DC input to the LNA, making it more robust. Figure (5.5) is the final output of the harvester and the input power to the LNA.

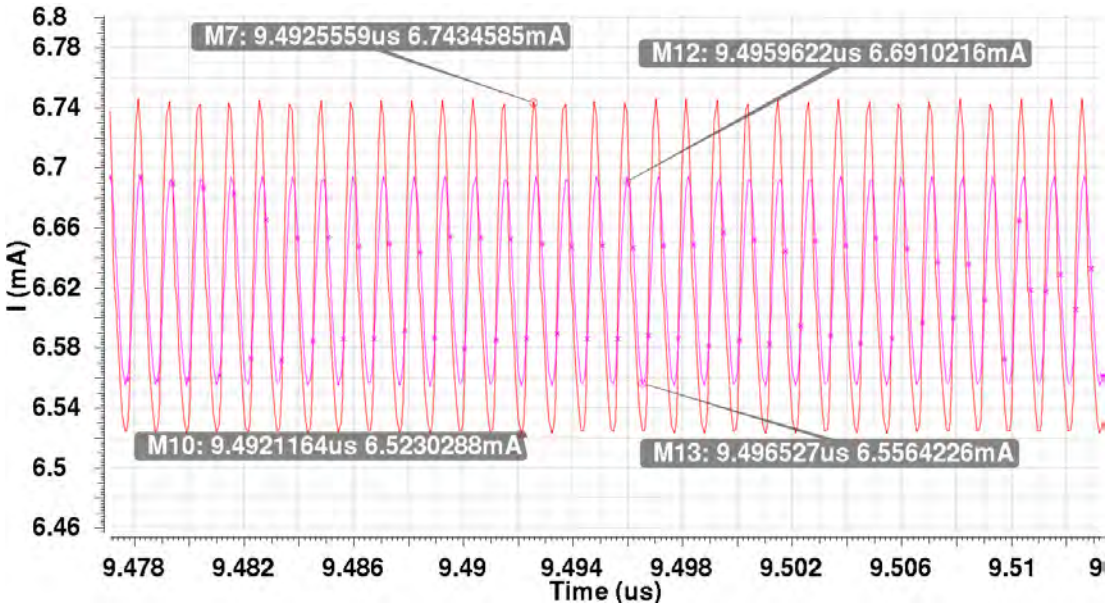


Figure 5.4 Output current before and after the addition of the smoothing capacitor, a reduction in output swing is noticed.

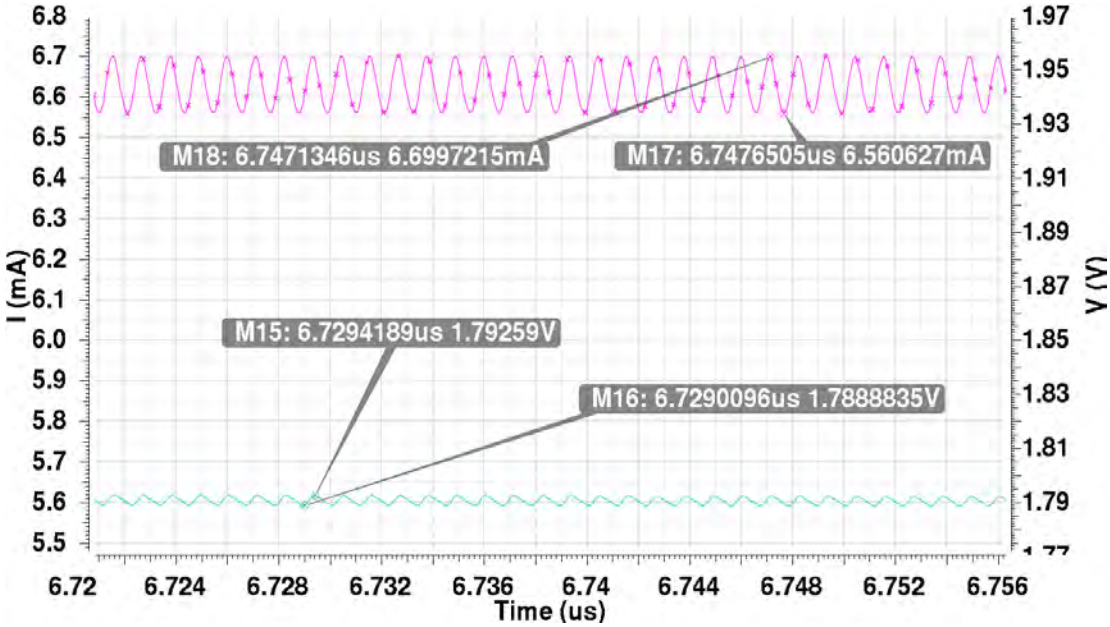


Figure 5.5 Final output of the harvester, the swing is due to non-ideality of the rectification stage.

The power spectrum of the signal can be measured using the spectrum function. Using this function plots the harmonics vs frequency, this is used to measure the power of the DC and all leakages. One thing to note is the spectrum function takes $20 * \log X$, so to find the power spectrum the power function needs to be sent to the calculator and the square root of the power sent to the spectrum function.

Figure (5.6) to (5.11) are the voltage, current and power spectrum, they are used to measure the V_{dd}, I and power of the harvester after rectification showing the zero-frequency value and the harmonics power. All harmonics are due to the leakages (sinusoidal after rectification) due to non-idealities in the transistors, it is impossible to have a 100% pure DC signal and such leakages are to be expected. Figures (5.6), (5.8) and (5.10) are in dB, making it easier to see the harmonics. Figures (5.7), (5.9), (5.11) are in volts, amps and watts respectively, to have an easier value to read and avoid conversion. The harmonics produced are all at least 40 dB less than the wanted signal (the DC signal), meaning the harvester has converted most of the power into DC.

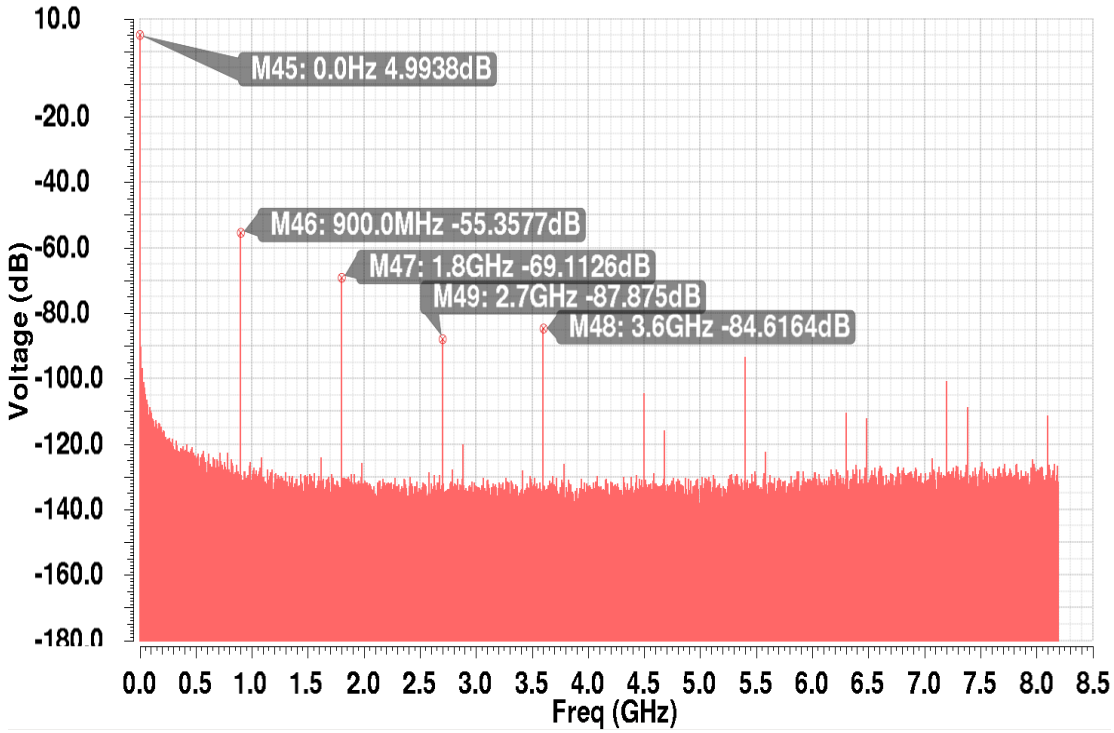


Figure 5.6 Output voltage harmonics in dB.

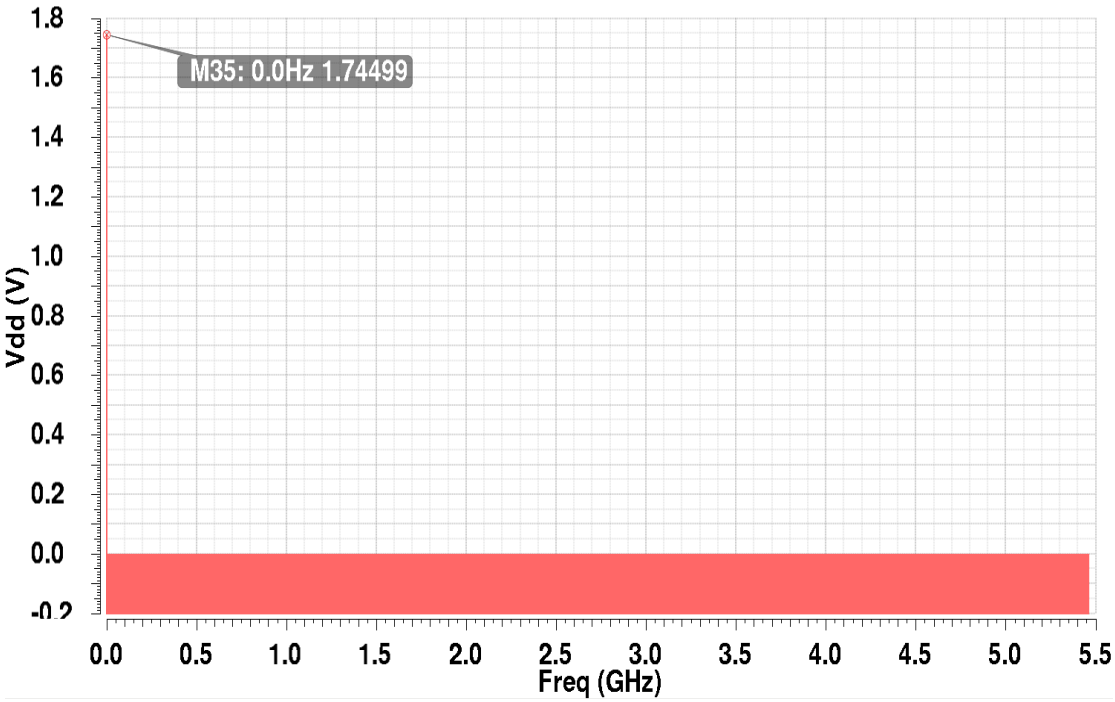


Figure 5.7 Output voltage harmonics in volts.

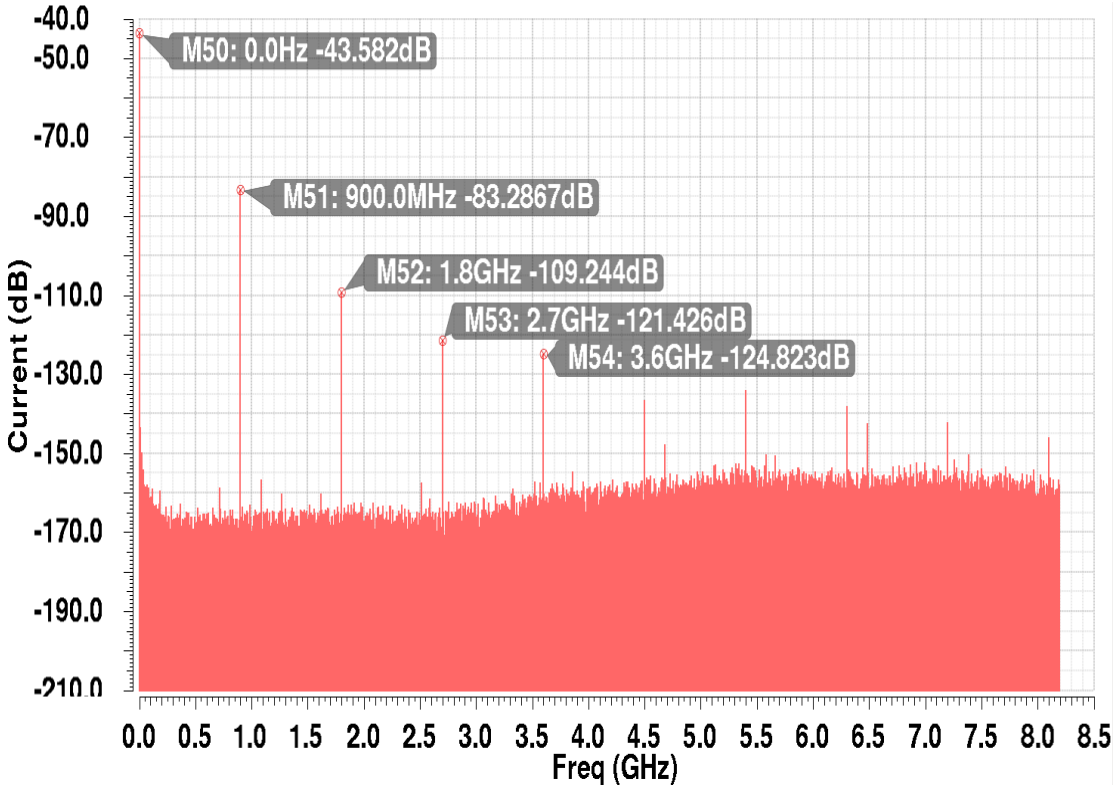


Figure 5.8 Output current harmonics in dB.

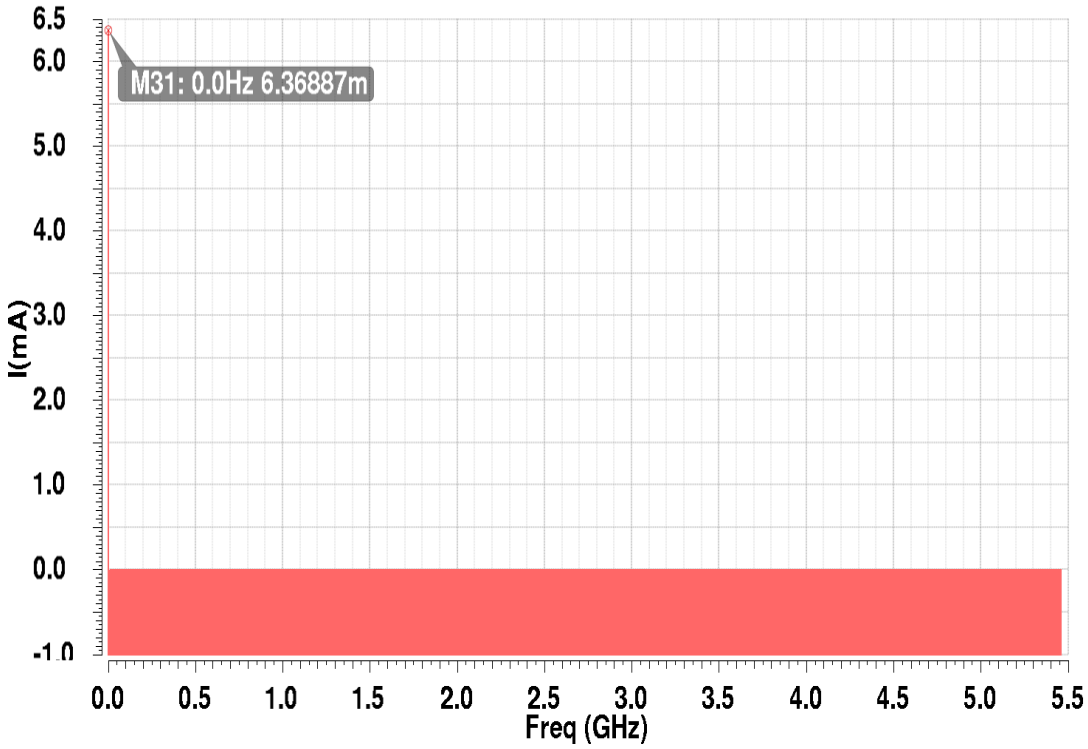


Figure 5.9 Output current harmonics in mA.

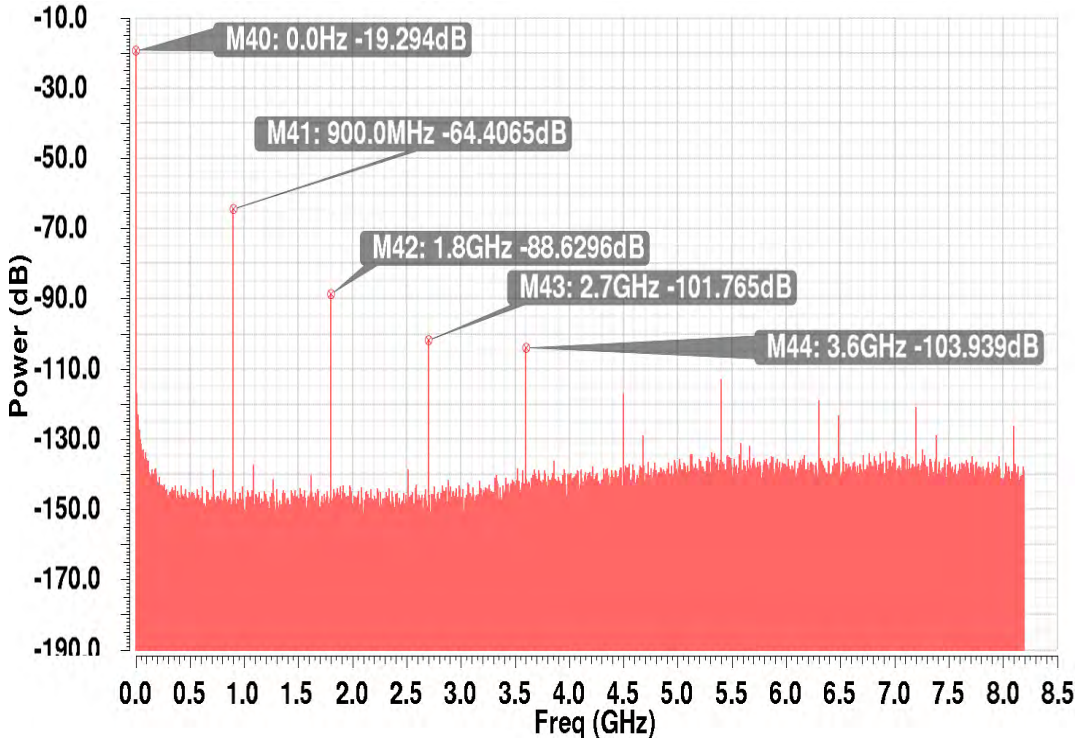


Figure 5.10 Output power harmonics in dB.

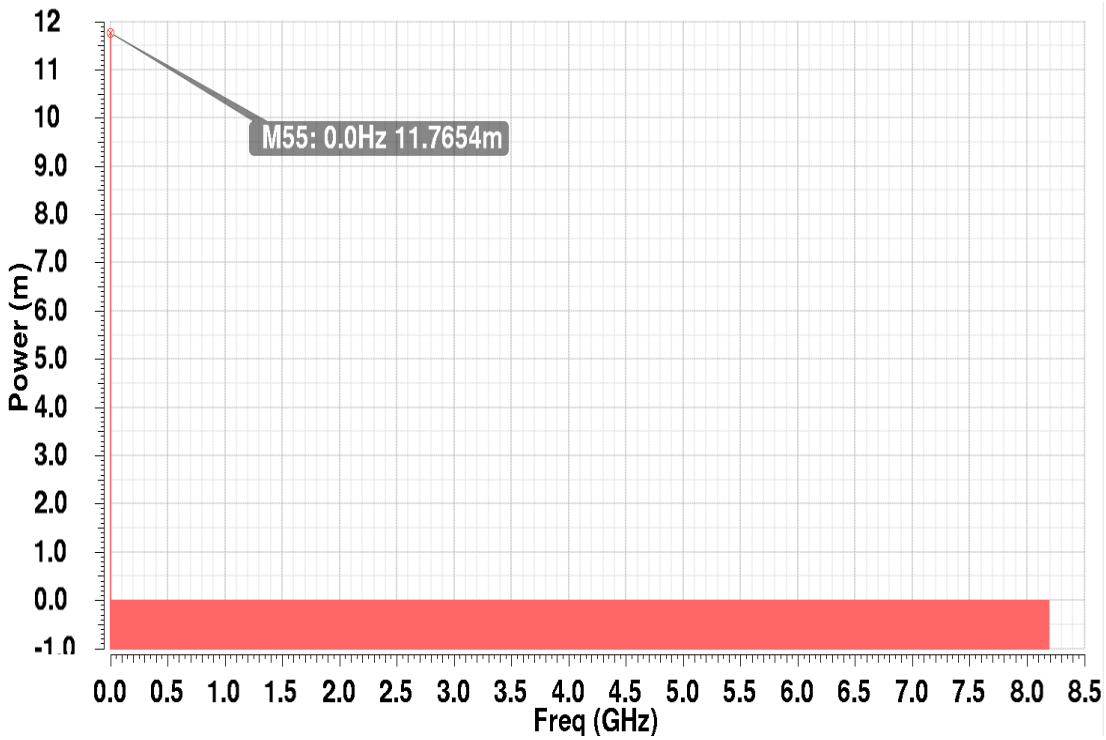


Figure 5.11 Output power harmonics in mW.

5.2 LNA Simulation

Due to the harvester needing time to fully settle (8us) most simulation on cadence such as “dc” cannot be done, meaning “dc print” option is not available, therefore finding the transconductance of the device is done manually. Also, “sp” simulation can be used after adding settling time, the main simulation used with the harvester is the periodic steady state “pss” as it allows for stabilization time in cadence. The DC values themselves cannot be evaluated. The DC simulation will take the zero-time values, making the output voltage and current either zero or an error message.

The value 508.3u from figure (5.12) is the zero-time value of the simulation, since the harvester did not reach the steady state this value is of no meaning. Figure (5.13) is where the “DC” simulation at zero second value is taken.

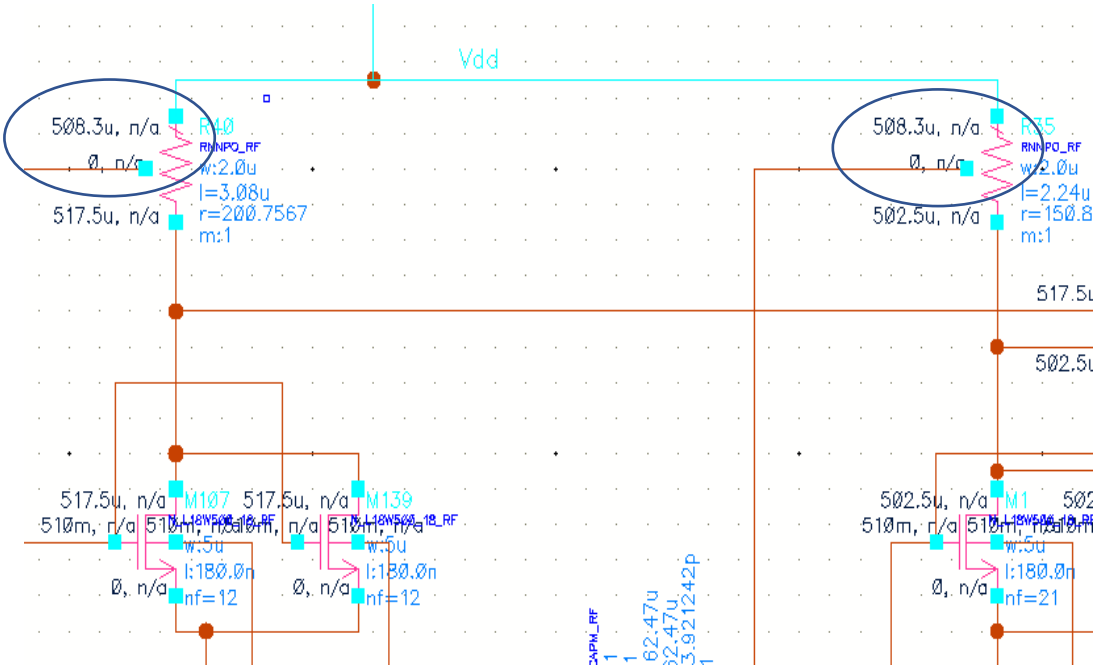


Figure 5.12 The "DC annotate" values in the Cadence schematic window.

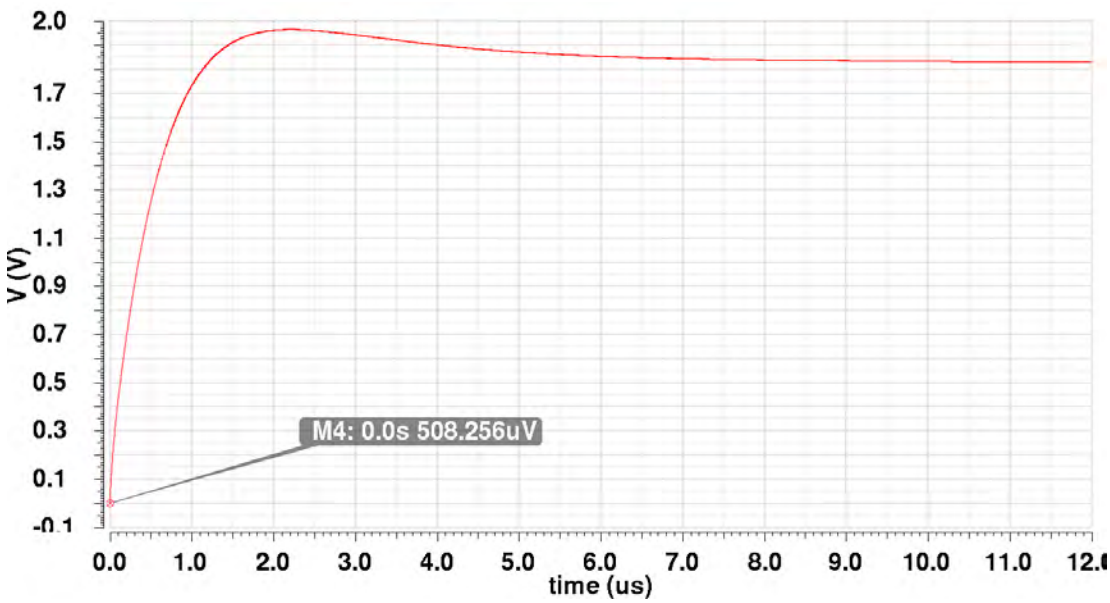


Figure 5.13 The value of the "DC" simulation is the zero second value.

**Finding the gain of the LNA with the harvester is done using transient, nothing extra needs to be simulated.*

Figure (5.14) is the output of the CG and CS at 900MHz. Figure (5.15) is the total gain of the LNA at 900MHz, the DC shift is reduced since the output is the

difference of each side and not the addition. A DC block capacitor at the output will remove the DC shift, this might be needed if this DC shift will saturate the next stage.

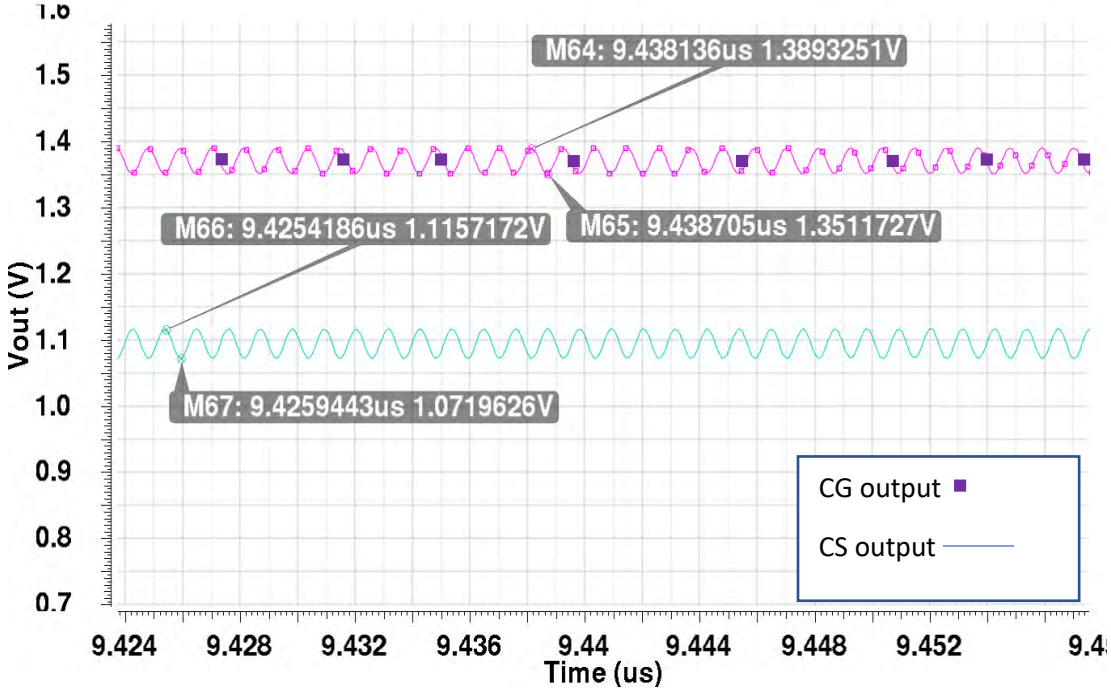


Figure 5.14 CG and CS output with an input of 10mV @900MHz. "Transient" simulation is used. CG gain=11.63dBV, CS gain = 12.8dBV.

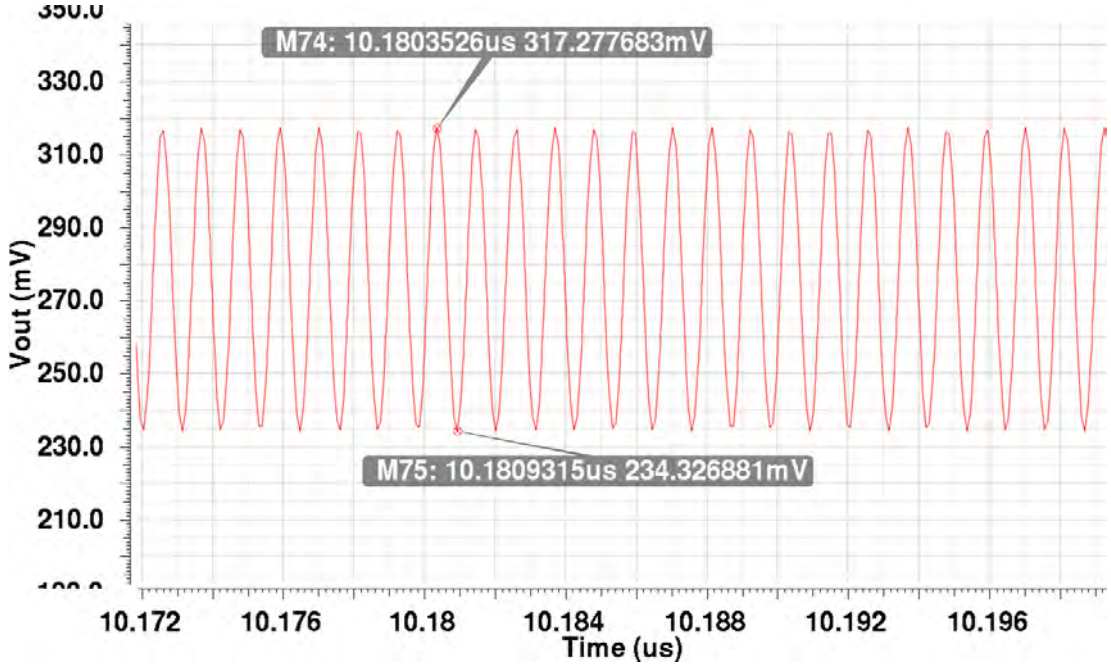


Figure 5.15 LNA total gain = 18.38dBV @900MHz

Figure (5.16) is the output of the CG and CS at 400MHz. Figure (5.17) is the total gain of the LNA at 400MHz, the DC shift is reduced since the output is the difference of each side and not the addition. A DC block capacitor at the output will remove the DC shift, this might be needed if this DC shift will saturate the next stage.

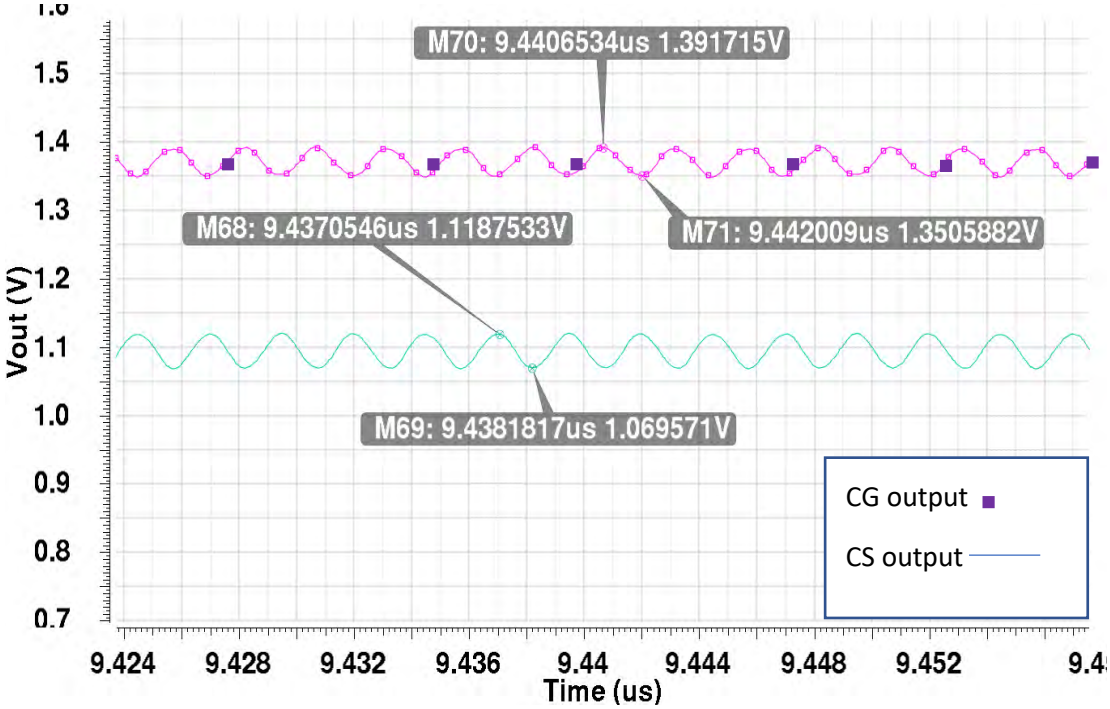


Figure 5.16 CG and CS output with an input of 10mV @400MHz. "Transient" simulation is used. CG gain=12.28dBV, CS gain = 13.84dBV.

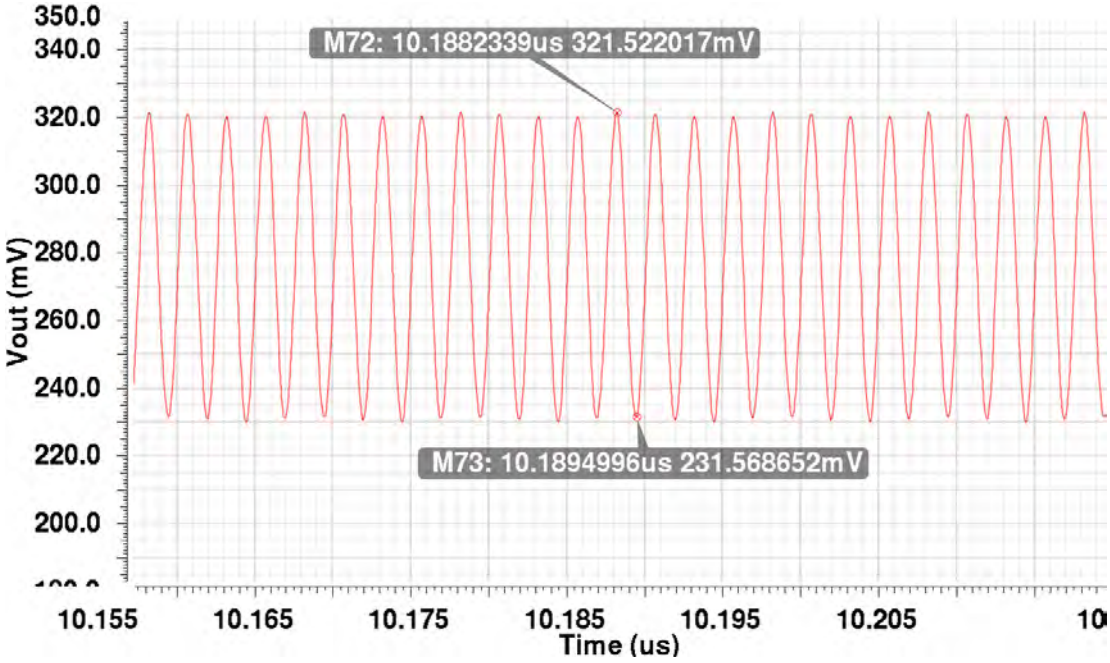


Figure 5.17 LNA total gain = 19.08dBV @400MHz

Figure (5.18) is the output of the LNA at 2.4GHz. Figure (5.19) is the total gain of the LNA at 2.2GHz, the DC shift is reduced since the output is the difference of each side and not the addition. A DC block capacitor at the output will remove the DC shift, this might be needed if this DC shift will saturate the next stage.

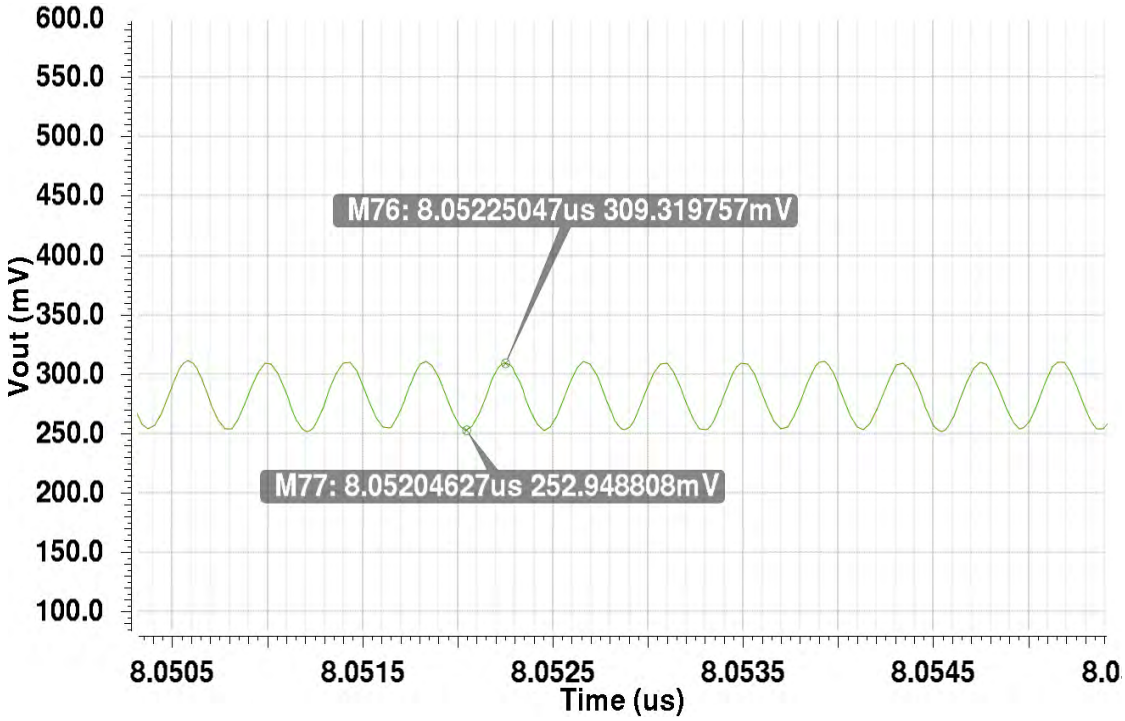


Figure 5.18 LNA total gain = 15.02dBV @2.4GHz

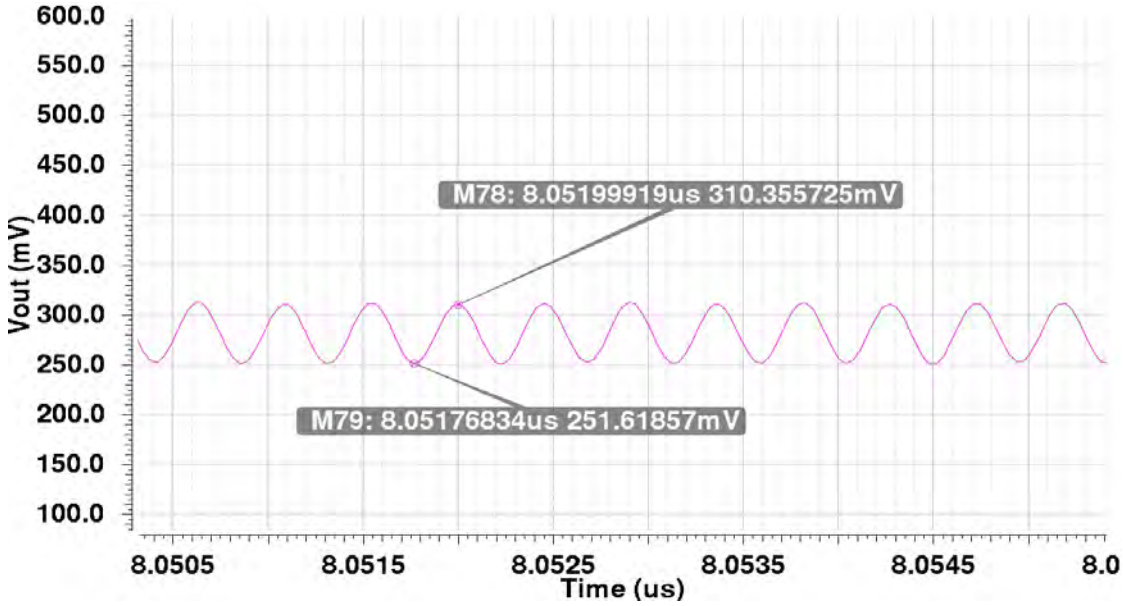


Figure 5.19 LNA total gain = 15.37dBV @2.2GHz

The overall noise of the system needs to be simulated differently, since it is a combination of “sp”, “pss” and “transient analysis” all three must be enabled. The reason for this is “sp” can only take 2 ports at once, which are reserved for input and output of the LNA, the third port in the circuit is the input of the harvester itself. “pss” only needs the output port to be selected and the input port is chosen after the simulation, also it allows for stabilization time. “Transient analysis” is the time-based simulation and is needed to allow the harvester to reach settling time and to allow “pss” its own stabilization time. Figure (5.20) is the LNA noise figure with a DC power supply as the power source and with the harvester as the power source.

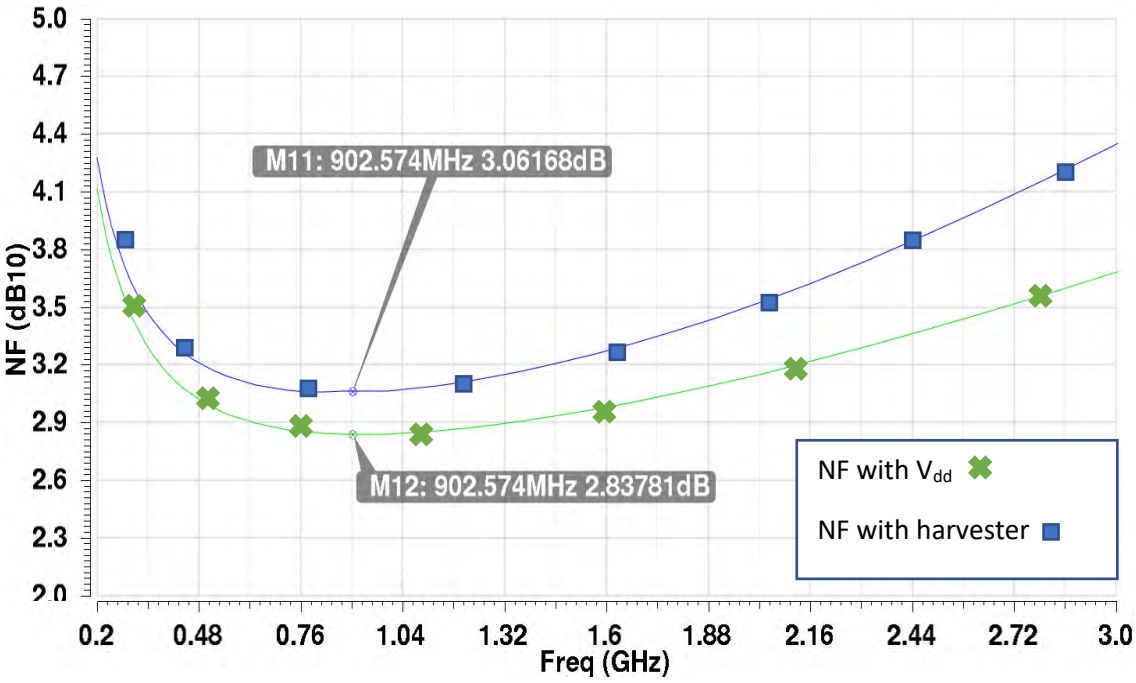


Figure 5.20 NF of the LNA with and without the Harvester, the harvester added a 0.2dB noise to the system. The noise of the harvester is related to PSRR

5.3 LNA and Harvester PVT

Figure (5.21) is the gain and NF of the circuit (LNA and harvester) with corner analysis and figure (5.22) is the legends for figure (5.21). The fast corner is done at -40°C, typical corner at 27°C, and slow corner at 85°C. This is done to take the best and worst case scenario of the circuit. Fast being the best and slow being the worst. Figure (5.23) is the S11 at all corners, even outside the 3dB bandwidth at 2.4GHz (which is an ISM band) S11 is still less than -10dB, making the design suitable for WSN.

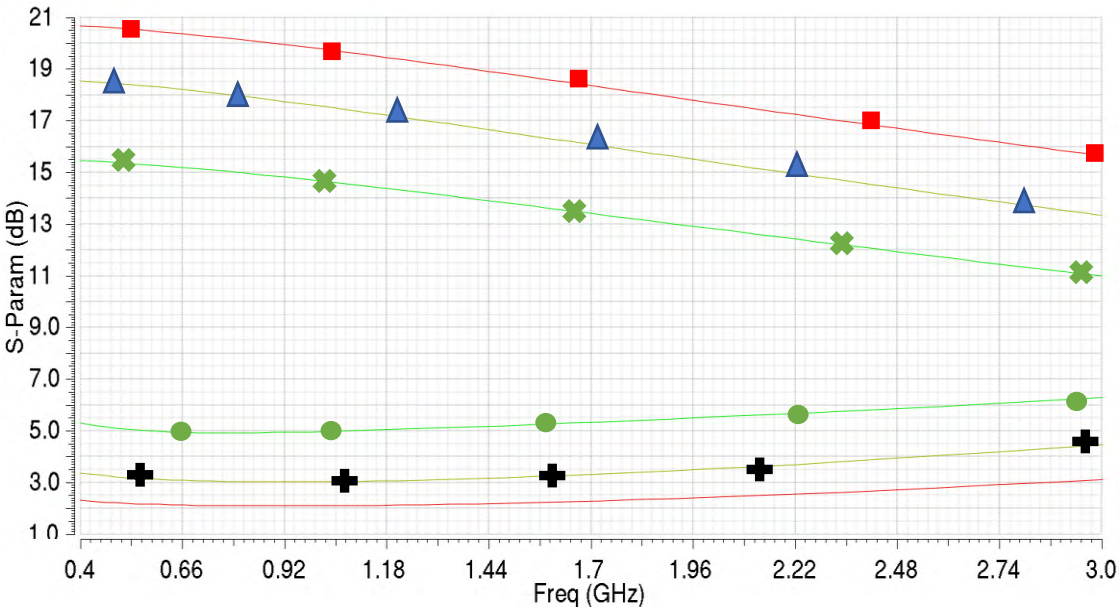


Figure 5.21 The Gain and NF of the LNA when powered by the harvester.

Figure 5.22 Legend for figure (5.21)

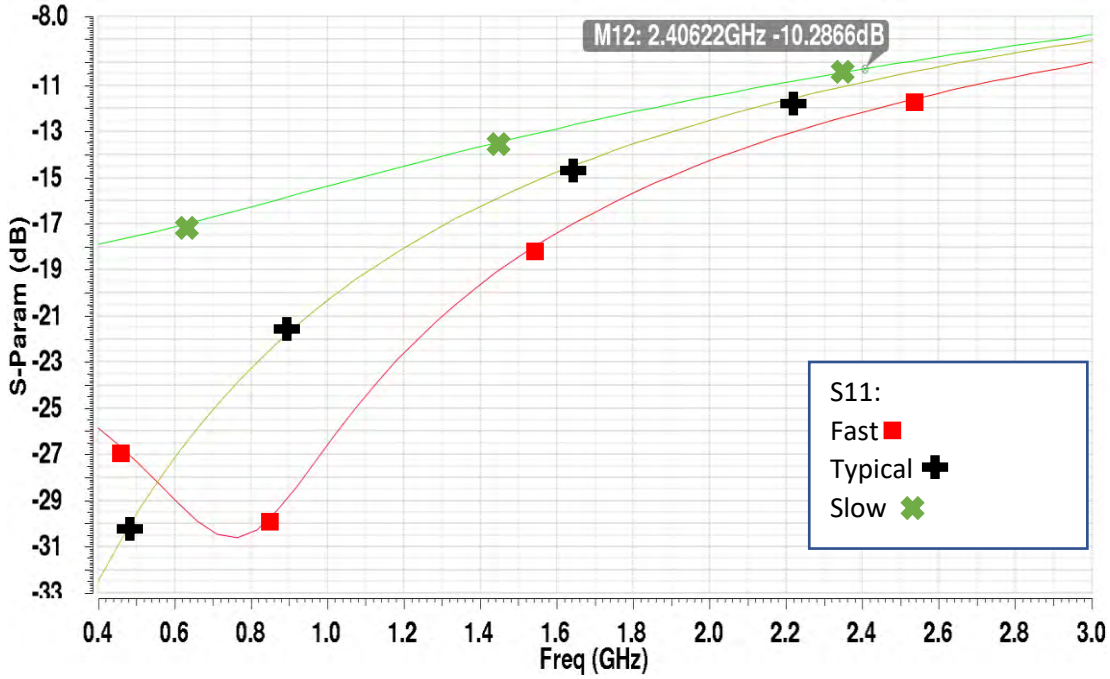


Figure 5.23 S11 at all three corners.

Using ADEXL tool from cadence, a table can be formed for all corners. The table itself can have specification added to it and will automatically compare the results with the specification provided to the ADEXL. Figure (5.24) are the corner analysis of the circuit in tabular format from ADEXL with an infinite output impedance, the S21, NF and S11 at key frequencies is displayed; start of bandwidth: 400MHz, GSM: 900MHz, end of band 1.8GHz and ISM band 2.4GHz. Figure (5.25) is the P1dB at 400MHz, 400MHz was chosen as the test frequency as it was the highest gain. All other frequencies will have a better P1dB.

Output	Spec	Weight	Pass/Fail	Min	Max	fast	typical	slow
S21 @ 400M				15.46	20.67	20.67	18.55	15.46
S21 @ 900M				14.85	19.98	19.98	17.78	14.85
S21 @ 1.8G				13.23	18.14	18.14	15.86	13.23
S21 @ 2.4GHz				12.08	16.86	16.86	14.56	12.08
NF @ 2.4GHz	< 5		fail	2.74	5.812	2.74	3.974	5.812
NF @ 1.8G	< 5		near	2.381	5.39	2.381	3.464	5.39
NF @ 400MHz	< 5		near	2.336	5.295	2.336	3.425	5.295
NF @ 900MHz	< 5		pass	2.142	4.948	2.142	3.086	4.948
Vdd				1.287	1.985	1.406	1.287	1.985
Id				-7.151m	-6.461m	-7.151m	-6.97m	-6.461m
S11 @ 2.4G	< -10		pass	-13.42	-11.04	-13.42	-11.86	-11.04
S11 @ 1.8G	< -10		pass	-15.68	-12.17	-15.68	-13.56	-12.17
S11 @ 900M	< -10		pass	-28.82	-15.83	-28.82	-21.71	-15.83
S11 @ 400M	< -10		pass	-32.5	-17.9	-25.88	-32.5	-17.9

Figure 5.24 Corner analysis for the circuit. Green, yellow and red colors are pass, near and failing specification, respectively.

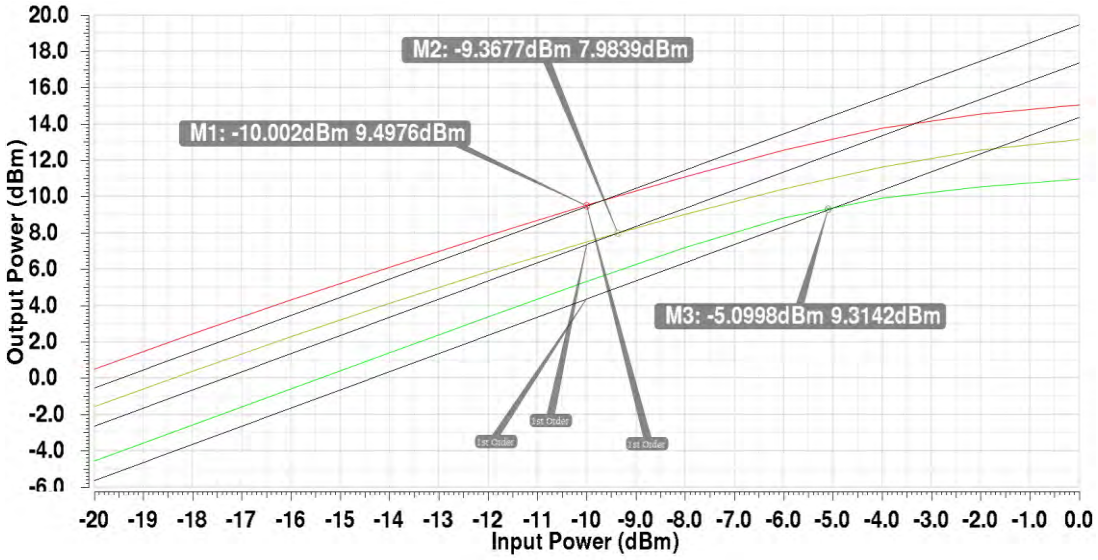


Figure 5.25 P1dB at the three corners.

5.4 Stability and PVT of each side of the System

Because an ideal buffer was used (VCVS), S12 is a zero value, this implies that the stability factor K_f is infinite. This scenario is unrealistic for stability analysis. Buffer are added to the system and each side of the LNA was tested individually. If the LNA is unstable; since the circuit is asymmetrical; it can be either from the CG or the CS stage of the circuit, figure (5.26) is the LNA and harvester with output buffers from Cadence View. ***Buffers process and supply are kept at typical, but the buffers went through temperature variations.***

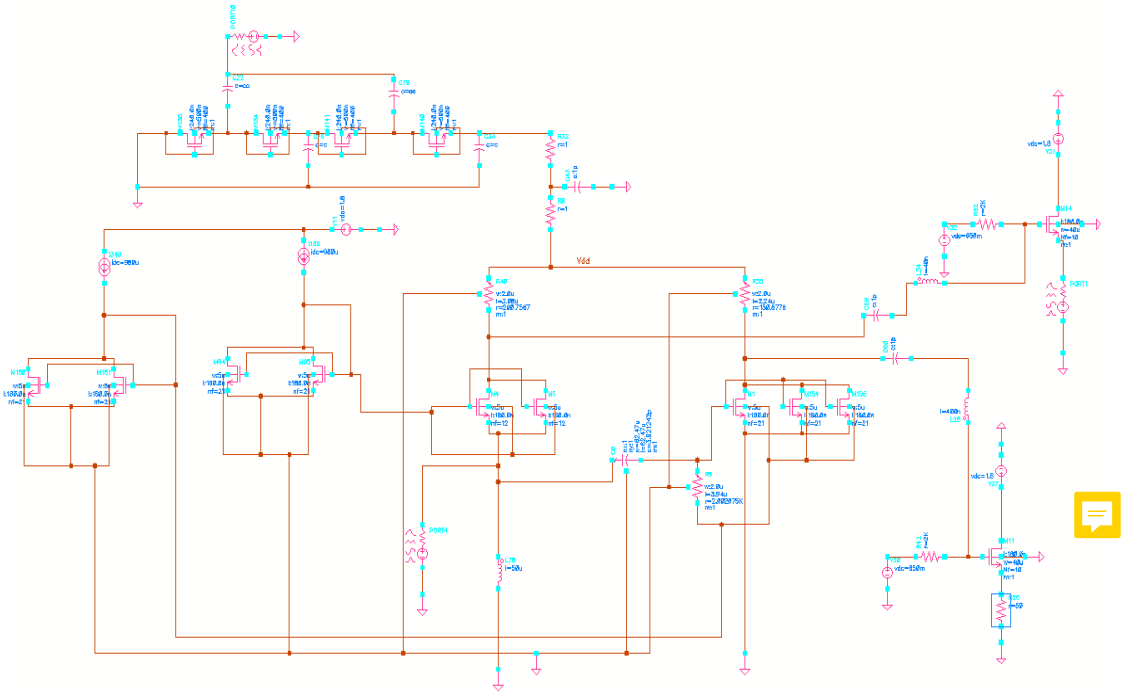


Figure 5.26 LNA and Harvester with buffers circuit.

The reason buffers power consumption is not taken into consideration as they are not part of the design, they are only used to measure the stability factor which is not possible with an infinite output impedance. The buffers are also considered to be ideal, where there values (width, length, etc) are unreasonable for a transistor, this is only possible as the transistors used are “test” transistors from the PDK and have infinite values (width, length, etc). Most PDKs come with such a transistor, but this transistor has no layout schematic and cannot be fabricated.

5.4.1 Common-gate at low frequencies (center @500MHz): Buffers process and supply is kept at typical but went through temperature variations, minor changes are made to the circuit to compensate for buffer loses. Inductor of 400n for CG are used in series with the buffers gate for matching with a resistor of 30 ohms. Input power increased from 15dBm to 16dBm to compensate for buffer loses, both the CG and CS are ON in this test. Figure (5.27) is the gain of the CG with buffers, the inductors helps increase the gain to compensate for the buffer losses. Figure (5.28) is the ADEXL table of the parameters. Since, $Kfmin > 1$ and $B1fmin > 0$ for all frequencies from 0 to 1THz the CG is unconditionally stable.

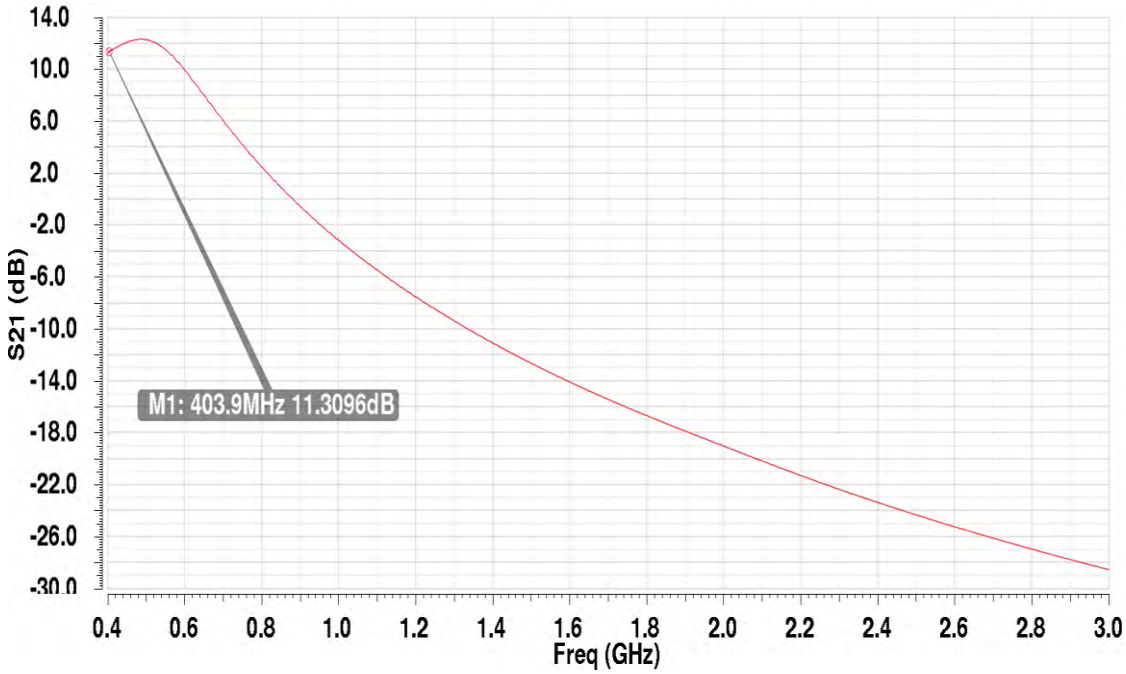


Figure 5.27 CG gain at typical corners with buffers.

The buffers do suffer from parasitics which effect the bandwidth, this is the reason for having a matching network for different center frequencies to help avoid this issue when testing for stability. The stability at that center frequency is tested, then the center frequency is shifted.

Output	Spec	Weight	Pass/Fail	Min	Max	fast	typical	slow
B1f min frequency				1T	1T	1T	1T	1T
Kf min frequency				500M	500M	500M	500M	500M
Kf min	> 1		pass	6.205	16.19	6.205	8.695	16.19
S21 @ 400M				6.227	13.63	13.63	11.24	6.227
Vdd				1.82	2.584	1.839	1.82	2.584
S21 @ 900M				-5.58	2.55	2.55	-560.3m	-5.58
B1f min	> 0		pass	760.5u	1.057m	1.057m	871u	760.5u
Id				-6.931m	-6.186m	-6.931m	-6.711m	-6.186m
S11 @ 2.4G	< -10		pass	-14.37	-11.98	-14.37	-12.94	-11.98
S21 @ 1.8G				-20.38	-13.63	-13.63	-16.69	-20.38
S11 @ 1.8G	< -10		pass	-19.59	-13.98	-19.59	-16.26	-13.98
S11 @ 400M	< -10		pass	-24.44	-17.18	-17.18	-24.44	-22.77
S11 @ 900M	< -10		pass	-40.98	-19.86	-24.1	-40.98	-19.86
S21 @ 2.4GHz				-26.4	-20.44	-20.44	-23.38	-26.4

Figure 5.28 Corner analysis and stability of CG at low frequencies.

5.4.2 Common-source at low frequencies (center @500MHz): Buffers process and supply is kept at typical but went through temperature variations, minor changes are made to the circuit to compensate for buffer loses. Inductor of 400n for CS is used in series with the buffers gate for matching with a resistor of 30 ohms. Input power increased from 15dBm to 16dBm, both the CG and CS are ON in this test. Figure (5.29) is the gain of the CS with buffers, the inductors helps increase the gain to compensate for the buffer losses. Figure (5.30) is the ADEXL table of the parameters. Since, $Kfmin > 1$ and $B1fmin > 0$ for all frequencies from 0 to 1THz the CS is unconditionally stable.

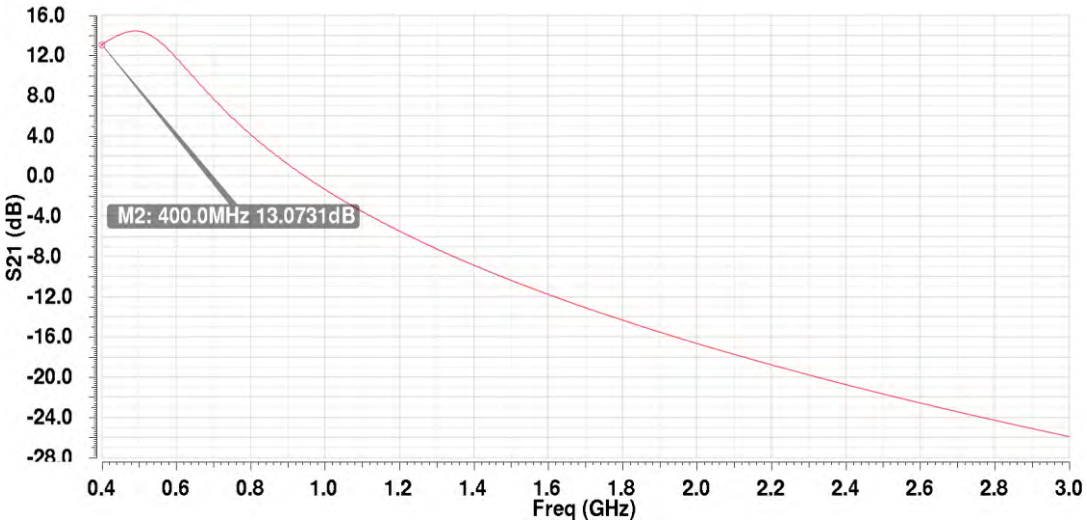


Figure 5.29 CS gain at typical corners with buffers.

Output	Spec	Weight	Pass/Fail	Min	Max	fast	typical	slow
B1f min frequency				1T	1T	1T	1T	1T
Kf min frequency				500M	500M	500M	500M	500M
Kf min	> 1		pass	57.75	88.34	57.75	66.82	88.34
S21 @ 400M				11.15	14.78	14.78	13.07	11.15
S21 @ 900M				-1.43	3.489	3.489	1.183	-1.43
Vdd				1.82	2.584	1.839	1.82	2.584
B1f min	> 0		pass	761.8u	1.06m	1.06m	872.5u	761.8u
Id				-6.958m	-6.207m	-6.958m	-6.735m	-6.207m
S21 @ 1.8G				-17.29	-11.99	-11.99	-14.35	-17.29
S11 @ 2.4G	< -10		pass	-15.29	-12.5	-15.29	-13.87	-12.5
S11 @ 1.8G	< -10		pass	-18.27	-13.95	-18.27	-16.21	-13.95
S11 @ 400M	< -10		pass	-24.38	-17.07	-17.07	-24.38	-22.8
S21 @ 2.4GHz				-23.77	-18.35	-18.35	-20.75	-23.77
S11 @ 900M	< -10		pass	-38.88	-19.51	-25.01	-38.88	-19.51

Figure 5.30 Corner analysis and stability of the CS at low frequencies.

5.4.3 Common-gate at high frequencies (center @2.1GHz): Buffers process and supply is kept at typical but went through temperature variations, minor changes are made to the circuit to compensate for buffer loses. Input power increased to 16dBm to compensate for buffer loses. RCG increased from 200 to 250 to increase the gain. Inductor of 30n for CG is used in series with the buffers gate for matching with a resistor of 50 ohms. Figure (5.31) is the gain of the CG with buffers, the inductors helps increase the gain to compensate for the buffer losses. Figure (5.32) is the ADEXL table of the parameters. Since, $Kfmin > 1$ and $B1fmin > 0$ for all frequencies from 0 to 1THz the CG is unconditionally stable.

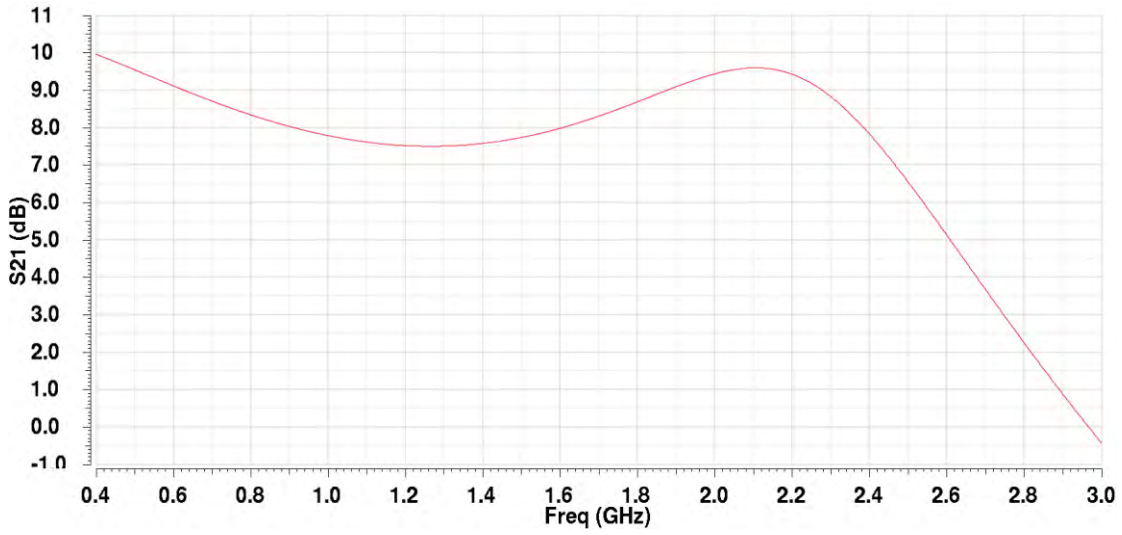


Figure 5.31 CG gain at typical corners with buffers.

Output	Spec	Weight	Pass/Fail	Min	Max	fast	typical	slow
B1f min frequency				1T	1T	1T	1T	1T
Kf min frequency				1.899G	2.099G	2.099G	1.999G	1.899G
S21 @ 1.8G				6.245	10.9	10.9	9.179	6.245
S21 @ 2.4GHz				3.738	9.358	9.358	6.865	3.738
S21 @ 900M				3.646	10.18	10.18	8.006	3.646
S21 @ 400M				3.245	11.12	11.12	8.643	3.245
Kf min	> 1		pass	2.883	4.64	2.883	3.479	4.64
Vdd				1.827	2.384	2.009	1.827	2.384
B1f min	> 0		pass	668.7u	695.6u	695.6u	668.7u	688.3u
Id				-6.71m	-5.342m	-6.71m	-6.35m	-5.342m
S11 @ 1.8G	< -10		pass	-15.17	-11.75	-12.76	-15.17	-11.75
S11 @ 2.4G	< -10		pass	-19.09	-13.07	-16.09	-19.09	-13.07
S11 @ 900M	< -10		pass	-21.38	-14.61	-17.17	-21.38	-14.61
S11 @ 400M	< -10		pass	-31.43	-17.06	-21.2	-31.43	-17.06

Figure 5.32 Corner analysis and stability of the CG at high frequencies

5.4.3 Common-source at high frequencies (center@2.1GHz): Buffers process and supply voltage is kept at typical but went through temperature variations, minor changes are made to the circuit to compensate for buffer loses. Input power increased to 16dBm to compensate for buffer loses. RCS increased from 150 to 200 to increase the gain. Inductor of 30n for CS is used in series with the buffers gate for matching with a resistor of 50ohms. Figure (5.33) is the gain of the CS with buffers, the inductors helps increase the gain to compensate for the buffer losses. Figure (5.34) is the ADEXL table of the parameters. Since, $Kfmin > 1$ and $B1fmin > 0$ for all frequencies from 0 to 1THz the CS is unconditionally stable.

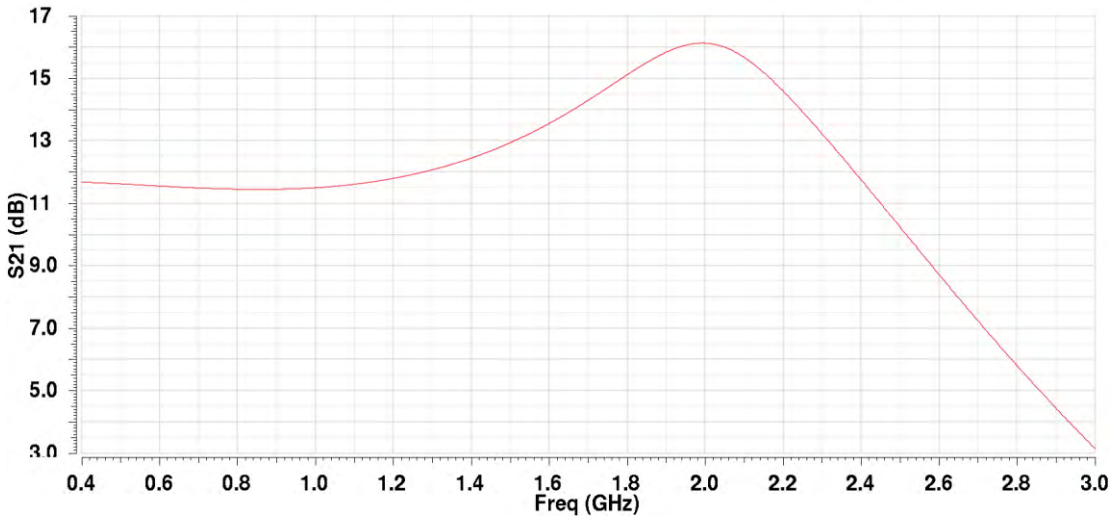


Figure 5.33 CS gain at typical corners with buffers.

Output	Spec	Weight	Pass/Fail	Min	Max	fast	typical	slow
B1f min frequency				1T	1T	1T	1T	1T
Kf min frequency				1.899G	1.899G	1.899G	1.899G	1.899G
S21 @ 1.8G				12.15	15.02	15.02	13.67	12.15
S21 @ 2.4GHz				8.679	14.18	14.18	11.53	8.679
S21 @ 400M				9.458	12.79	12.79	10.95	9.458
S21 @ 900M				9.397	12.62	12.62	10.84	9.397
Kf min	> 1		pass	5.701	7.491	5.701	6.095	7.491
Vdd				1.827	2.385	2.009	1.827	2.385
B1f min	> 0		pass	922.7u	1.373m	1.373m	1.09m	922.7u
Id				-6.707m	-5.343m	-6.707m	-6.349m	-5.343m
S11 @ 1.8G	< -10		pass	-15.37	-11.93	-12.83	-15.37	-11.93
S11 @ 2.4G	< -10		pass	-19.41	-13.15	-16.59	-19.41	-13.15
S11 @ 900M	< -10		pass	-21.36	-14.6	-17.14	-21.36	-14.6
S11 @ 400M	< -10		pass	-31.39	-17.05	-21.19	-31.39	-17.05

Figure 5.34 Corner analysis and stability of the CS at high frequencies

From figure (5.27) to figure (5.34) most of the LNA specifications are plotted with harvester output voltage and current. Since the $Kfmin > 1$ and $B1fmin > 0$ for all frequencies from 0 to 1THz for the CS and CG, this makes the LNA unconditionally stable. Although the supply voltage did not change in the PVT simulation, when the transistors themselves go through process and temperature variation the harvester efficiency being affected, meaning the circuit is indirectly subject to voltage variations. As for the biasing, since the current mirror transistors also go through process and voltage variations, the biasing is affected accordingly.

Chapter 6. Conclusion

Balun LNA is a differential pair, therefore the thermal noise is expected to cancel if the LNA is designed properly. Chapter 2 discussed different types of receivers superhetrodyne, zero-IF and homodyne with their advantages and disadvantages, background information about different parameters such as P1dB, S-parameters, and IMD. Chapter 3 described different types LNA topologies such as CG, CS differential and Balun LNAs, tradeoffs when designing an LNA and thermal noise calculation of transistors and resistors. Chapter 4 introduced energy harvesters and the basic concept of RF energy harvesting, also why the equations are not used to determine the properties of the CPR rather sweeping to find the parameters is the best option. Chapter 5 are the literature review of LNAs and low power applications, with major focus on the Balun LNA thermal noise analysis with a step by step analysis of the thermal noise done to reproduce an already derived noise figure equation for the Balun LNA, this was done to follow the sequence of thinking for the next noise derivation. Chapter 6 introduced cadence and the basic test benches to start the design, also the impact of FBB on the circuits gain, noise, biasing and DC simulations shown, which concluded with FBB increases the gain for the same biasing voltage, reduces the noise at the lower frequencies but increases noise at higher frequencies, the increase in noise can be due to an increase in parasitic. Chapter 7 detailed a step by step analysis of the noise and it proved that the condition for balancing the Balun LNA will cancel the thermal noise of both Balun transistors and not only the CG stage. If the unbalance of the output gain is created due to the CS stage having higher gain than the CG stage, the addition of a degeneration resistor to the CS to balance the output was presented. The degeneration resistor impact on the thermal noise cancelation was derived and simulated, concluding with: A reduction of the gain unbalance with a degeneration resistor can reduce the transistors thermal noise (or cancel it) without changing the transconductance g_m or the drain resistors R_D. A new set of conditions revolving around CS degeneration were derived to balance and cancel the thermal noise. PVT variation for the LNA alone were simulated where gain, noise and phase are compared for all three corners. Chapter 8 detailed the choice of transistor for the harvester, three transistors are tested: triple well, low threshold, zero threshold transistors, with all simulations and testing pointing

towards the low threshold transistor with FBB is the most efficient option. The number of CPR stages from one to three has been tested, chapter 8 concluded with: 2-stage Dickson charge pump using FBB low threshold transistors as the most efficient configuration and most suitable option for the RF harvester from the UMC180nm PDK. Chapter 9 is the LNA and Harvester integrated together to work as one unit, although the harvester efficiency dropped due to it not having the optimum load, the LNA was successfully powered by the harvester and the overall noise of the system simulated, corners of the overall circuit are taken (PVT) although the supply voltage was not directly varied, the impact of process and temperature on the harvester and biasing indirectly effected the supply value, making PVT complete.

As for future work, a smaller technology (65nm) can be used to further lower the power consumption of the LNA and increase the efficiency of the harvester. A layout to be carried out with extraction view pre-fabrication stage. Also, an addition of a wideband matching network can be added to the output of the LNA. The harvester can be modeled with inductive coupling input for the power transfer to take into consideration the loses and properly estimate its efficiency. Due to the LNA not being the optimal load for the harvester, efficiency has been lost which requires further studying and research to optimize this mismatch issue.

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