DESIGNING LOW FREQUENCY I.C FILTER USING PSEUDO RESISTOR FOR BIOPOTENTIAL MEASURMENTS

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ABSTRACT

Standard medical diagnosis requires attaching sensors or electrodes to the patient and then connecting these electrodes to bulky equipment powered by mains supply. This is usually an acceptable procedure for short term patient monitoring. However, for long term monitoring, this approach is neither comfortable nor durable. Therefore considering fully implantable electronic systems which have many useful applications including monitoring cardiac irregularities in pacemaker systems, are the preferred.

This thesis intends to show the design of low frequency IC filters. Given that large time constants are required in low cutoff frequency filter designs, various approaches can be utilized to provide large values of resistors or capacitors.

To demonstrate the proposed method, third order low-pass and high-pass filters for ECG signals with cutoff frequencies in range of 0.1-100 Hz are implemented. Butterworth topology is used in both filter designs to preserve the morphological information of the ECG signals.

Here, we focused on increasing the resistor values via using MOS pseudo resistor where large values of resistors can be accomplished with small die area. A pseudo resistor is simply a MOSFET that is biased in weak inversion region where the gate voltage is below threshold voltage. Weak inversion is used in ultra low power designs. When transistor is biased in weak inversion Vg < Vth , for fixed gate voltage, different approaches can be utilized to provide large values of resistors. This can be summarized as follow:

- If Vgs<Vth and $V_{DS}<U_T$, where U_T is the thermal voltage =26 mV , then the transistor has a fixed resistance and it is of the order 10^9 ohms. This resistor can be used in designing filters if V_{DS} is less than $3U_T$ to $5U_T$ and this resistance is called the pseudo resistor.
- If Vgs<Vth and $V_{DS}>U_T$, then the transistor has a fixed resistance and it is independent of V_{DS}. However, since λ is not zero, r_o exists and it is of the order 10^9 ohms and the transistor acts as a current source. However, V_{DS} should be greater than 100 mV which means biasing is required. This resistor can be used in designing filters if V_{DS} is more than 100mV, this concept has been used in OTA designs.
- If transistor is in saturation and Vgs= $V_{DS}<U_T$, then the transistor has a fixed resistance and it is of the order 10^{10} ohms. This resistor can be used in designing filters if V_{DS} is less than 25mv.
- If transistor is in saturation and Vth>Vgs= $V_{DS}>U_T$, then the transistor has an exponential relationship between I_D and V_{DS}. This prevents from using the transistor as a resistor.

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CHAPTER 1

INTRODUCTION

Bioelectric signals are produced as a result of electrochemical activity of excitable cells including nervous, muscular or glandular tissue evoked potential. Biopotential signals are detected by electrodes which convert low level ionic currents into electronic desired signal and unwanted noise. The voltage amplitude and frequency bandwidth ranges of some common bioelectric signals are shown in Table 1 [1].

Table 1: Bioelectric signals amplitude and frequency range

Source	Amplitude (mV)	Frequency Bandwidth (Hz)
Electrocardiogram (ECG)	1–5	0.1–100
Electroencephalogram (EEG)	0.001–0.01	0.1–40
Electromyogram (EMG)	1–10	20–2000
Electrooculogram (EOG)	0.01–0.1	dc–10

The additive noise spectrum covers both low and high frequencies. The noise is caused by electrode electrolyte interface and motion artifacts, 50 Hz power line interference, noise generated by muscular contractions, thermal noise and RF interference. The analog pre processing stage of a typical data acquisition system contains amplification and filtering to reduce the unwanted noise and enhance the desired biopotentials. Therefore the signal is amplified to an adequate level with low noise and low distortion over the required range of frequency [1]. Figure 1 shows the block diagram of a typical biomedical data acquisition system:

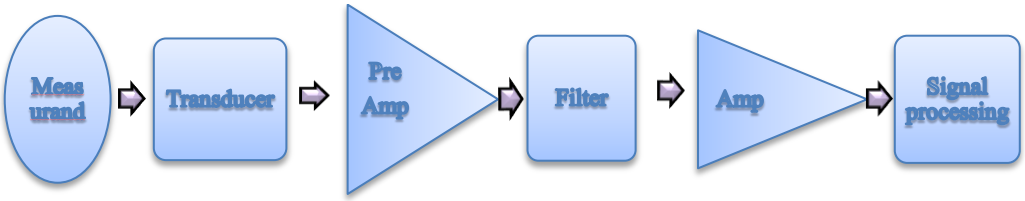


Figure 1: Typical data acquisition system of biomedical signals [1]

The analog preprocessing stage contains anti-aliasing low pass filter and high pass filter. The high pass filter is required to block the high amplitude low frequency drift voltage generated mostly by electrode electrolyte interface and motion artifacts. The low pass filter is used to limit the frequency band of biomedical signals and reduce additive noise prior sampling.

Constant gain in the pass band is the major feature for these filters to preserve the clinical information embedded in the morphology of the filtered signal, so Bessel or Butterworth filters are preferred to other topologies.

Standard medical diagnosis requires attaching sensors or electrodes to the patient and then connecting these electrodes to bulky equipment powered by mains supply. This is usually an acceptable procedure for short term patient monitoring. However, for long term monitoring, this approach is neither comfortable nor durable. Fully implantable electronic systems can have many useful applications including monitoring cardiac irregularities in pacemaker systems, left ventricular assist devices and artificial hearts. Multielectrode neural recordings are used to observe the simultaneous activity of large numbers of neurons in the brain for the exploration of the brain and its physiological functions at the cortical as well as the deep brain levels [1]. However, implantable devices which include filters pose another set of problems that need to be addressed.

The main design specifications of an implantable integrated circuit filter design are:

- Low noise
- High Dynamic Range
- Low distortion
- Small die area
- Reduced power consumption

Biomedical signals have low frequency range. For example ECG signals occupy a frequency bandwidth 0. 1-100 Hz while EEG signals occupy 0.1-40 Hz [2]. Signals to be processed are in range of 10μV-10mV [2]. Due to silicon area limitations in the integrated circuit, practical capacitors are limited to below 50 pF.

The simplest form of a low pass or high pass filter uses one resistor and one capacitor. Transfer function of a low pass filter is

$$T(s) = \frac{1}{1+sRC} \tag{1}$$

where RC is the time constant τ.

The cut-off frequency (in Hz) of the filter is therefore determined from this time constant as:

$$f = \frac{1}{2\pi RC} \tag{2}$$

For a low frequency, a large time constant is needed, which means that the value of R and/or C needs to be very large. For example a low pass filter with cutoff frequency of 100 Hz would require a capacitor value of 10 pF which results in resistor value of 0.159 GΩ. If the filter to be implemented using discrete components on a printed circuit board then there should be no problem because of the availability of such R and C values. However, if such filter needs to be implemented on integrated circuit, then fabricating such C and R values becomes a challenge. This is where the problem is raised in implantable biomedical applications that need to occupy very small area. Therefore the resistance and capacitance required have to be realized by other means or special circuit techniques to achieve the desired large time constant.

To accomplish this task, several techniques have been proposed which will be discussed in detail throughout the literature review.

It is well known that Digital Signal Processing (DSP) is a powerful technique for low frequency applications however biomedical signals carry large amplitude undesirable low frequency drift signals. The amplitude of such artifact signals is greater than those of the desired biopotentials. The small bio signal may be in range of micro volts accompanied by the low frequency drift, so if high gain is required immediately, the amplifier will saturate and the desired signal will be lost. This is why a small gain in range of 10-100 is first used followed by filtering and a second stage

of amplification. Therefore the signal fed to the analog to digital converter will have high resolution.

This research is intended to design an implantable low pass and high pass filter for ECG signals. The first emphasis will be on designing a low pass filter with cutoff frequency of 100 Hz and then a high pass filter with cut off frequency of 0.1 Hz.

It is known that filter design at low frequencies is not a trivial task in a sense to achieve large time constants where small chip area is of high interest. This led to use the MOSFET pseudo resistor elements. To obtain a pseudo resistor element in a circuit, the resistors are replaced by MOSFET transistors, where the source and drain nodes correspond to the two terminals of the resistor and the drain current corresponds to the current passing through the resistor. Pseudo resistor elements are two terminal circuit elements whose current is a function of the instantaneous difference in the pseudo voltage across the two terminals, where pseudo voltage is a nonlinear function of the source and drain voltage at each terminal.

Each pseudo resistance value is controlled by the gate voltage of the transistor as long as it's weekly inverted. Harrison [3] used this concept for the first time in design of low power low noise neural amplifiers. He provided large values of resistors by pseudo resistors. Where the low cut off frequency required for his design was resulted from use of pseudo resistors and coupling capacitors while the high cut off frequency was generated through the -3 dB of OTA which could be varied according to biasing current. This concept has been used by some other authors as well were they have elaborated on the design of OTA, or how to get results in a pulse generated form. What considered in this work are different approaches in designing pseudo resistors. In the first approach, a PMOS is used to provide the required amount of resistance which is called a single tunable pseudo resistor where in the second approach the so called double tunable pseudo resistor, two identical PMOS will provide this resistance. The current voltage characteristics of both will be covered in detail to know how they behave for different values of gate voltages.

A third order Butterworth filter is selected since in ECG signal the fidelity of the sharp QRS spike must be preserved for diagnosis, there must be little rounding of R peak and no transient "ringing" following QRS spike [4]. Sallen & key is the

architecture studied in design of third order Butterworth low pass and high pass filters.

To view the results in more detail, not only the third order but also the first and second order LPF & HPF are designed. Single tunable and double tunable pseudo resistor concept has been tested for each and every filter and the results of all have been compared with respect to the desired cut off frequency of 0.1 Hz and 100 Hz for HPF & LPF respectively. All of the transistors used in this design are real transistors from AMS library in AWR software with 0.35µ process.

The results of using ideal and real components as for other elements of the circuit will be evaluated to see how they affect the overall cut off frequency. As a final point the linearity, noise and power consumption of the pseudo resistors as part of the circuit will be measured.

CHAPTER 2

BACKGROUND AND LITERATURE REVIEW

This chapter introduces methods that have already been used to increase the resistance or capacitance in different circuits. Switched capacitors, Miller effect and gyrators are methods which will be discussed in detail. Furthermore low frequency filter design using reduced G_m will be explained in detail. These methods will present how to decrease the transconductance of an operational transconductance amplifier (OTA) in order to reach low frequencies.

2.1 Alternative methods to Increase Resistance or capacitance in a circuit:

2.1.1. Switch Capacitor Topology:

Switch capacitors are used to increase the resistance of a network and as a result to decrease the cut off frequency [1]. The main operation of a switched capacitor is to use capacitors and analog switches to perform the same function as that of a resistor [5]. This switched capacitor circuit can then play the role of a resistor in an active filter circuit. The most basic setup of a switched capacitor circuit is shown in Figure 2.

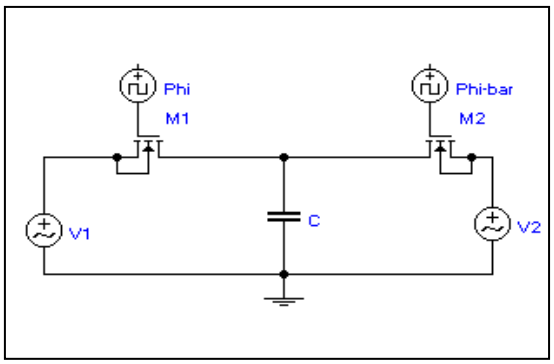


Figure 2: Basic setup for switched capacitor circuit

Figure above shows the switches as MOSFETs and a capacitor. The MOSFETS will be turned on when their gate voltages are high and will be off when the gate voltages are low. Both MOSFETs are driven by clock signals that are non-overlapping which means that the MOSFETS will conduct during alternate half cycles [5]. A simpler circuit diagram of a switched capacitor with the MOSFETs replaced by switches is shown in figure 3.

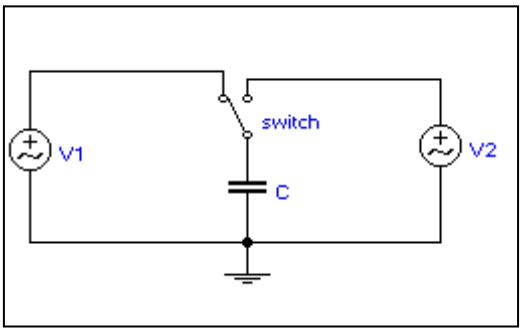


Figure 3: Circuit diagram of switch capacitor

When the switch is connected with the left side of the circuit the capacitor charges to V1. On the other hand, when the switch is connected to the right side of the circuit the capacitor charges up to V2. Due to this constant switching between the left and right side of the circuit, there will be a net charge transfer of

$$\Delta Q = C.\Delta V = C\ (V1 - V2) \tag{3}$$

The flipping of the switch from right to left and back is determined by the clock frequencyf_{CLK}. Therefore, the charge transferred in 1 second is

$$f_{CLK}.\Delta Q = C\ .f_{CLK}.(V1 - V2) \tag{4}$$

The switched capacitor circuit can act like a resistor with the condition that the f_{CLK} is much higher than the frequency of the voltage waveforms. This means that the switching process can be considered as almost continuous [5]. The circuit diagram of the equivalent resistance modeled from the switched capacitor is shown in Figure 4.

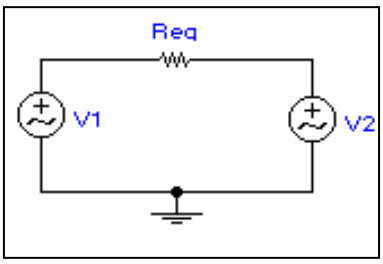


Figure 4: Equivalent resistance modeled by switched capacitor

The value of this equivalent resistance is then given by:

$$R_{eq} = \frac{V1-V2}{I_{AVG}} = \frac{1}{C.f_{CLK}} \quad (5)$$

Table 2 summarizes the advantages and disadvantages of using switch capacitors.

Table 2: Advantages & Disadvantages of switch capacitors

Advantages	Disadvantages
High accuracy	Pre and post filtering
Low sensitivity to parasitic capacitors	Aliasing and switching problems
Low harmonic distortion	Low precision
Bandwidth can be easily programmable	

2.1.2 Miller Effect:

In this technique, the capacitor is connected in feedback with a voltage amplifier with voltage gain equal to A_v , therefore the effective capacitor is equal to $(1+ A_v)C_L$ [1].

Miller Effect works by increasing the capacitance of an inverting voltage amplifier due to amplification between the input and output terminals [6]. Figure 5 shows an ideal voltage amplifier of gain A_v and it has an impedance Z connected between the input and output nodes.

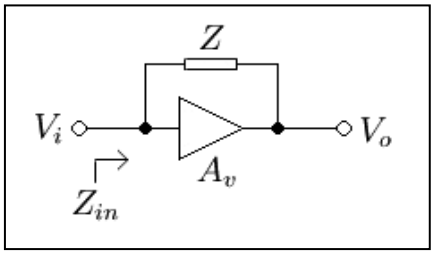


Figure 5: Ideal voltage amplifier

The output voltage of the above amplifier is $V_o = A_v V_i$ and the input current is

$$I_i = \frac{V_i - V_o}{Z} = \frac{V_i(1-A_v)}{Z} \quad (6)$$

The input impedance is then given by

$$Z_{in} = \frac{V_i}{I_i} = \frac{V_i Z}{V_i(1-A_v)} = \frac{Z}{1-A_v} \quad (7)$$

If the input impedance Z used in the amplifier is a capacitor, then

$$Z = \frac{1}{j\omega C} \quad (8)$$

Therefore, the resulting input impedance is given by

$$Z_{in} = \frac{1}{j\omega C(1-A_v)} = \frac{1}{j\omega C_M} \quad (9)$$

$$C_M = C(1 - A_v) \quad (10)$$

As shown above, the resulting capacitance is scaled by a factor of 1-A_v, with A_v being the gain of the amplifier.

Table 3 presents the advantages and disadvantages of Miller effect.

Table 3: Advantages & disadvantages for Miller capacitor

Advantages	Disadvantages
Increasing capacitance	Additional amplifier=more die area
	Swing reduction

2.1.3 Gyrators:

In [7] a scaled capacitor is obtained by using two gyrators or Riordan realization. A gyrator block diagram is shown below:

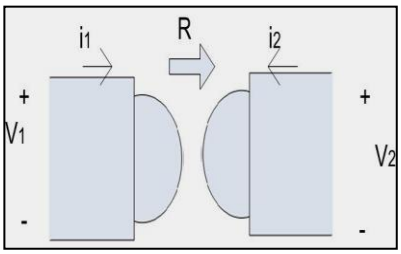


Figure6: Block diagram of a Gyrator [7]

This model is defined by currents and voltages:

$$V_1 = Ri_2 \quad (11)$$

$$V_2 = -Ri_1 \quad (12)$$

By connecting a load impedance to the output extremity of the Gyrator, looking from the input extremity

$$Z_i = R^2 \frac{1}{Z_L} \tag{13}$$

The load at the output extremity is terminated by a capacitor. From the input side we have

$$C_{eq} = \frac{R_2^2}{R_1^2} C \tag{14}$$

The above equation clearly stated that a scaled capacitor is obtained by using two gyrators. The circuit in figure 7 shows that the capacitance value can be multiplied by using two cascaded gyrators which consist of 4 op-amps, resistors and just 1 capacitor to act as a low pass filter.

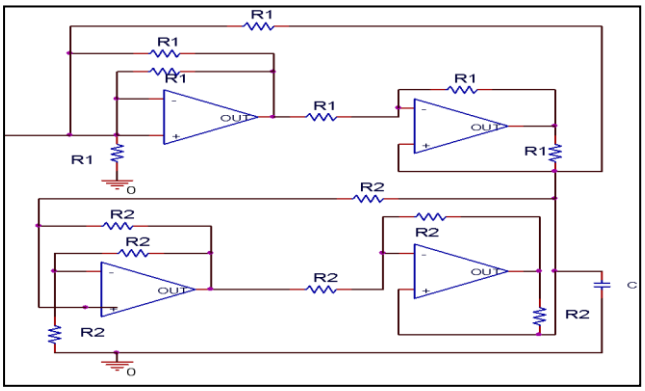


Figure 7: Cascade Gyrator to obtain larger capacitance value [7]

Recent study [7] suggested that instead of using two gyrators it is preferred to use Riordan realization of gyrators as shown below:

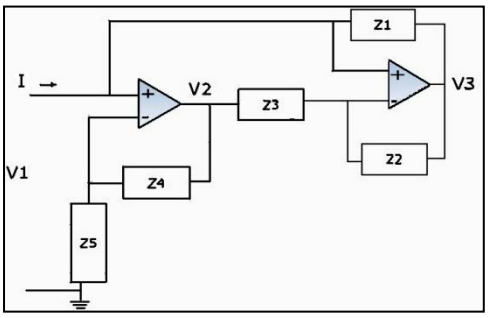


Figure 8: Realization of Gyrator introduced by Riordan [7]

The input impedance in the above circuit is

$$Z_{in} = \frac{V_1}{I} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \quad (15)$$

One can notice that by using Z_1 ,Z_3,Z_5 ,as a capacitor ,while other components are resistors, the input impedance will be a capacitor [7].

The gain of the system can be changed by changing the capacitor location. Therefore it is desirable to place the capacitor where least amount of current is to flow to avoid undesirable response. The capacitor values affect the gyrator performance. The best result is obtained when the filter response in very similar to that of the referenced response. The same applies for different resistor values [7].

Table 4 displays the advantages and disadvantages of the use of gyrators.

Table 4: Advantages & disadvantages for Gyrator

Advantages	Disadvantages
A filter with variable cut off frequency	Complex
No switching problem	Unstable
No need for pre & post filtering	

2.2. Low pass Filter Designs with Reduced G_m:

In operational transconductance amplifier (OTA) filters, the time constant is inversely proportional to transconductance and directly proportional to the capacitor. Therefore some methods should be utilized to decrease the transconductance in order to reach low frequencies.

2.2.1 Capacitive Scaling Scheme & OTA Reduced G_m:

This technique is using both linearized OTA based on current division technique and impedance scalars in conjugate with each other. Current division technique and linear biased transistors are combined for implementation of OTA [1].

The input stage in a voltage to current convertor should be linearized in order to reduce the harmonic distortion. This can be achieved by using transistors biased in linear region with large saturation voltage [8]. Further G_m reduction can be done by current division as follow:

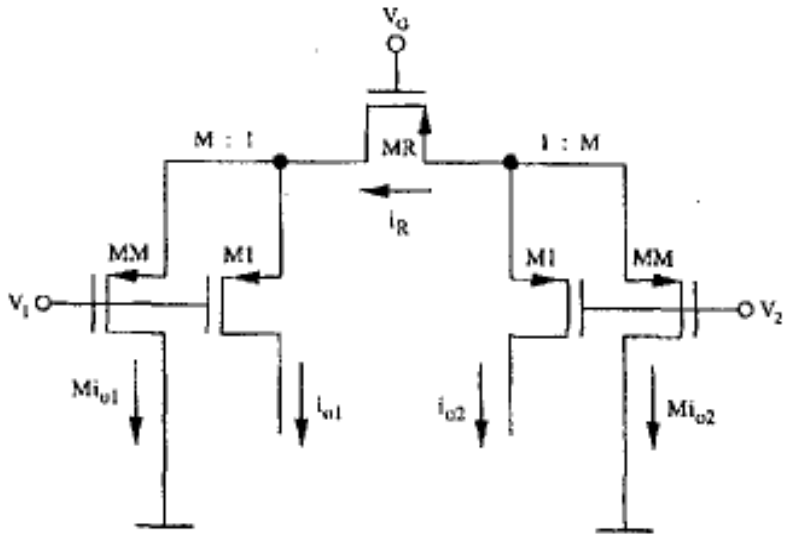


Figure 9: current division technique for low frequency voltage to current converters [8]

If the small signal transconductances are such that $g_mMM >> g_0MR$ and $M= g_mMM/ g_mM1>>1$, then the input voltage $V_{DS}MR$ (v_1-v_2) is converted to current by the linear biased transistor MR and this current is collected by MM and M1. Since $g_mMM» g_mM1$ only small part of the current is collected by the OTA output [8]. Therefore the OTA small signal transcoductance is

$$G_m = \frac{g_{0MR}}{M} = \frac{1}{M}\left(\mu_n C_{ox}\frac{W}{L}(V_G - V_{CM} - V_T)\right) \quad (16)$$

This shows that the G_m can be reduced by increasing M and reducing the saturation voltage [8]

$$V_{DSAT} = (V_G - V_{CM} - V_T) \quad (17)$$

The current division concept has been used for OTA design for low frequency applications. However an OTA using current division method for low frequency is shown below with slight modifications:

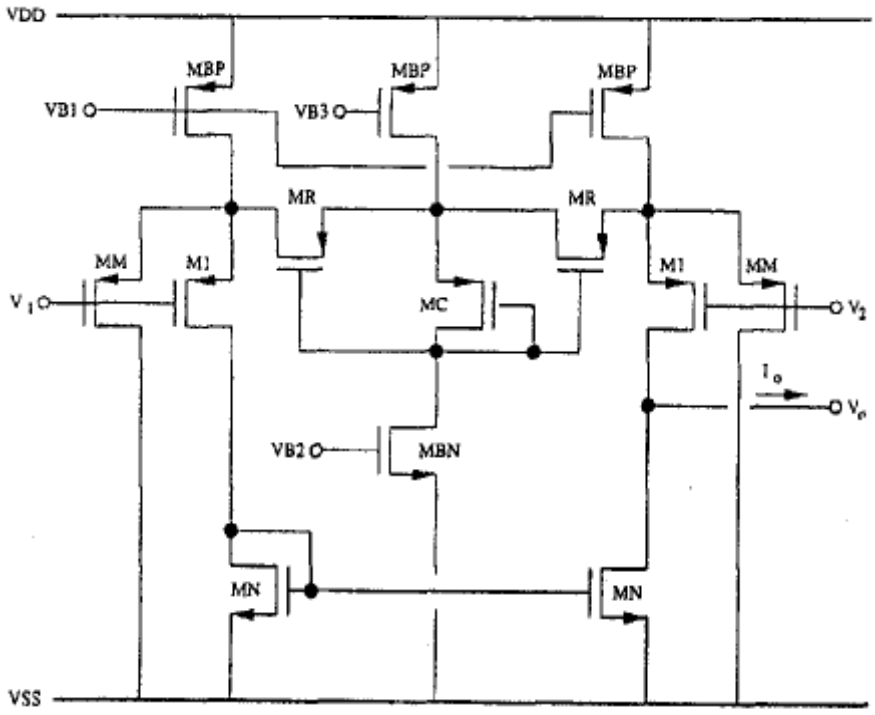


Figure 10: OTA for low frequency applications [8]

In this circuit the

$$G_m = \frac{g_{0\,MR}}{M+1} \quad (18)$$

This is controlled by adjusting V_{DS} of MC. Compared to the previous circuit, here MR is split into two transistors and its gate voltage is related to common source voltage. Thus transconductance is little sensitive to the common mode input voltage [8].

In low frequency applications flicker noise is an important issue which should be reduced to few micro volts. This can be accomplished by using P-channel transistors and increasing the gate area of the critical transistors.

Thermal noise components represent a fundamental limit for the noise level. MBP, MM and MR transistors have low noise contribution due to current division factor; thus most important noise sources are due to M1 and MN. However if the load capacitor is increased, noise level and g_mM1 and g_mMN are reduced.

“The effective impedance of a system is inversely proportional to the input current. If more current is generated for the same voltage, then the equivalent impedance is reduced; for capacitors, the equivalent capacitance in increased [8]. In [8] "the equivalent capacitance is scaled up by the current amplification factor if the current of the capacitor is sampled, amplified and feedback into the input". This is shown in figure 11:

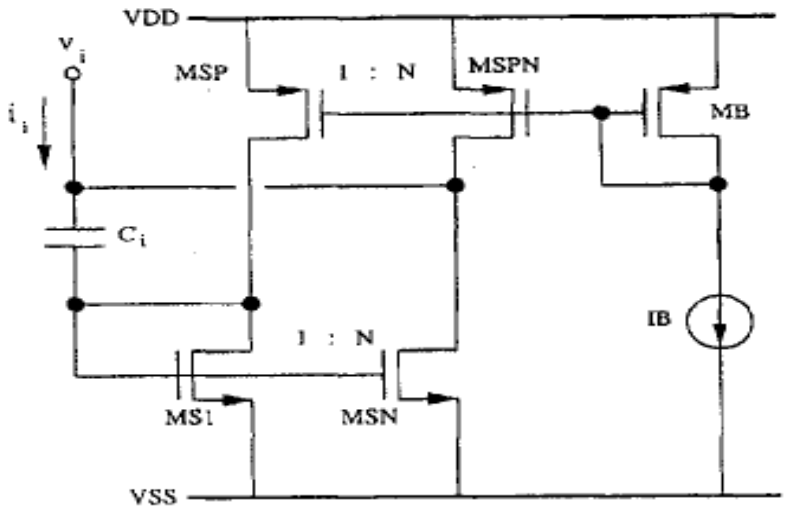


Figure 11: Basic circuit for capacitance scalar [8]

According to figure if the small signal transconductance of the diode connected transistor is large enough the equivalent impedance is

$$Z_i = \frac{V_i}{i_i} = \frac{1}{s(N+1)C_i} \tag{19}$$

It is clear that g_mMS1 must be increased for proper circuit operation; on the other hand the noise level of the impedance scalar increases. A cascade structure can be used to overcome this problem which results that the main noise components and the frequency operation of the impedance scalar to be almost independent [8].

Table 5 shows the advantages & disadvantages of this method.

Table 5: Advantages & disadvantages for capacitive scaling scheme & OTA reduced G_m

Advantages	Disadvantages
The precision of the resulting capacitor is high	500 pF and G_m 10^{-9} A/V
Low noise	
Low distortion	
Reduced harmonic distortion	
Increased dynamic range	

2.2.2 Current Cancellation:

In [2,9] the transconductance of OTA can be reduced by current cancellation technique. This technique employs partial positive feedback.

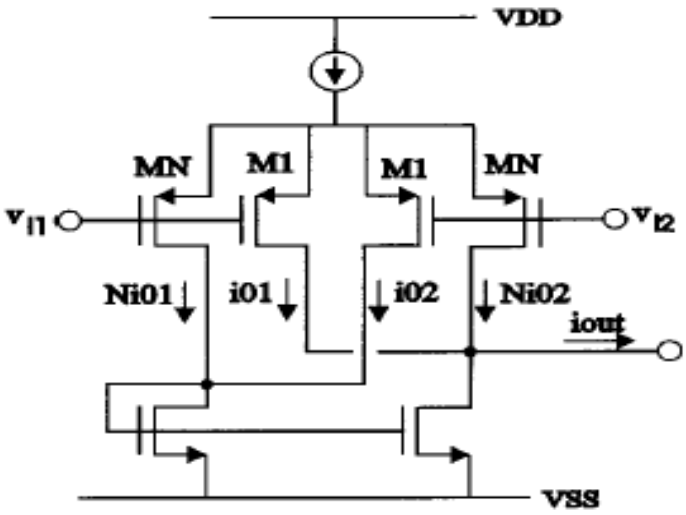


Figure 12: Current cancellation technique using partial positive feedback [2,9]

The OTA small signal transconductance is given by

$$G_m = \frac{N-1}{N+1} g_{m1} \tag{20}$$

Where N is the ration of the transconductance of MN to M1. G_m can be very small if N is nearly equal to 1.

Table 6 explains the advantages and disadvantages of current cancellation method.

Table 6: Advantages & Disadvantages for current cancellation

Advantages	Disadvantages
Good noise performance	Not very stable
	Sensitive to transistor mismatch

2.2.3 Transistor Biased in Linear Region with Current Divider:

Conductance in MOS transistor biased in linear region is proportional to $V_{DSAT} = V_{GS} - V_T$. By using very small saturation voltage small amount of conductance value can be obtained [1].

Also the current generated by a transistor biased in linear region can be split by current divider to reduce G_m further as shown in the figure below:

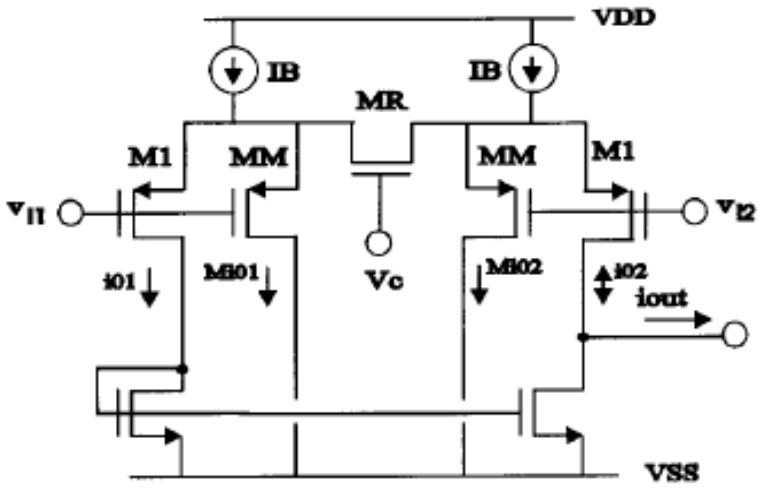


Figure 13: OTA based on a triode biased transistor & current division [9]

There is no positive feedback in this method. If the conductance of MR is much smaller than the transconductance of MM then [9]

$$G_m = \frac{2g_{m1}g}{2g+(1+M)g_{m1}} \tag{21}$$

Where M is the ration of the transconductance of MM to M1 and g is the small signal conductance of MR.

$$g \cong \mu C_{ox} \frac{W_R}{L_R}(V_{SGR} - V_{TR}) \tag{22}$$

Where R is used to denote parameters of MR. If 2g«(M+1)g_{m1} then [9]

$$G_m = \frac{2g}{(1+M)} \tag{23}$$

Due to this equation, the OTA transconductance can be further reduced by increasing factor M; which allow us to use higher bias voltage for triode biased transistor [9]. The noise level is mainly due to noise contribution of M1, MM and N-type transistors, however by using well known noise analysis techniques it can be reduced drastically. In low frequency applications flicker noise is a strong limitation for the OTA dynamic range. For smaller small signal transconductance, cross coupled technique can be incorporated to this topology as shown below:

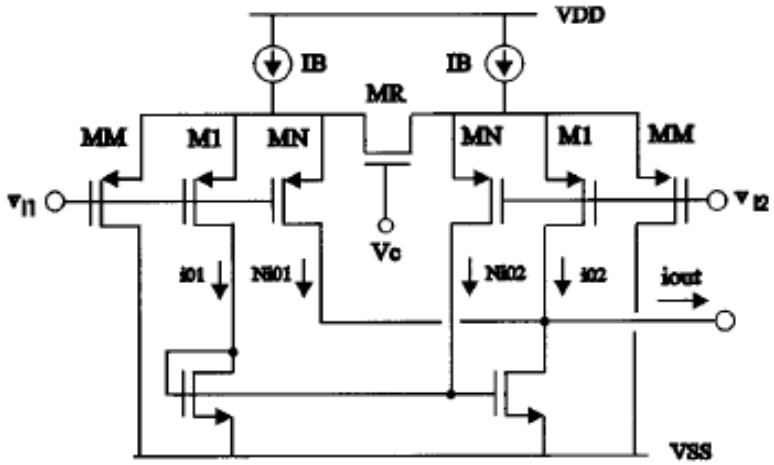


Figure 14: OTA with very low transconductance [9]

The G_m is given as

$$G_m = \frac{2(N-1)}{M+N+1}\left(\mu C_{ox}\frac{W_R}{L_R}(V_{GSR} - V_{TR})\right) \tag{24}$$

Where N is the ratio of transconductance of MN to M1. If N is near to 1, very small OTA transconductance can be achieved. The noise level of the OTA is increased since noise contribution of M1 and MN are of the same order of magnitudes [9].
The advantages and disadvantages of this method are summarized in table 7.

Table 7: Advantages & disadvantages for transistor biased in linear region with current divider

Advantages	Disadvantages
Harmonic distortion is reduced	For small V_{GS} , G_m is highly sensitive to V_T
	Harmonic distortion is inversely proportional to V_{DSAT}
	Increase offset voltage due to leakage current

2.2.4 Current Mirrors with Large Division Factors:

An OTA in negative feedback configuration has an output current that is proportional to the voltage difference between non-inverting input and output; this is the so called OTA-R [10].

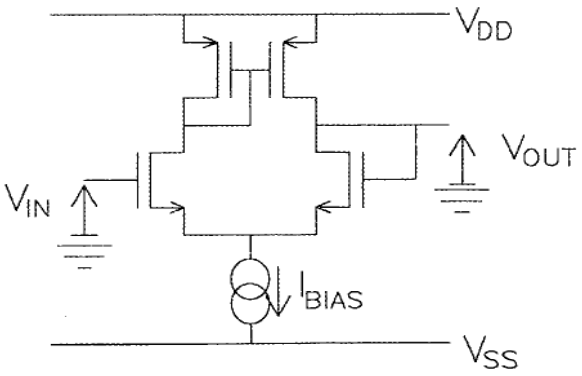


Figure 15: Schematic of a simple OTA in a negative feedback configuration used as an OTA-R [10]

For a given OTA-R the resistance value is tunable through the bias current. However this is limited by the change of the linear range of OTA-R. Figure below shows a new multiplication scheme for an OTA-R based on output current division [10].

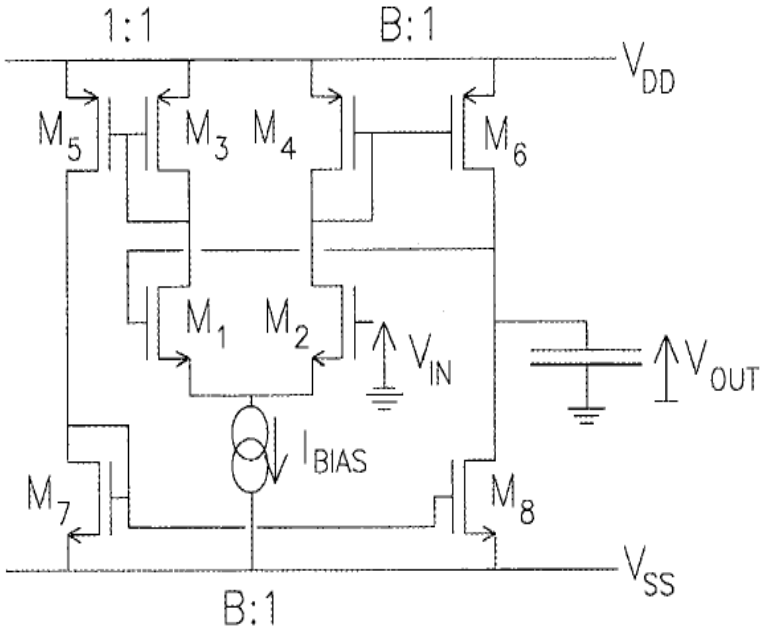


Figure 16: Principle transistor structure for OTA-R based transistor circuit [10]

Using large B factor makes it possible to use a large input bias current such that a linear input range of several volts is possible which allows to bias current mirrors in strong inversion. This reduces mismatch errors in the current mirrors themselves [10].

The time constant of the above circuit is

$$\tau = \frac{BC}{g_m} = \frac{BC}{\sqrt{\left(\mu C_{ox}\frac{W}{L}\right)_{DP} I_{BIAS}}} \tag{25}$$

To reduce the time constant BC should be decreased or I_{bias} should be increased. By splitting the large current division into succession of several smaller current divisions the current division factor is alterable. But with small current flowing through different branches, there is detrimental l for leakage current immunity.

The summary of advantages and disadvantages of this method is shown in table 8.

Table 8: Advantages & disadvantages of current mirror with large division factor

Advantages	Disadvantages
High DR	Not suitable for low voltage applications
Very low distortion	Large die area

2.2.5 A Low Power Low Noise CMOS Amplifier for Neural Recording Applications:

This bio amplifier is consisting of an OTA and MOS bipolar Pseudo resistor elements. Figure 17 shows schematic of the neural amplifier.

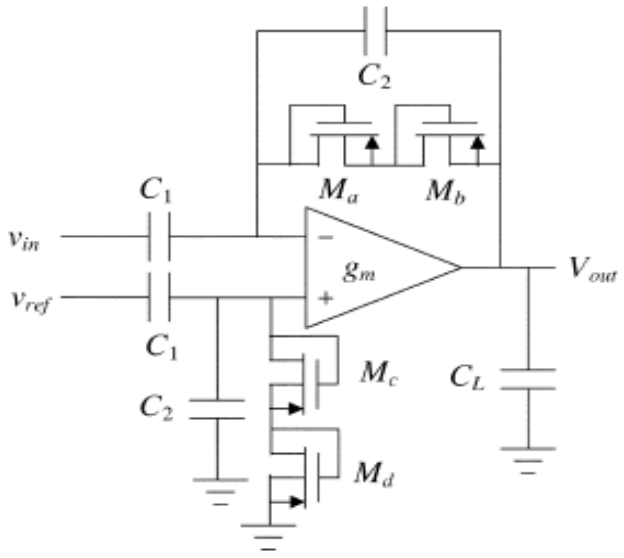


Figure 17: Schematic of neural amplifier [3]

The mid band gain A_M is set by C_1/C_2 and for the case where C_1, C_L»C_2, the bandwidth is approximately $g_m/(A_M C_L)$. Transistors M_a-M_d are acting as Pseudo resistors. This means with negative V_{GS} each device functions as diode connected PMOS transistor and with positive V_{GS}, the parasitic source –well-drain pnp bipolar junction transistor is activated and the device acts as a diode connected BJT [3]. These transistors are used instead of large resistors. For very small voltage values ΔV=0.2 V a resistance of $10^{11}\Omega$ is achievable.

The OTA is designed for low power and low noise circuit while MOS- bipolar are selected to be in series in order to reduce distortion for large output signals [3].The low frequency cut off of the ac-coupled amplifier is $1/2r_{incremental}C_2$.

The proposed design acts as low noise amplifier as well as a reconfigurable band pass filter where the low pass corner frequency is adjusted by changing the bandwidth of the OTA and the high pass corner frequency is controlled by the Pseudo resistors [3].

One of the major concerns for low noise low frequency circuits is flicker noise. This effect has been reduced by using PMOS transistors as input devices and using devices with large gate area.

"Flicker noise in PMOS devices is typically one to two orders of magnitude lower than flicker noise in NMOS transistors as long as $|V_{GS}|$ does not greatly exceed the threshold voltage and flicker noise is inversely proportional to gate area [3]."
Advantages and disadvantages of this method are summarized in table 9.

Table 9: Advantages & disadvantages for neural amplifier

Advantages	Disadvantages
Poly-poly capacitors for maximum linearity	Mid band gain slightly lower than design due to fringing effect
One amplifier contains 0.16mm^2 of silicon area	First order implementation only
Input referred noise 1.2 µV	The feedback network induces DC line drift and distortion of the output signal
Distortion below 1% & THD for input less than 16.7 mV peak to peak	
DR 69 dB	
Low noise & low power	
Suitable for mili hertz to 7 KHz signals	
CMRR & PSRR ≥80 dB	

2.2.6 A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip

In [11] a novel balanced tunable Pseudo resistor structure is introduced for adjustment of high pass corner frequency while the low pass corner frequency is realized by -3 dB of OTA.

The OTA acts as low noise amplifier as well as a reconfigurable band pass filter. In this design the low pass corner frequency is adjusted by changing the bandwidth of OTA where the high pass frequency corner is controlled by the balanced tunable Pseudo resistors.
The schematic of the tunable pseudo resistor is shown in the figure below:

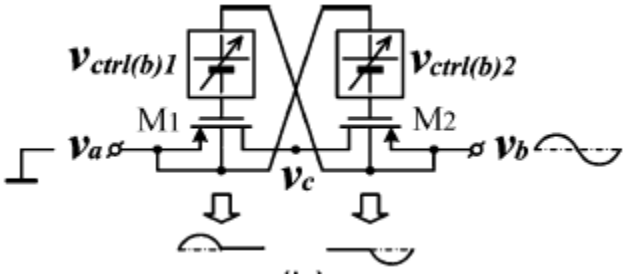


Figure 18: Schematic of the proposed tunable pseudo resistor [11]

As mentioned before the low pass corner frequency is determined by -3 dB cut off frequency of OTA. This can be achieved by either by varying the load capacitance or adjusting the g_m by means of changing the transistor bias current. The proposed design was fabricated in a 0.35 µm standard CMOS process with $V_{thn} + V_{thp} = 1.15$ V where the chip occupies 1 mm^2 silicon area excluding pads. The measurement results are shown in table 10.

Table 10: Measured Performance of the Sensor Interface Chip [11]

Supply Voltage	1V
Process Technology	0.35 µ Process
Current	33~337 nA
Midband Gain	45.6/49/53.5/60 dB
High Pass Corner Frequency	4.5 mHz~3.6 Hz
Low Pass Corner Frequency	31~292 Hz
Input Referred Noise	2.5 μV_{rms} (0.05Hz~460 Hz)
THD @ Full Output Swing	0.6 %
CMRR	≥71.2 dB (Below 300 Hz)
Total Power Consumption	445 nW~895 nW

2.3 Comparison of Methods:

Table 11: Comparison of previously used methods in designing low G_m

Method	Noise	Power	Size	Distortion	Dynamic Range
Capacitive Scaling	250µV	30µW	large	HD3:-75dB	58 dB
Transistor Biased in Linear Region with Current Mirror	high	15µW	small	low	62dB
Current Mirror with Large Division Factor	30µV	Average	$0.5mm^2$	low	High
Low Noise Low Power CMOS Amplifier for Neural Recording	2.2µV	Low	$0.16mm^2$	low	69dB
OTA with Balanced Tunable Pseudo Resistor	2.5 μV_{rms}	445 nW~895 nW	1 mm^2	THD: 0.6 %	

As shown in the table the last two methods provide better results in terms of power and noise. Although the size in balanced tunable may be slightly larger but from power consumption point of view it is superior. Another important factor is the tuning ability which is available in the later technique.

CHAPTER 3

METHODOLOGY

This chapter includes two main sections. In the first part, it will discuss the so called pseudo resistive elements where in the second part it will include a detailed overview of transistors biased in week inversion.

3.1 Pseudo Resistor Elements:

The novelty in these techniques will be the use of pseudo resistors instead of large value resistors. In this case large values of resistors can be achieved with very small die area by utilizing transistors biased in the weak inversion region.

Shi [12] defines pseudo resistor element as a two terminal circuit element whose current is a function of instantaneous difference in the pseudo voltage across the two terminals, where the pseudo voltage is a nonlinear function of the drain and source voltage at each terminal.

A transistor with fixed gate and bulk voltages is a linear pseudo resistor between the drain and source over a wide range of currents including weak inversion.

In order to present a better view of how the pseudo resistors are performing a detailed overview of MOSFET and current in weak inversion is provided.

3.1.1. Drain Current Expression

In [13] the author assumes that gate voltage V_G has increased to a point where an N-channel is formed at the silicon surface from mobile electrons. If the source and drain voltages V_S and V_D are different, electrons of density n_p forming the mobile inverted charge Q_i move by a combination of drift and diffusion, will result in a drain current . The following figure shows the cross section of NMOS.

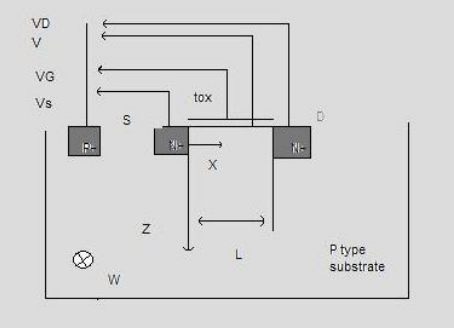


Figure 19: Cross section of NMOS

For a long channel, the flow of current is in the x direction (the position along the channel) with current density is defined as [13]:

$$J_n = \mu q \left(-n_p \frac{d\psi}{dx} + U_T \frac{dn_p}{dx}\right) \tag{26}$$

Where,

μ: Mobility of electron

$-n_p \frac{d\psi}{dx}$ *:* Drift component of the current, proportional to the electric field $-\frac{d\psi}{dx}$

$U_T \frac{dn_p}{dx}$: Diffusion component, proportional to gradient of charge concentration $\frac{dn_p}{dx}$

With charge sheet approximation, integration in the direction of z axis (distance from silicon surface) is obtained by replacing qn_p by $-Q_i$. For a sufficiently wide channel, integration along the y axis (perpendicular to the plane of cross section) is simply a multiplication by W. At the silicon surface, (z=0), ψ becomes the surface potential ψ_s. The drain current becomes:

$$I_D = \mu W \left(-Q_i \frac{d\psi_s}{dx} + U_T \frac{dQ_i}{dx}\right) \tag{27}$$

Since Q_i of electrons is assumed to be concentrated at the surface then [13]

$$Q_i \propto exp \frac{\psi_s - \phi_F - V}{U_T} \tag{28}$$

Therefore,

$$\frac{dQ_i}{dx} = \frac{Q_i}{U_T}\left(\frac{d\psi_s}{dx} - \frac{dV}{dx}\right) \tag{29}$$

Where ϕ_F is the Fermi potential, V is the channel voltage which varies between V_S at x=0 and V_D at x=L. Introducing (29) into (27) yields [13]

$$I_D = \mu W(-Q_i) \tag{30}$$

This expression includes drift and diffusion components and shows that the overall current is proportional to the gradient of the channel voltage.

Since the current is constant along the channel, it can be integrated from source to drain [13]:

$$I_D \int_0^L dx = \int_{V_s}^{V_d} \mu W(-Q_i)\, dV \tag{31}$$

Since only Q_i changes along the channel then (33) becomes [13]

$$I_D = \beta \int_{V_s}^{V_d} \frac{-Q_i}{C_{ox}} dV \tag{32}$$

Where $\beta \triangleq \mu C_{ox} \frac{W}{L}$, (33)

Equation (32) shows that the drain current can be obtained directly from the $Q_i(V)$ as shown in Figure 20.

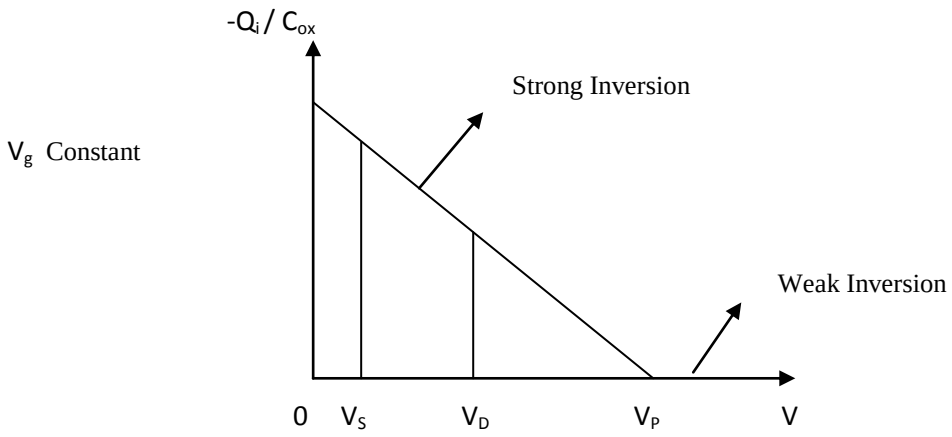


Figure 20: Charge sheet approximation vs. channel voltage [13]

This result demonstrates that the drain current is independent of the shape of $Q_i(V)$ and is valid for all values of the source and drain voltages even values larger that pinch off voltage, where the inverted charge is very small. Since the mobile charge tends to zero for voltage tending to infinity then equation (32) can be rewritten as [13]

$$I_D = \beta \int_{V_S}^{\infty} \frac{-Q_i}{C_{ox}} dv - \beta \int_{V_D}^{\infty} \frac{-Q_i}{C_{ox}} dv = I_F - I_R \tag{34}$$

This equation shows that drain current can be written as the difference between forward current and reverse current. Moreover it shows that the forward current

depends on the gate voltage V_G and V_S but not V_D while reverse current depends on V_G and V_D but not V_S. Therefore the drain current is "the superposition of independent and symmetrical effects of the source and drain voltages." This is shown in the figure below:

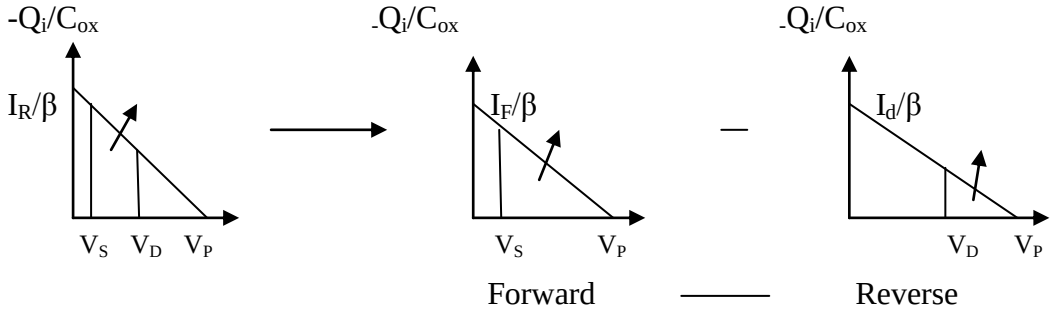


Figure 21: Superposition of independent and symmetrical effects of V_S & V_D [13]

3.1.2. Approximation of the Drain Current in Weak Inversion:

In [13] the inverted charge as a function of channel voltage and surface potential can be approximated as

$$Q_i = Q_{si} - Q_b = -\Gamma_b C_{ox}\sqrt{U_T}\left(\sqrt{\frac{\psi_S}{U_T} + exp\,\frac{\psi_S - 2\Phi_F - V}{U_T}} - \sqrt{\frac{\psi_S}{U_T}}\right) \quad (35)$$

Where Q_{si}: *Semiconductor total charge density*
Q_b: *Depletion charge density*
Γ_b: *Substrate modulation factor*
C_{ox}: *Oxide capacitance per unit area*
U_T: *Thermal voltage*
ψ_S: *Surface potential*
Φ_F:*Fermi potential of silicon substrate*
V: *Channel voltage*

The inverted charge cannot be calculated from this equation, since the surface potential cannot be expressed analytically as a function of the gate voltage. However the linearization of $Q_i(\psi_s)$ by means of constant slope factor can be used to obtain explicit solution. Therefore the surface potential is related to the pinch-off voltage by[13]

$$Q_i = nC_{ox}(\psi_s - \psi_p) \quad (36)$$

ψ_p: *Pinch-off surface potential*

Replacing equation (36) into (35) to eliminate ψ_s results in

$$\frac{\psi_p - 2\Phi_F - V}{U_T} = \frac{-Q_i}{nC_{ox}U_T} + ln\left[\frac{-Q_i}{\Gamma_b C_{ox}\sqrt{U_T}}\left(\frac{-Q_i}{\Gamma_b C_{ox}\sqrt{U_T}} + 2\sqrt{\frac{Q_i}{nC_{ox}U_T} + \frac{\psi_p}{U_T}}\right)\right] \quad (37)$$

This equation demonstrates a general relationship between the density of inverted charge and channel voltage and gate voltage. By normalizing the equation, where $q_i = \frac{Q_i}{Q_{Spec}}$, $v_p = \frac{V_p}{U_T}$, $v = \frac{V}{U_T}$ it can be expressed as [13]

$$2q_i + lnq_i + ln\left[\frac{2n}{\gamma_b}\left(q_i\frac{2n}{\gamma_b} + 2\sqrt{\psi_p - 2q_i}\right)\right] = \psi_p - 2\Phi_f - v \quad (38)$$

The third term of equation can be referred to as voltage shift (v_{sh}).This equation is valid only for $\psi_p \gg 2q_i$. Since variation of v_{sh} with q_i never exceeds unity, q_i can be neglected. Therefore the equation simplifies to [13]

$$2q_i + lnq_i + ln\left(\frac{4n}{\gamma_b}\sqrt{\psi_p}\right) = \psi_p - 2\Phi_f - v \quad (39)$$

The inversion charge can be related to particular value of channel voltage called pinch-off voltage V_p. This is defined by [13]

$$v_p \triangleq \frac{V_P}{U_T} \triangleq v(2q_i + lnq_i = 0) \quad (40)$$

$$v_p = \psi_p - \left(2\Phi_f + v_{sh}\right) \quad (41)$$

Introducing this definition in (39) results in

$$2q_i + lnq_i = v_p - v \quad (42)$$

In weak inversion $q_i \ll 1$; therefore the linear term becomes negligible and q_i is defined as [13]

$$q_i = exp(v_P - v) \quad (43)$$

The corresponding forward and reverse components of drain current are derived from the following integral [13]

$$i_{f,r} = \int_{v_s}^{v_d} q_i dv \quad (44)$$

The normalized and non-normalized current equations are as follow [13]

$$i_d = exp(v_P - v_{s,d}) \tag{45}$$

$$I_{F,D} = I_{SPEC} exp \frac{V_P - V_{S,D}}{U_T} \tag{46}$$

By substituting V_P approximation in (46), the drain current will be defined as follow [13]:

$$I_D = I_{SPEC} exp \frac{V_G - V_{T0}}{nU_T} \left(exp \frac{-V_S}{U_T} - exp \frac{-V_D}{U_T} \right) \tag{47}$$

Where

$$I_{SPEC} \triangleq \mu U_T \frac{W}{L} (-Q_{SPEC}) = 2n\mu C_{ox} \frac{W}{L} U_T^2 = 2n\beta U_T^2 \tag{48}$$

Equation (47) shows that drain current is an exponential function of gate, source and drain voltages. In weak inversion, the current components decrease exponentially with V_S/U_T and V_D/U_T. This mode of operation is achieved for gate voltages below threshold voltage, so the pinch off voltage becomes negative and weak inversion is already reached for $V_S = 0$.

For $V_G = 0$, the transistor will act as a reverse biased PN junction. The reason is that the transistor itself is composed of two back to back diodes where by applying V_D one will be a reversed PN junction and by imposing zero volts for gate and source they will be shorted to the ground. In this case the current will be due to the leakage current.

If $V_G=V_S=0$, the saturation current (I_F in forward mode where it's dependant on V_S) is reduced to

$$I_{D0} = I_{SPEC} exp \frac{-V_{T0}}{nU_T} \tag{49}$$

As mentioned earlier for small values of gate voltage that are below the threshold voltage the transistor is operating in weak inversion. If one assumes an NMOS transistor with source and bulk connected to the ground ,V_D= 3.3 V and V_G = 0.1 V then there is no voltage applied to bulk and source PN junction. The diffusion of holes and electrons must eventually cease. The direction of induced electric field will cause the resulting force to repel the diffusion of holes from the P region and diffusion of electrons from the N region. This positively charged region and negatively charged

region compromise the depletion region where there is no mobile electrons and holes. However due to electric filed there is a potential difference across the region. In other words the source and the bulk are shorted to the ground.

With a positive voltage connected to drain terminal, the bulk and drain PN junction will be reversed. The current in the reversed PN junction is as follow:

$$i_d = I_S \left[exp^{\frac{v_D}{nU_T}} - 1 \right] \tag{50}$$

By applying a positive voltage to the gate the magnitude of the induced electric filed increases. Minority carrier electrons are attracted to the oxide semiconductor interface. This region of minority carrier electrons is the electron inversion layer where here is called the weak inversion due to small gate voltage below the threshold. The magnitude of the charge in the inversion layer is a function of the applied gate voltage. Therefore the overall current in this situation for a NMOS will be

$$I_D = I_{SPEC} exp \frac{V_G - V_{T0}}{nU_T} \left(1 - exp \frac{-V_D}{U_T} \right) \tag{51}$$

3.1.3. Transistors Operated as Pseudo Resistors:

Linear resistors are very area consuming in IC circuit designs. Equivalent resistors can be implemented by means of transistors while the corresponding range of linearity is limited.

Based on equation (47) drain current in weak inversion is in linear relationship with exponential voltages. Therefore a pseudo voltage can be defined as [13]

$$V^*_{A,B} = \pm V_0 exp \frac{-V_{A,B}}{U_T} \tag{52}$$

Where, $V_{A, B}$ corresponds to $V_{D, S}$ and V_0 is any positive constant voltage. Following the Ohms law, by dividing current and voltage, the pseudo conductance is defined as

$$G^* = \frac{1}{R^*} = \frac{I_{SPEC}}{V_0} exp \frac{V_G - V_{T0}}{nU_T} \tag{53}$$

Substituting (52) and (53) in (47), will result in pseudo ohms law.

$$I_{AB} = G^*(V_A^* - V_B^*) = \frac{(V_A^* - V_B^*)}{R^*} \quad (54)$$

Therefore any linear resistor may be converted to a pseudo resistor network made of transistors only, by replacing each resistor by the source and drain of a transistor. Each pseudo resistance value is controlled by the gate voltage of the transistor according to (53). Although this principle is also valid in moderate and strong inversion, but then the gate voltage must be identical for all transistors. Therefore the possibility to control the resistance by the gate voltage only exists in weak inversion. The current in a pseudo resistor is a function of the potentials at the two terminals (pseudo voltages).

Fig. 22 shows the bias scheme the so called gate voltage biasing to bias up the pseudo resistor. In the voltage bias scheme, a single n-FET or a single p-FET or a series combination of an n-FET and a p-FET can be replaced for a better linearity [11].

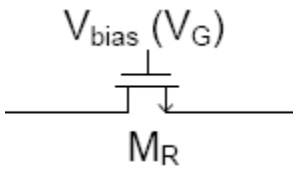


Fig 22: Biasing scheme for pseudo resistor

The drawback of the gate voltage biased pseudo resistor is that its effective resistance is hard to control. Assuming the drain-to-source voltage equals zero, the effective resistance is exponentially dependent on its gate voltage in weak inversion region.

3.2. Gate Voltage Biased Tunable Pseudo Resistor:

In the first attempt, gate voltage biased single tunable pseudo resistor is used to compare the results in the filter design with that of double tunable pseudo resistor.

The schematic of a single tunable pseudo resistor is shown as of the following:

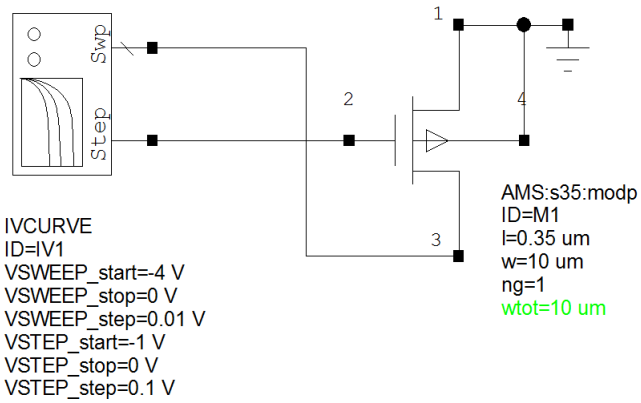


Figure 23: Single tunable transistor pseudo resistor

Figure 24 shows PMOS current voltage characteristics for negative gate voltages while V_{DS} has been swept from -4 V to 0 V.

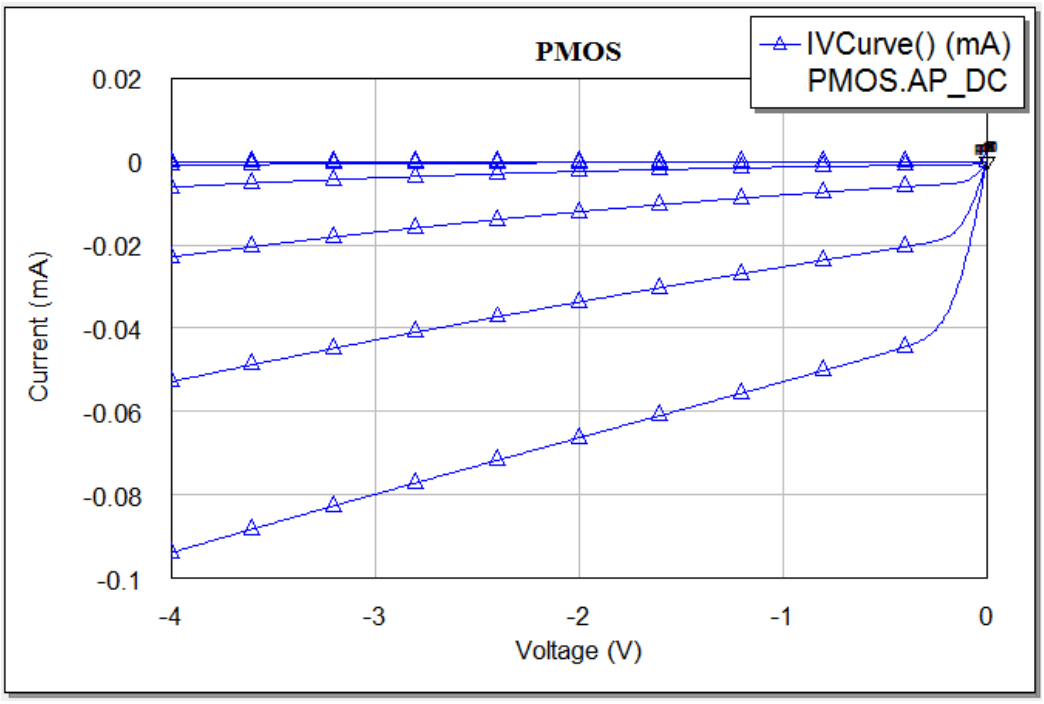


Figure 24: IV characteristics of single tunable pseudo resistor

As mentioned above in the first approach the so called single tunable pseudo resistor large values of resistors are achievable for small gate voltages below threshold value

where the PMOS is biased in weak inversion. Therefore the gate voltage is tuned so that the desired resistor values are achieved. Since this is used in the design of filters the gate voltages are tuned so that the desired cut off frequency is obtained. Figure 25 demonstrates the result of a single tunable pseudo resistor for V_G = -0.4 V where V_{DS} is swept from -1 to 0.

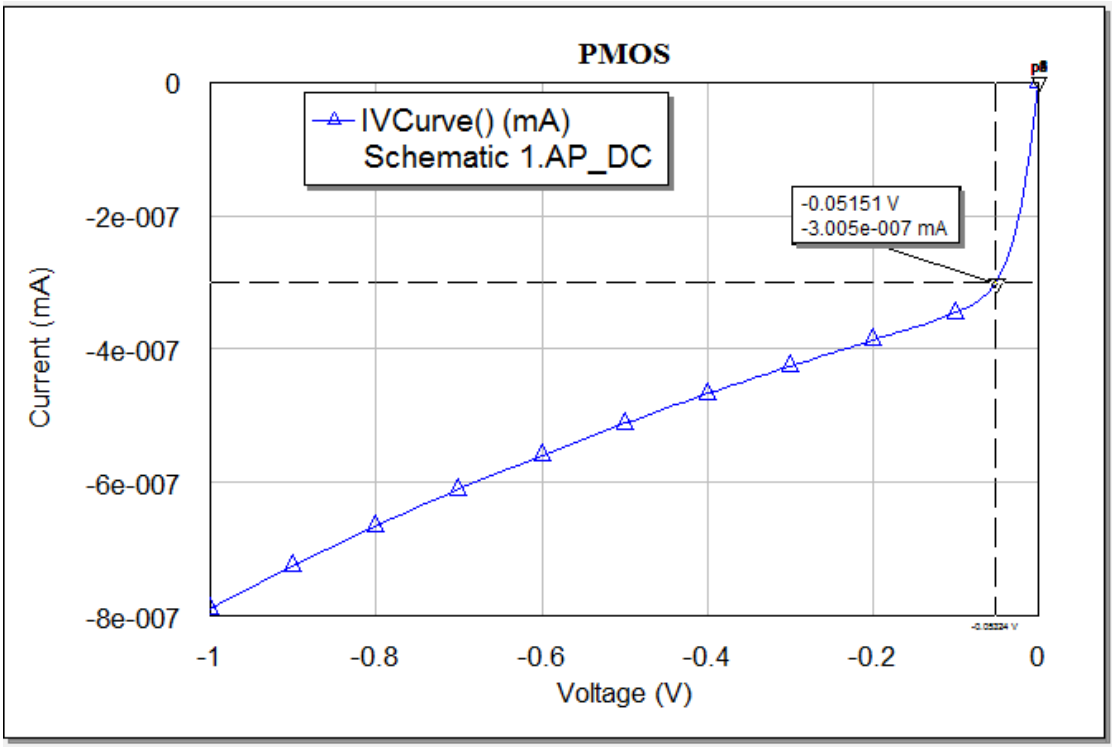


Figure 25: IV characteristics of single tunable pseudo resistor for V_G=-0.4V

As it's illustrated on the graph, small values of voltages and currents correspond to large values of resistors in range of 0.1GΩ. The drain current saturates to its forward value as soon as V_S-V_D > 2U $_T$ to 3U $_T$. In this case the transistor is saturated and the drain current is independent of the drain voltage, so the transistor can be modeled as a current source. However for values less that 3U $_T$ the drain current is strongly dependant on drain voltage and the transistor acts as pseudo resistor.

Moreover it shows that for very small changes in the voltage the resistance values changes in magnitude.

The following graph shows the behavior of the single tunable pseudo resistor over an expanded and zoomed -in voltage range where the gate voltage is swept from -0.41 V to 0 for V_{DS} = -0.01 to 0.01 V.

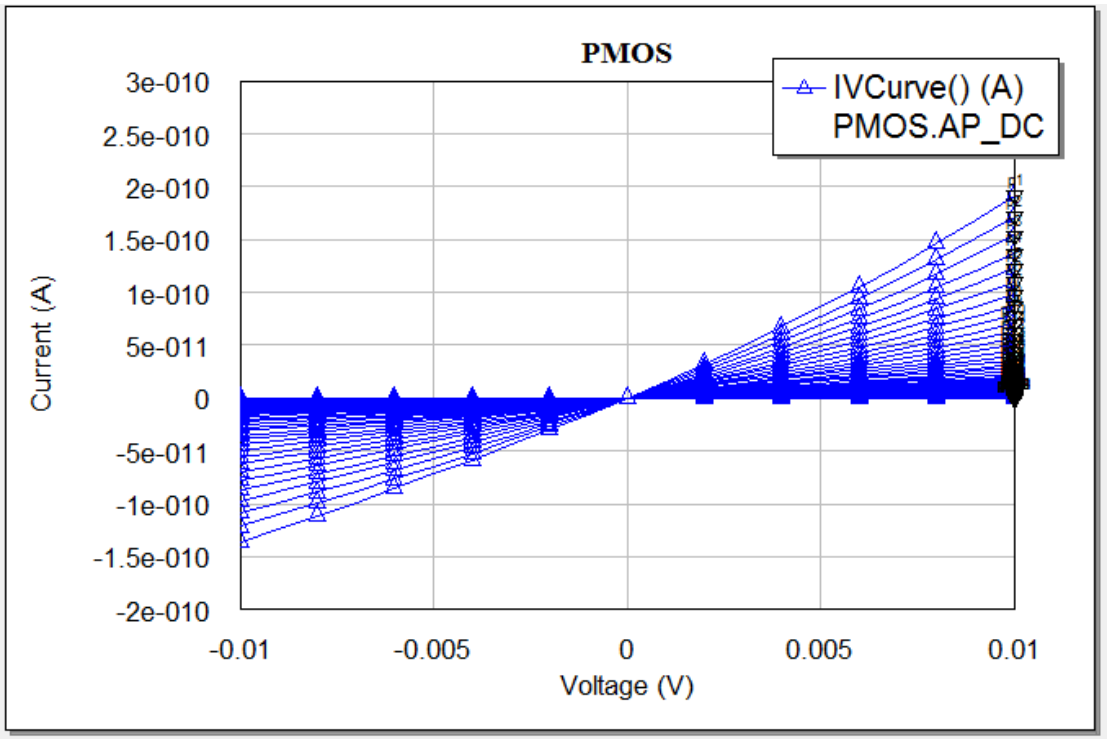


Figure 26: Linear region of a single tunable pseudo resistor

This V_{DS} range of linearity is what's expected from the input signal that is coming to the filter since the ECG signal has been amplified by very small gain in order to have the signals in range of tens of µV to mVs.

Keeping the V_{DS} swept from negative to positive voltage values is shown in graph 27.

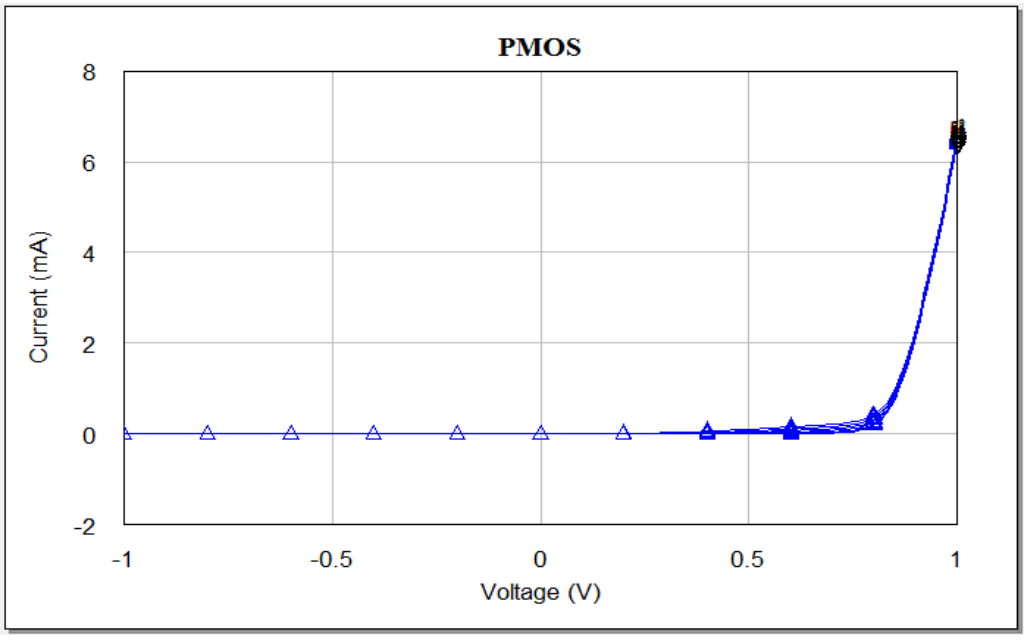


Figure 27: IV characteristics of single tunable pseudo resistor sweeping up to positive V_{SD}

The graph illustrates high non-linearity for positive voltage values. This is clearer if the gate is fixed at a specific voltage, for example -0.4 V as in the previous case .This is shown in plot 28.

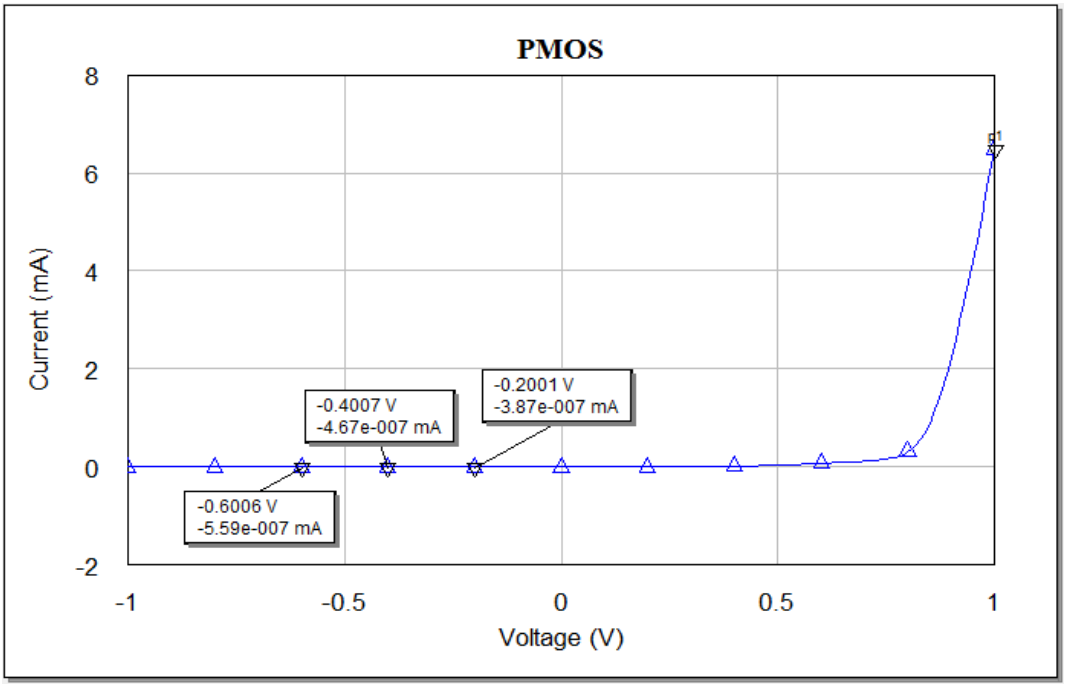


Figure 28: IV characteristics of single tunable pseudo resistor swiping up to positive V_{SD} & V_G=-0.4V

This high non- linearity is starting at around V_{SD} = 0.4 V. Therefore this design gives more consistent results for negative voltage values.

A pseudo resistor can also be obtained by using a saturated transistor where gate to source voltage is equal to drain to source voltage and both are smaller than thermal voltage of 26 mV. ($V_{GS} = V_{DS} < U_T$).

In this case the resistance will be a very high as shown in the following graph:

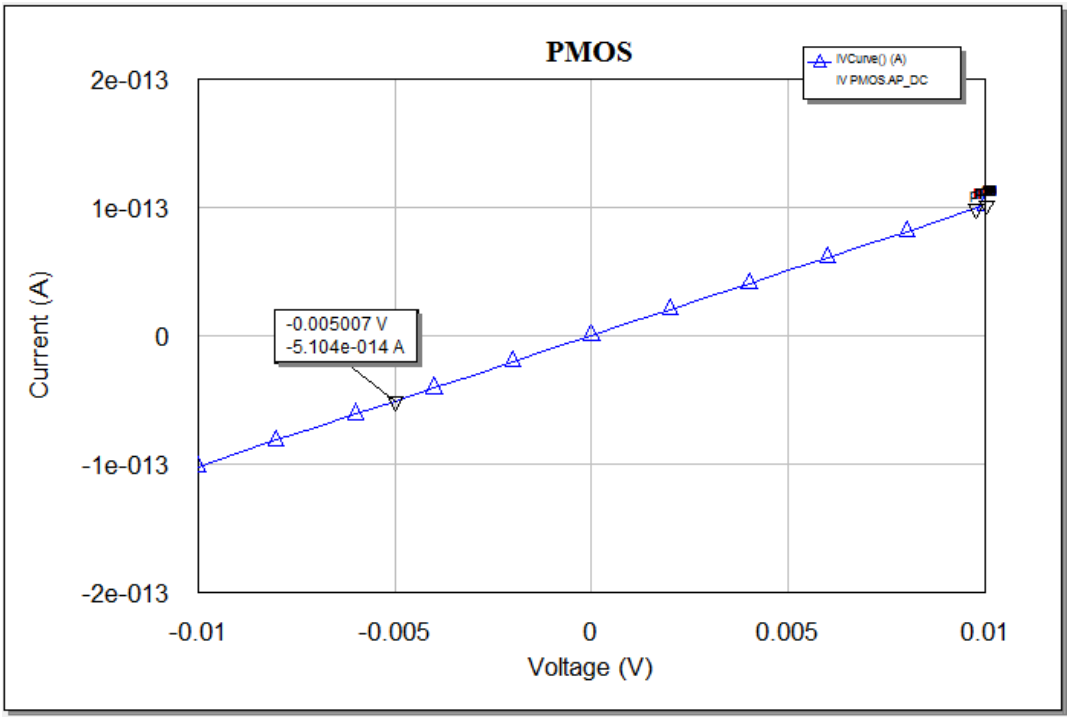


Figure 29: Linear region of a pseudo resistor where $V_{GS} = V_{DS} < U_T$

Based on Figure 29, the value of resistor is in range of 100 GΩ, which is much larger than the gate biased pseudo resistor.

In the next approach two identical PMOS are used in order to increase the resistance and linearity of the circuit. The schematic is shown below:

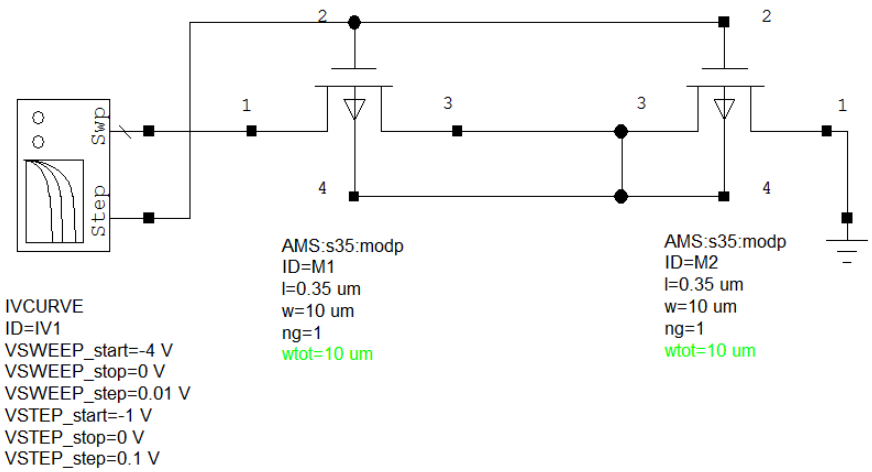


Figure 30: Schematic of double tunable pseudo resistor

The current voltage characteristics of the double tunable pseudo resistor are shown in the next figure :

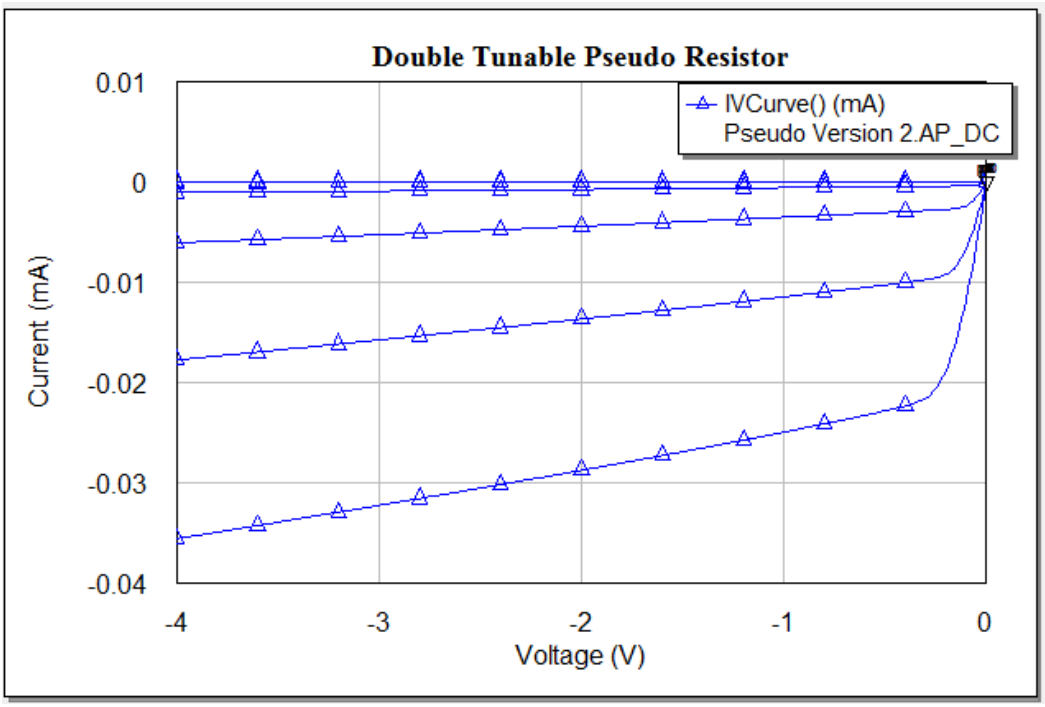


Figure 31: IV characteristics of double tunable pseudo resistor

Here the total V_{DS} has been swept from -4 V to 0 V for negative gate voltages. By fixing the gate voltage at a specific value like -0.4 V as in the single pseudo resistor approach one can clearly notice the difference in the two approaches in terms of resistance values. This is shown in the next graph:

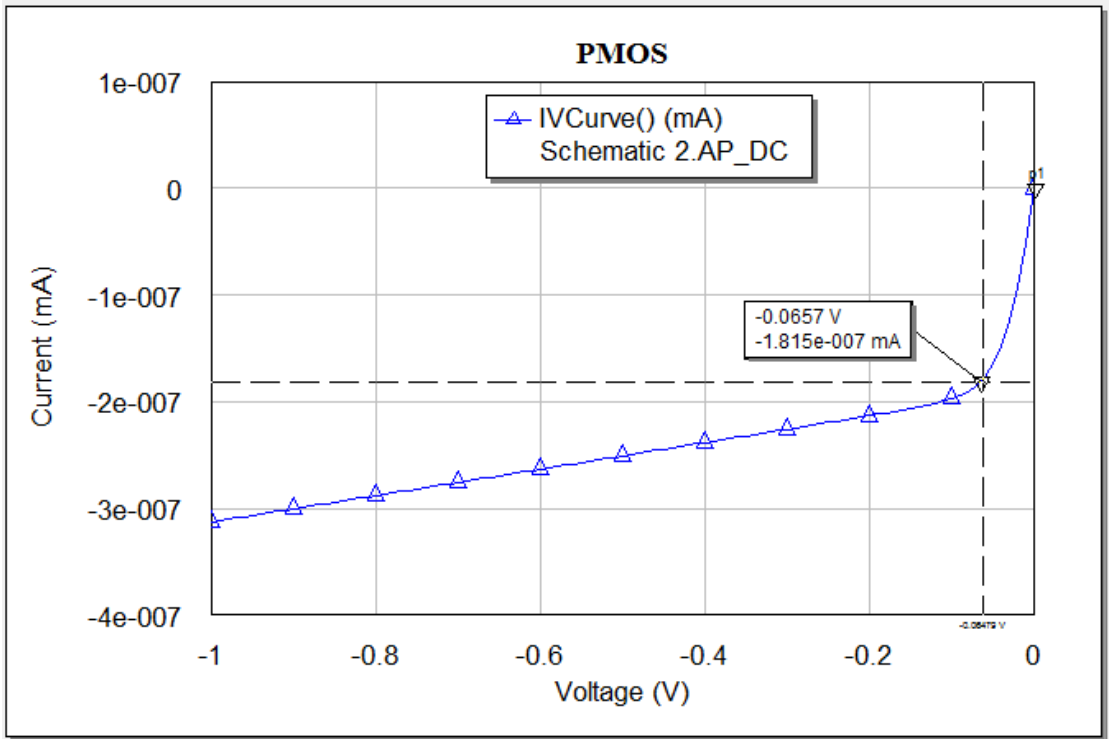


Figure 32: IV characteristics of double tunable pseudo resistor for V_G=-0.4V

The following graph shows the behavior of the double tunable pseudo resistor over an expanded and zoomed -in voltage range where the gate voltage is swept from -0.41 V to 0 for V_{DS} = -0.01 to 0.01 V.

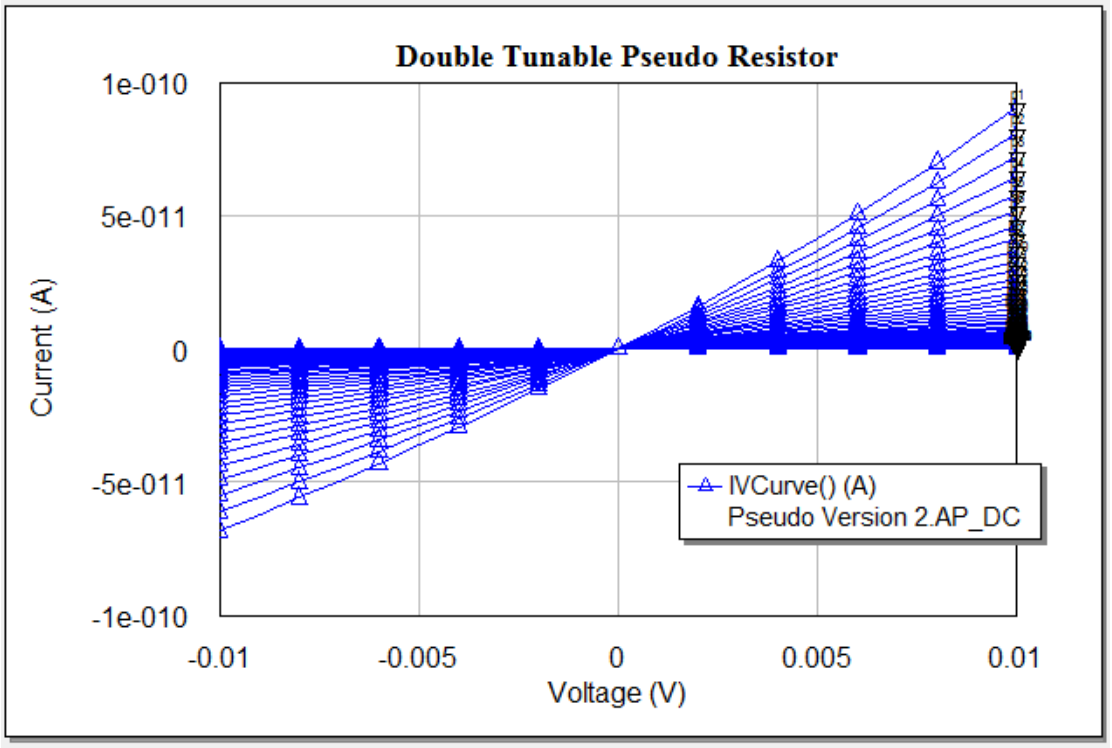


Figure 33: Linear region of double tunable pseudo resistor

By comparing figure (26) with figure (33) it is clear that the linear range that is used as pseudo resistor is greater in double tunable pseudo resistor than in single tunable pseudo resistor. Moreover, for the same values of voltages provided, different values of current are shown which result in various resistor quantities. The following graph compares the resistance of single and double tunable pseudo resistors.

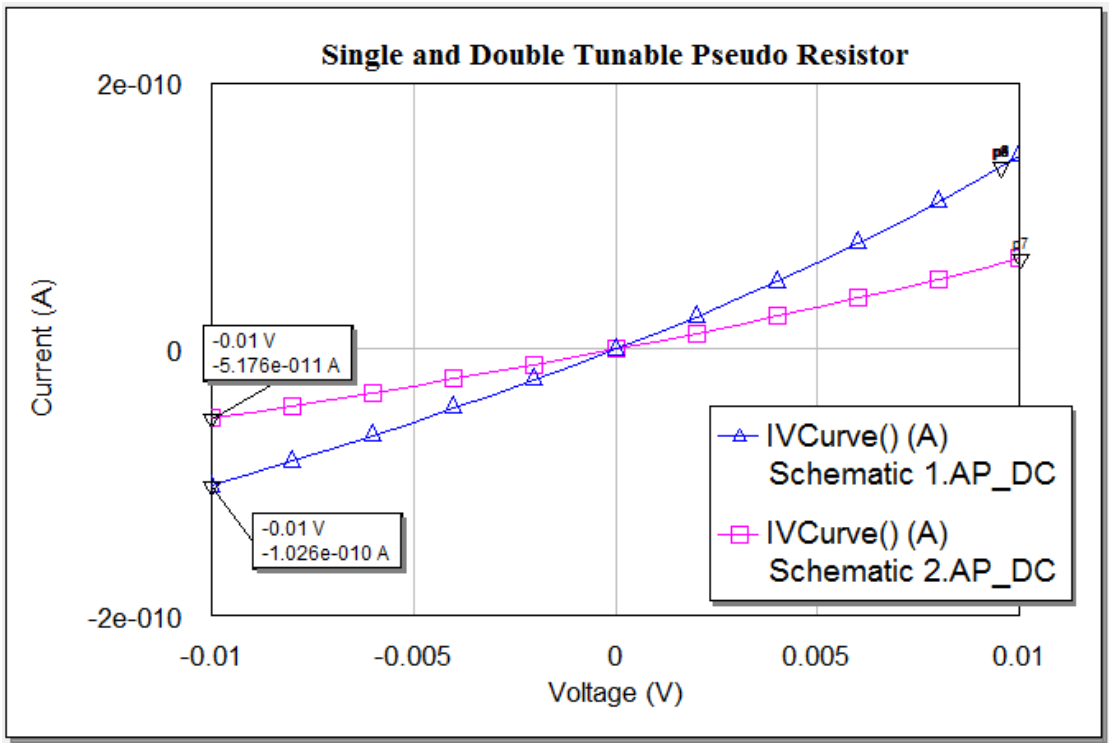


Figure 34: IV characteristics of single and double tunable pseudo resistor for V_G=-0.4V

As shown in graph 34 the same amount of voltage corresponds to different current values where in result the resistor values are different. For example in double tunable pseudo resistor, V_{DS} = -0.01 V , I_D = -5.176e^{-11} A → R = 0.193 GΩ Where in single tunable pseudo resistor, V_{DS} = -0.01 V , I_D = -1.026e^{-10} A → R = 0.097 GΩ .This result shows that at a fixed gate voltage the same amount of V_{DS} provides higher resistance in double tunable pseudo resistor than in single tunable .

Keeping the V_{DS} swept from negative to positive voltage values create high non-linearity in positive voltages approximately starting at around 0.1 V. Therefore this design presents more consistent results for negative voltage values. This is shown in the following graphs for several values of gate voltages and fixed gate value of -0.4 V respectively. As a result ,in double tunable pseudo resistors the non-linearity range starts to show its effects earlier than in single tunable resistor, but the resistance values at the same gate voltage will be higher in the double tunable pseudo resistor.

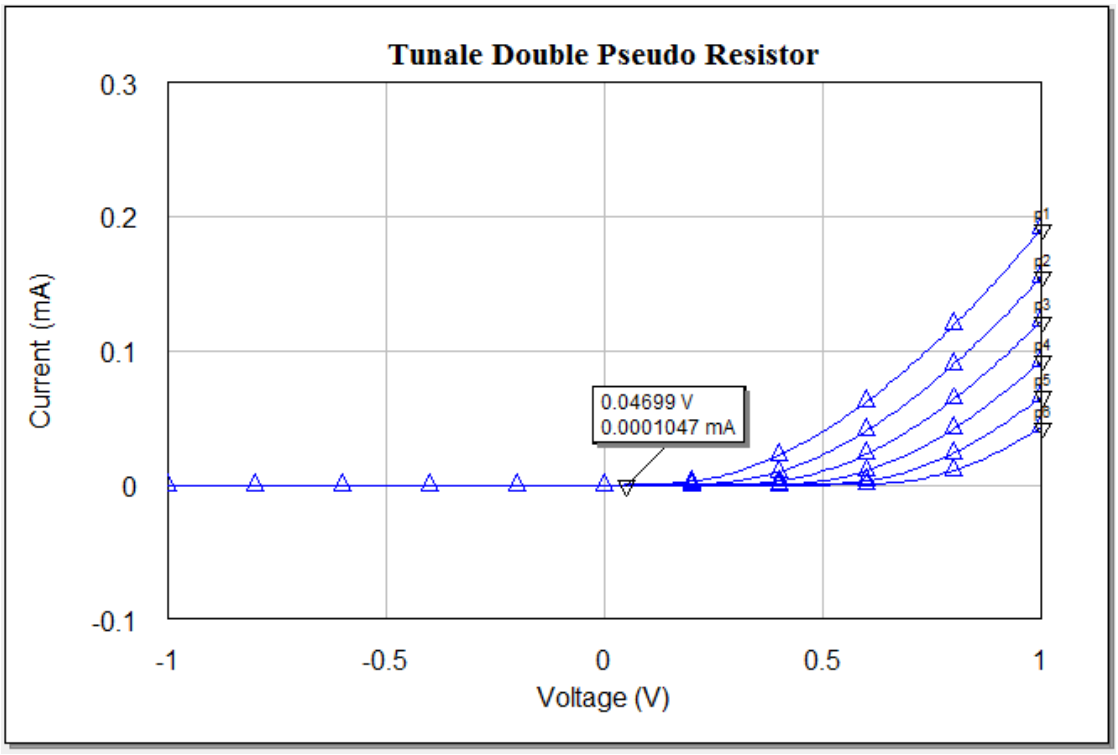


Figure 35: IV characteristics of double tunable pseudo resistor sweeping up to positive V_{SD}

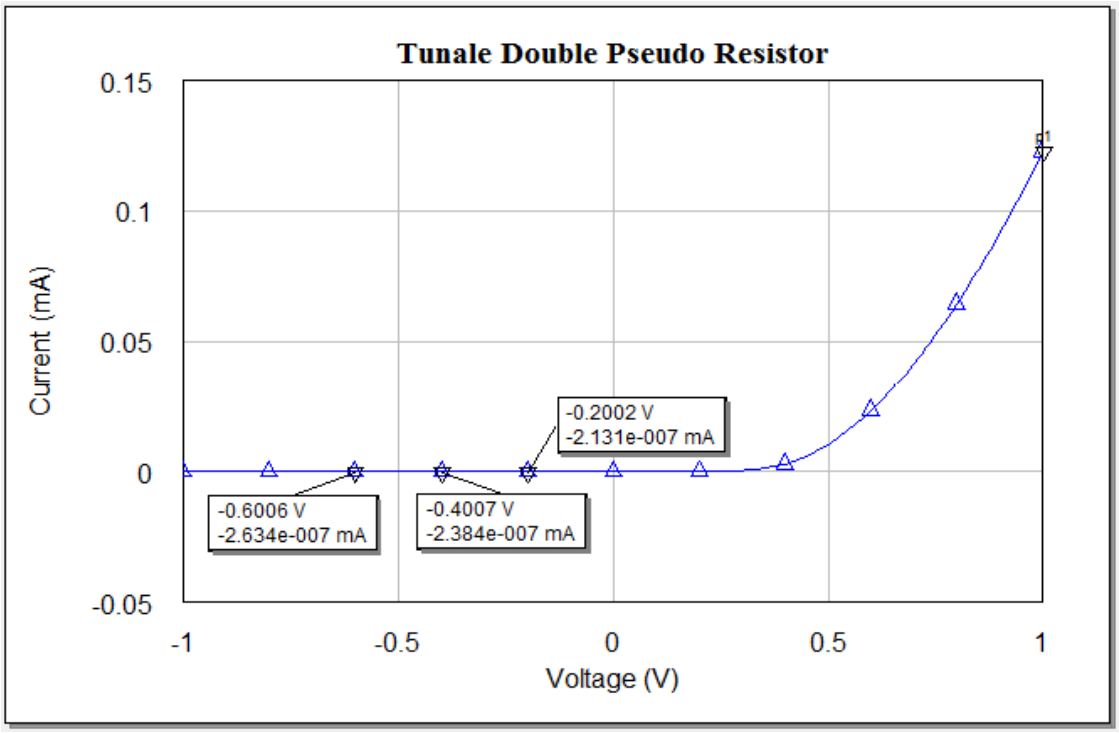


Figure 36: IV characteristics of double tunable pseudo resistor sweeping up to positive V_{SD} & V_G=-0.4V

CHAPTER 4

RESULTS ANALYSIS AND SIMULATION

In this chapter, design and results of low pass (LP) and high pass (HP) filters using both single tunable pseudo resistor and double tunable pseudo resistor is described. Next the DC biasing voltage of the pseudo resistors will be replaced by a set of transistors to compare the results. The ideal capacitor and resistor values will be substituted by their AMS counterparts to illustrate the difference in the filter performance. Finally a comparison table for different cut off frequencies with their corresponding biasing voltages will be provided. Linearity, Noise and power consumption of pseudo resistor elements will be simulated.

4.1. Low Pass and High Pass Filter Designs:

In this work, the electrocardiograph signal is of prime concern. Hence, a third order Butterworth filter is utilized. The Butterworth model is selected because it gives maximally flat pass band filter. Since an ECG signal is of interest, the fidelity and morphology of the sharp QRS spike must be preserved for diagnosis. There must be little rounding of R peak and no transient "ringing" following QRS spike. The Butterworth or Bessel are classes of analog filters that are free from ringing and suitable for conditioning ECG signals [4].

The Sallen and Key topology is tested for both the third order Butterworth LPF and HPF.

In a Sallen and Key topology, an odd order filter is realized by using multiples of second order LPF with an additional pole [14]. However for more simplicity of the design and significantly the smaller chip area, a unity gain Sallen and Key with equal value of resistors is developed. At low frequencies, where capacitors appear as open circuits, the signal is simply buffered to the output. At high frequencies where capacitors appear as short circuits, the signal is shunted to the ground at the

amplifier's input and the signal doesn't appear at the output [14]. On the other hand, in the HPF at low frequencies the capacitors will act as open circuits and the signal cannot go through and appear at the output while at high frequencies capacitors will act as short circuits so that the signal is simply buffered to the output.

The following circuit shows a third order Butterworth Sallen and Key LPF [15]. All the OP-AMPs used throughout the design are ideal block elements.

The port parameters are chosen such that they match the input and output characteristics of the operational amplifier (op-amp).

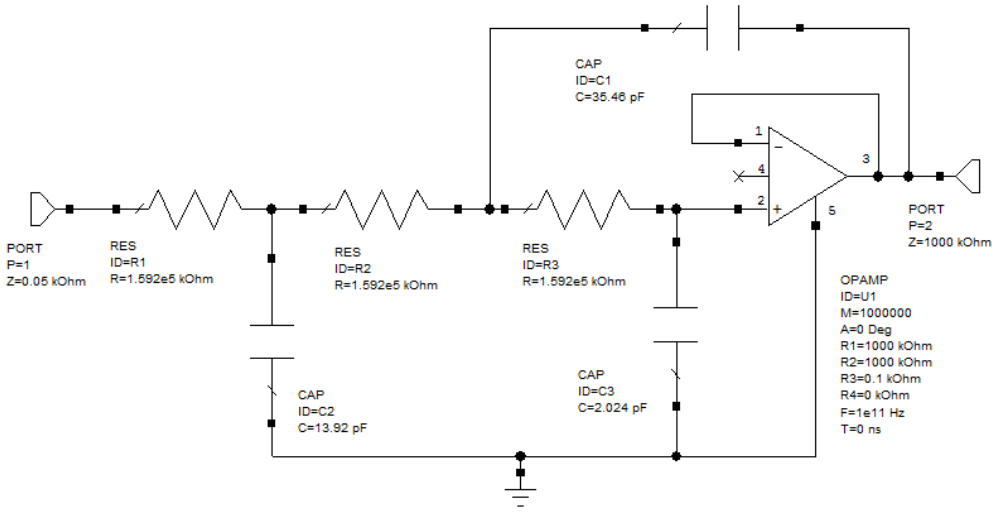


Figure 37: Third Order Butterworth Sallen and Key LPF

The component value calculations are covered in Appendix A. Following the same procedure as LPF, one can design a unity gain HPF with equal values of capacitors and different resistor sizes. However for simplicity of the design, equal values of resistors and capacitors are considered where the gain of op amp would be 2 or 6 dB. The most important reason in choosing equal values for components will be revealed in the design of HPF using concept of Pseudo resistors. Based on the tables available for Butterworth Sallen and Key HPF, the existing Q value for a third order filter is 1 [16].

Reference to general Sallen and Key design as shown below, the gain is given by

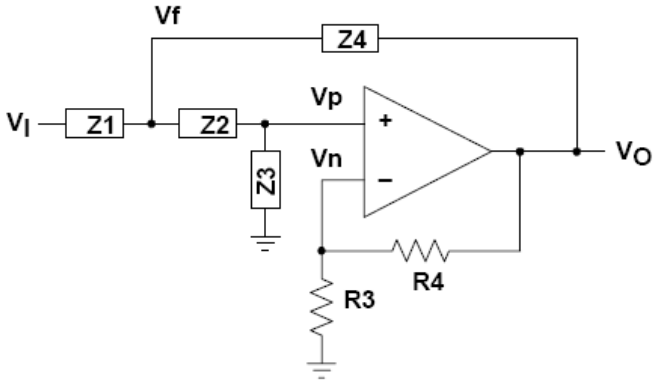


Figure 38: Generalized Sallen Key Schematic

$$K = 1 + \frac{R_4}{R_3} \tag{55}$$

$$Q = \frac{1}{3-K} \tag{56}$$

For a third order Butterworth Sallen and Key, the quality factor Q would be equal to 1 and the gain is 2 (6 dB). Assuming the normalized value $R_4 = 1\Omega$, R_3 would be 1 Ω as well.

The following circuit shows a third order Butterworth Sallen and Key HPF [15].

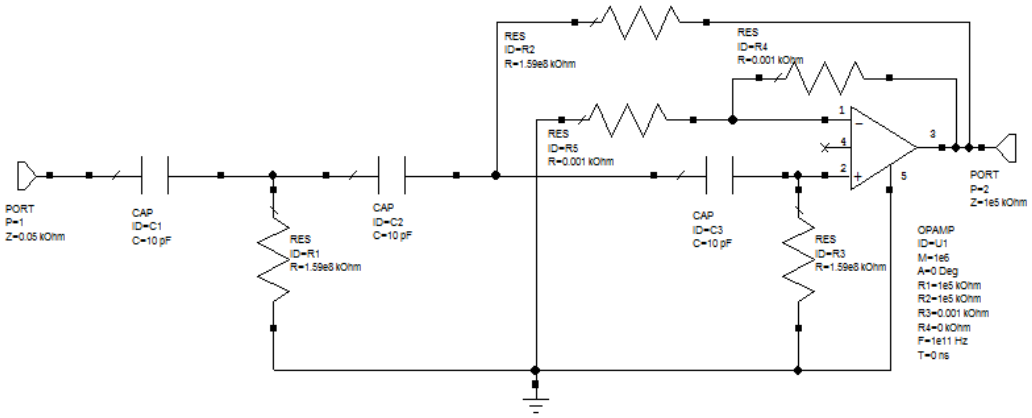


Figure 39: Third Order Butterworth Sallen and Key HPF

The graphs for these two filters are shown respectively.

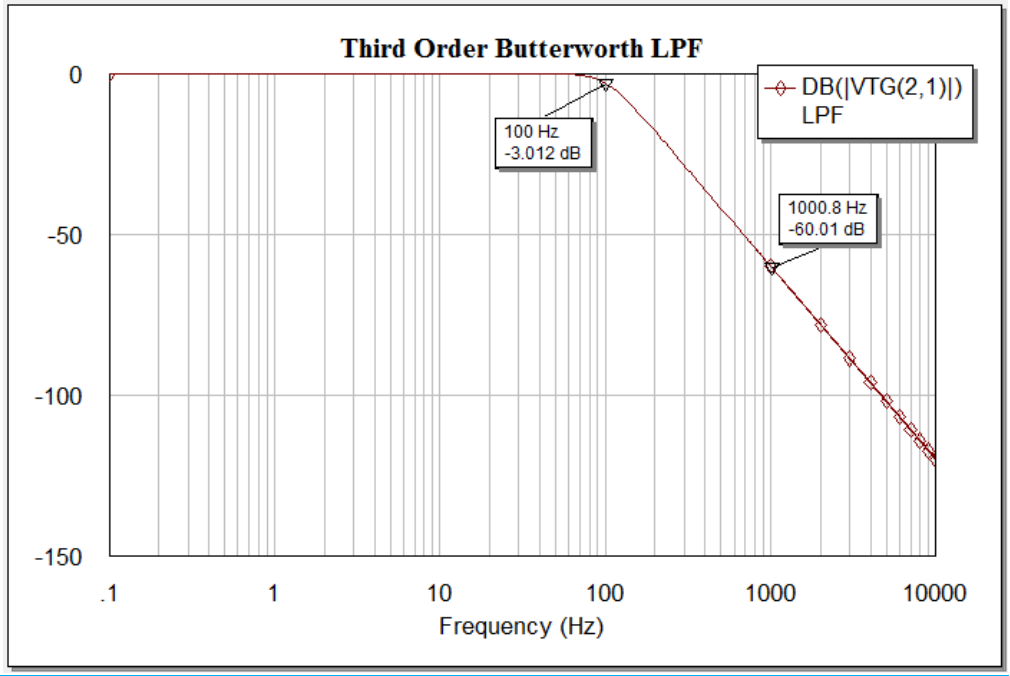


Figure 40: Third Order Butterworth Sallen and Key LPF with C_f=100 Hz

As it's shown from the graph, the maximum gain is unity (0 dB) and the -3 dB shows 100 Hz cut off frequency. Because it's a third order the roll off at -60 dB is 1000 Hz. The following graph shows the HPF. Since the gain in this case is 2 (6 dB), the -3 dB cut off frequency of 0.1 Hz will occur at 3dB and accordingly the role off is at -60 dB of the maximum gain ; where in this case is -54 dB at 0.01 Hz.

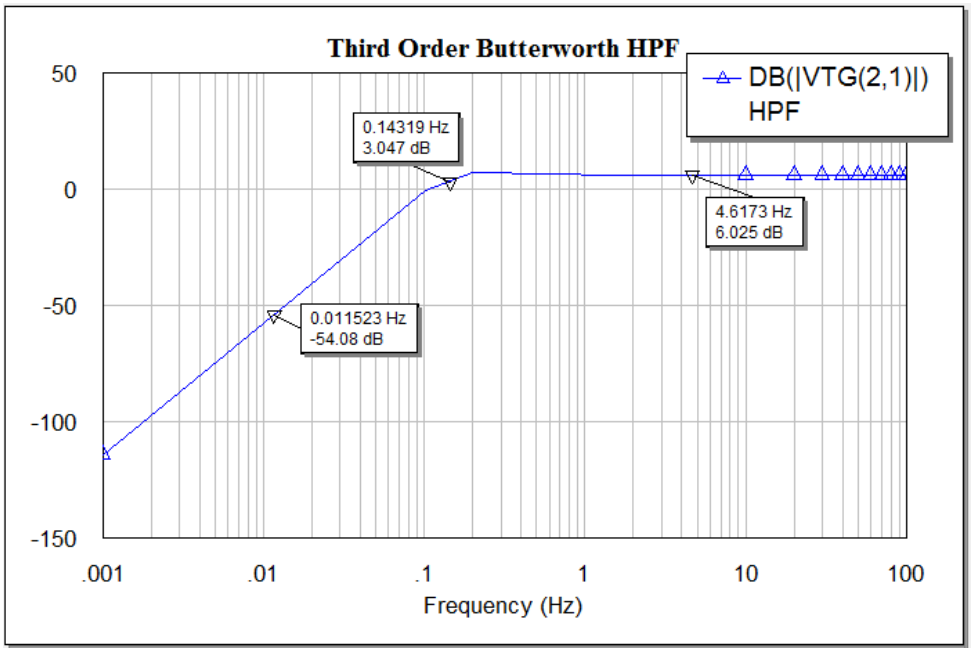


Figure 41: Third Order Butterworth Salen Key HPF with f_c=0.1 Hz

4.2. LPF and HPF Using Single Tunable Pseudo Resistor:

As the first approach in the design of a LPF with cut off frequency of 100 Hz using single tunable pseudo resistor, not only the third order but also the first and second orders are considered so that it can provide a strong and detailed understanding of employing pseudo resistors.

As previously mentioned the unity gain Sallen and Key approach is implemented for low pass filtering. In this design, the single tunable pseudo resistor is a PMOS transistor, AMS 0.35µ process in AWR software, which corresponds to a real transistor. The reason behind choosing PMOS rather than NMOS is due to lower flicker noise. Flicker noise will be discussed in section 4.6.

The following schematic shows the first order LPF. The desired cut off frequency is achieved by tuning the gate voltage of the transistor to reach 100 Hz cut off frequency.

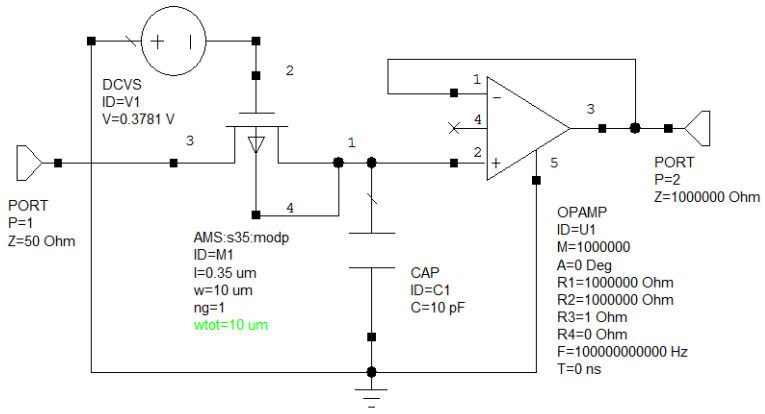


Figure 42: Schematic of first order LPF using single tunable pseudo resistor

In this design the capacitor value is assumed to be 10 pF. Therefore the resistance provided from single tunable pseudo resistor for 100 Hz cut off frequency is 0.159 GΩ. The result is shown in the following graph so that the 100 Hz cut off appears at –3dB.

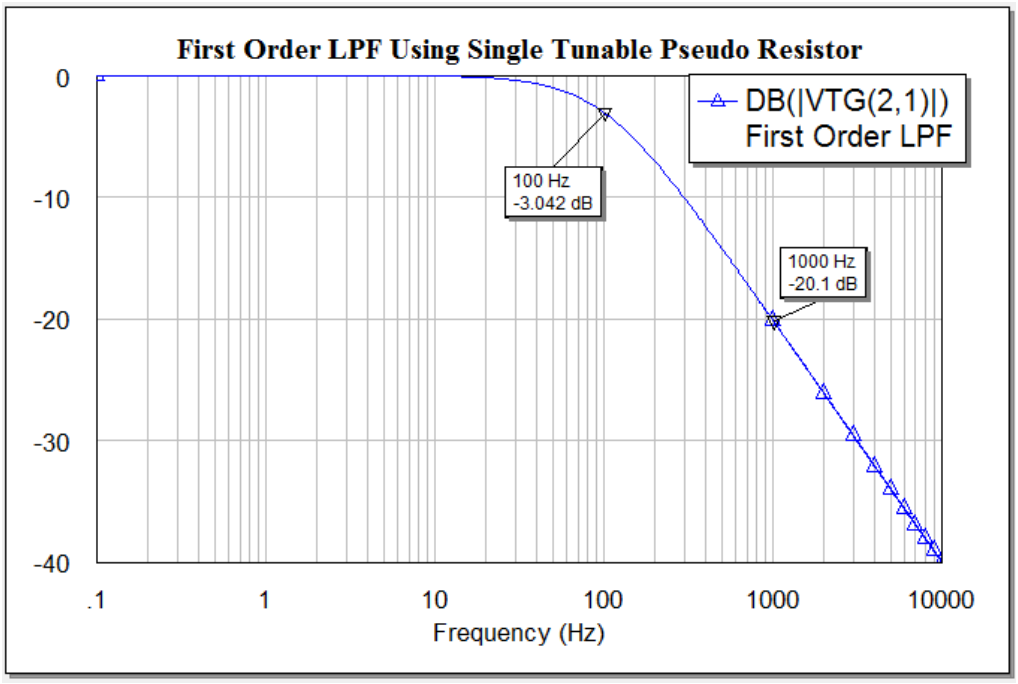


Figure 43: First order LPF using single tunable pseudo resistor

The same procedure has been repeated for the second and third order LPF using single tunable pseudo resistor. As shown in the schematics for the same value of cut off frequency, the same gate voltage V_G = -0.378 V is used to achieve equal values of resistors. The schematics are shown below respectively.

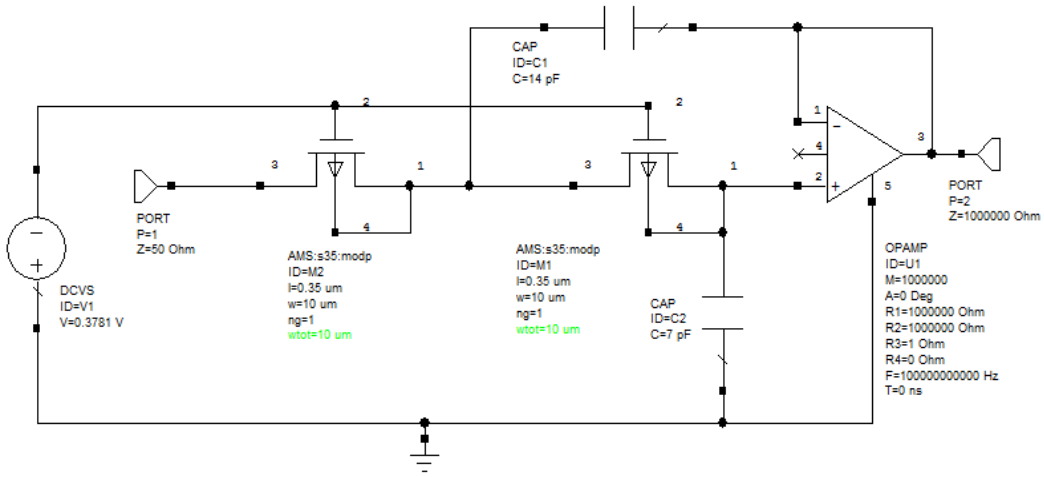


Figure 44: Schematic of second order LPF using single tunable pseudo resistor

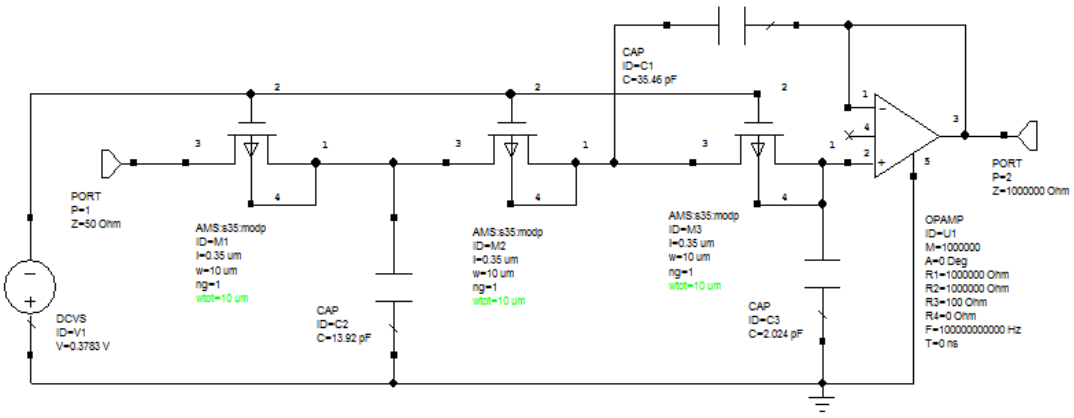


Figure 45: Schematic of the third order LPF using single tunable pseudo resistor

In both second and third order LPF, the exact cut off frequencies are achieved. Thus in the second order 100 Hz is at -3 dB and the roll off at -40 dB is 1000 Hz where the same cut off frequency in third order will have the roll off of -60 dB at 1000 Hz. These are shown in the next two graphs.

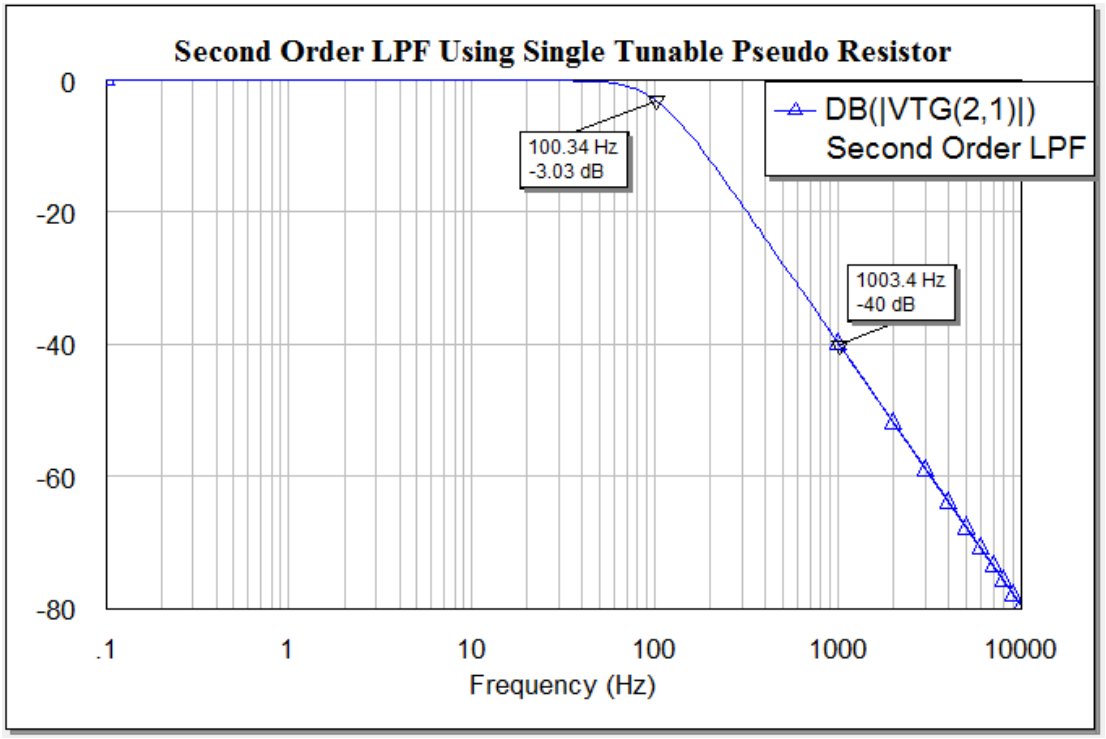


Figure 46: Second order LPF using single tunable pseudo resistor

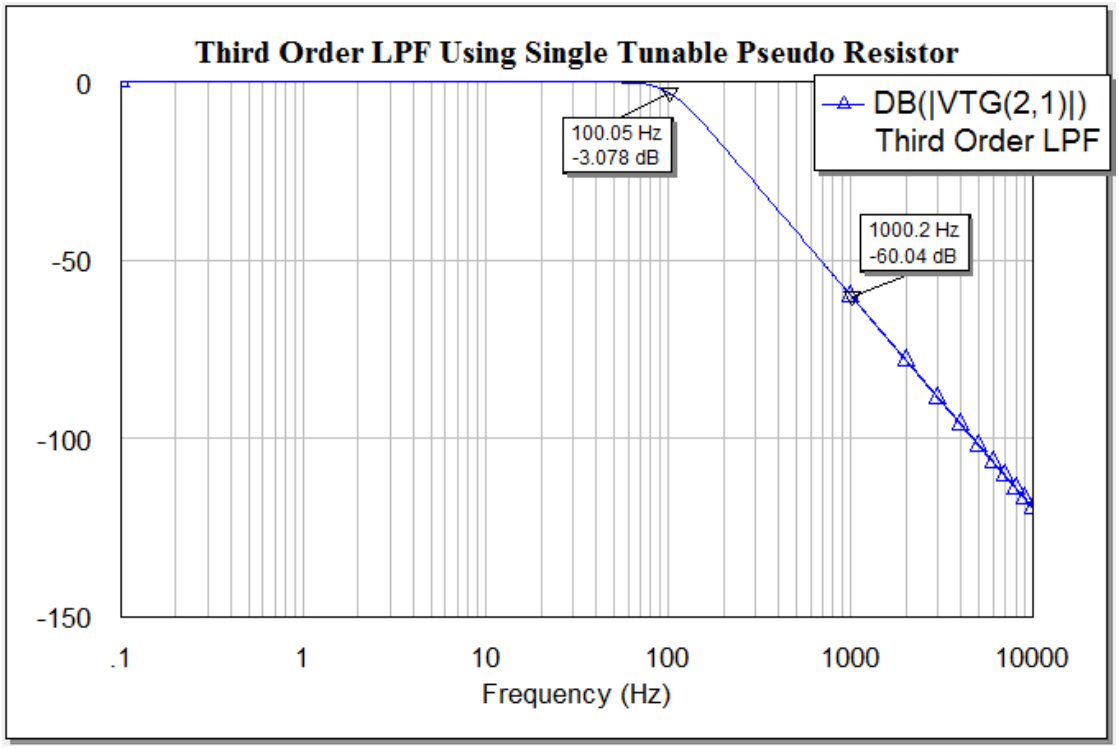


Figure 47: Third order LPF single tunable pseudo resistor

In design of HPF using single tunable pseudo resistor, equal values of capacitors and resistors are used. The main reason is due to biasing the pseudo resistors. As noticed, the tuning of gate voltage is what decides the cut off frequency and, as the result, the resistance of the circuit. One important issue in this design and also double tunable pseudo resistor approach is that very small changes in the gate voltage will result in huge changes in frequency; therefore it is a highly sensitive circuit. For that reason in order to reduce this sensitivity and to obtain more consistent results, the same values of resistance are chosen so that the same gate voltage can be applied to all of the transistors otherwise a separate tuning is required in each case.

A summary of different gate voltages with their corresponding cut off frequencies will be given in later sections.

The 0.1 Hz cut off frequency is obtained by V_G = -0.135 V to provide the adequate resistance of 159 GΩ where C =10 pF.

The schematics of the first, second and third order HPF using single tunable pseudo resistor are shown below respectively.

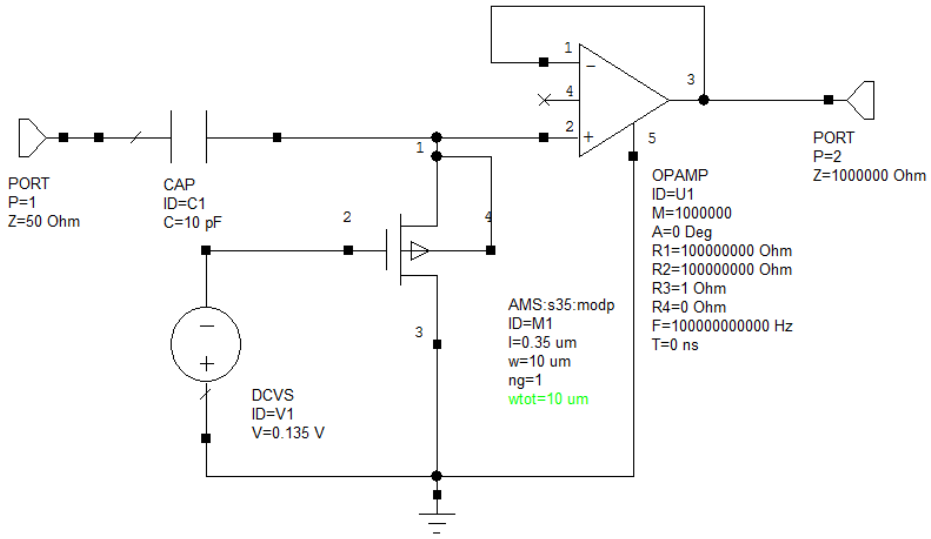


Figure 48: Schematic of the first order HPF using single tunable pseudo resistor

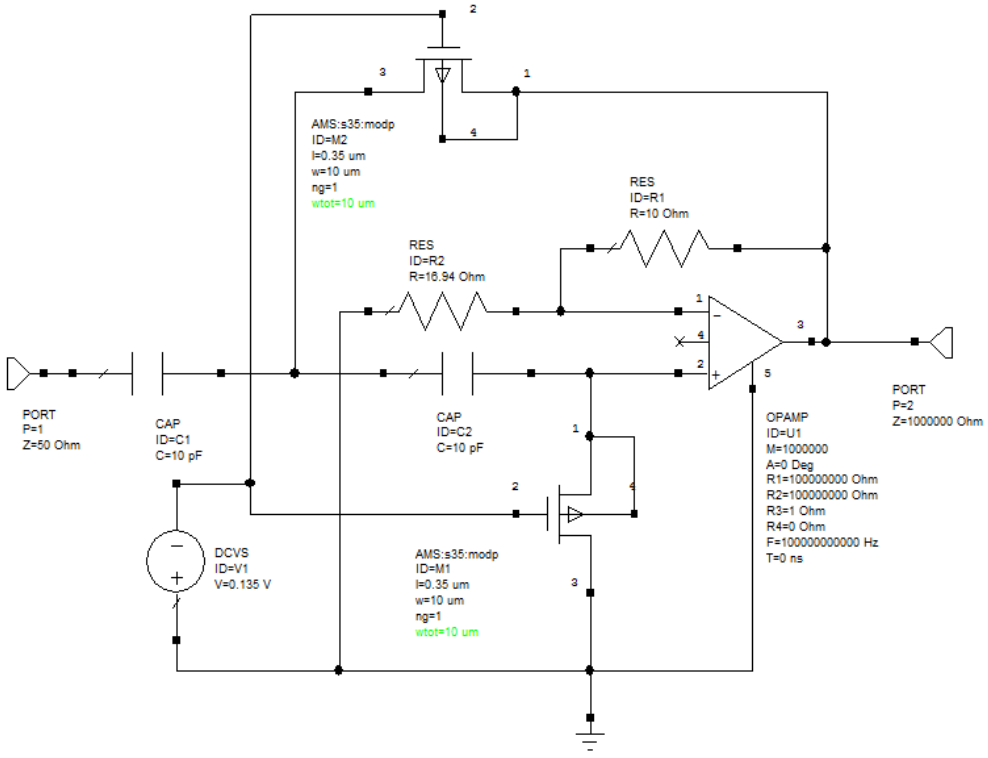


Figure 49: Schematic of the second order HPF using single tunable pseudo resistor

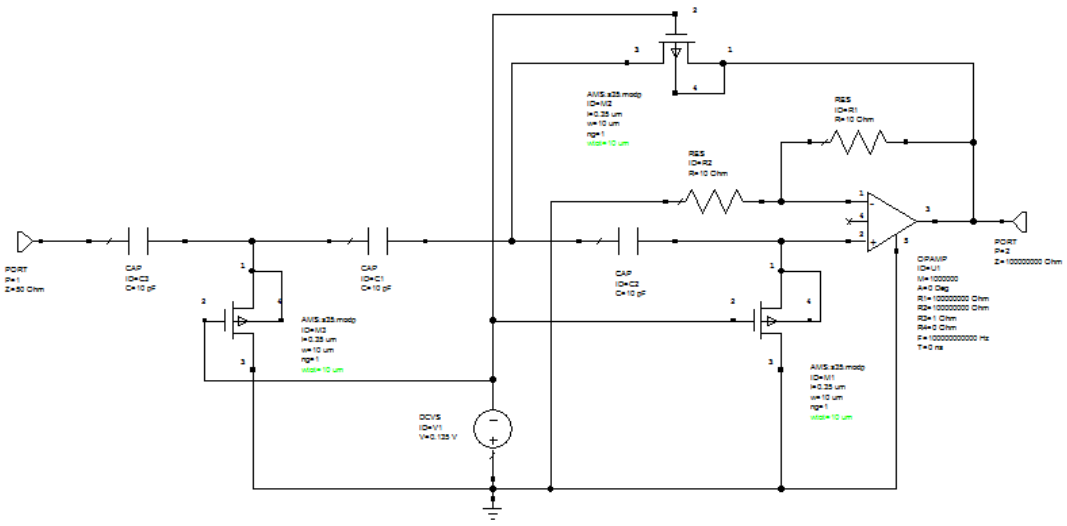


Figure 50: Schematic of the third order HPF using single tunable pseudo resistor

The gain in the second and third order HPF are calculated based on the general topology of Sallen and Key filter. The derivation can be found in Appendix B.

In the first order filter f_C =0.1 Hz is at – 3dB with the roll off of -20 dB at 0.01 Hz. This is presented in the next figure.

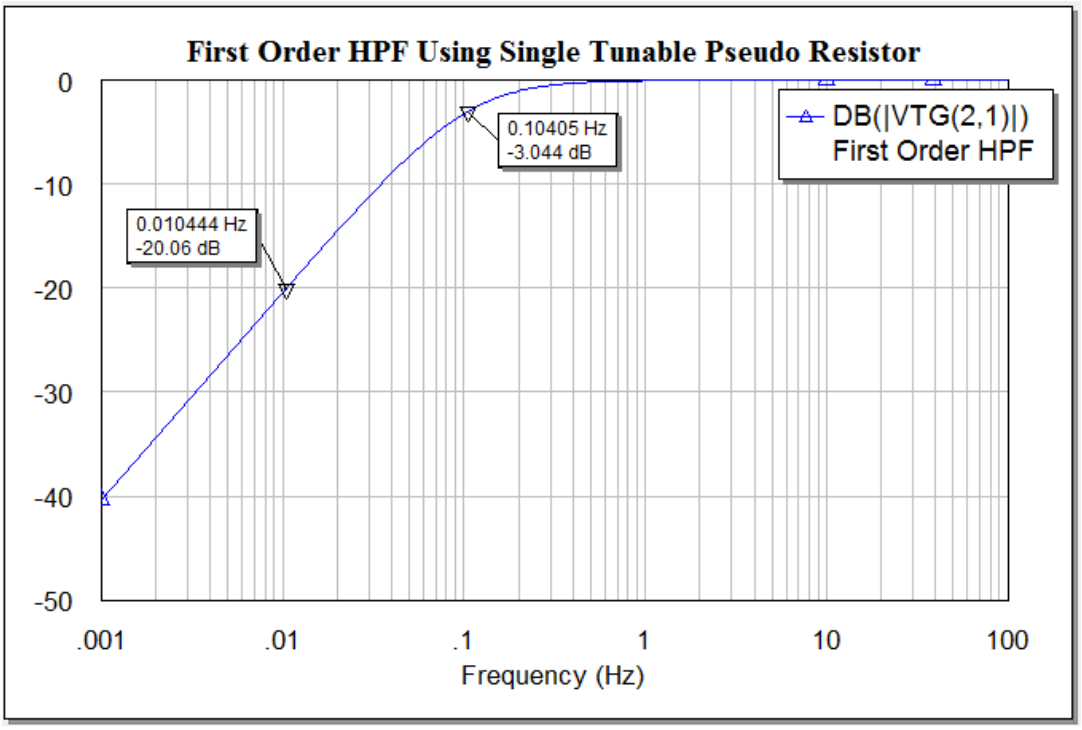


Figure 51: First order HPF using single tunable pseudo resistor

The second order HPF has 4 dB gain. Therefore the cut off frequency of 0.1 Hz will occur at 1 dB and the roll off per decay is 0.01 Hz at -36 dB. Third order HPF with

gain of 6 dB will have f_C of 0.1 Hz at 3 dB and the roll off should be at -54 dB for 0.01 Hz. The results obtained from both graphs are consistent with expected response.

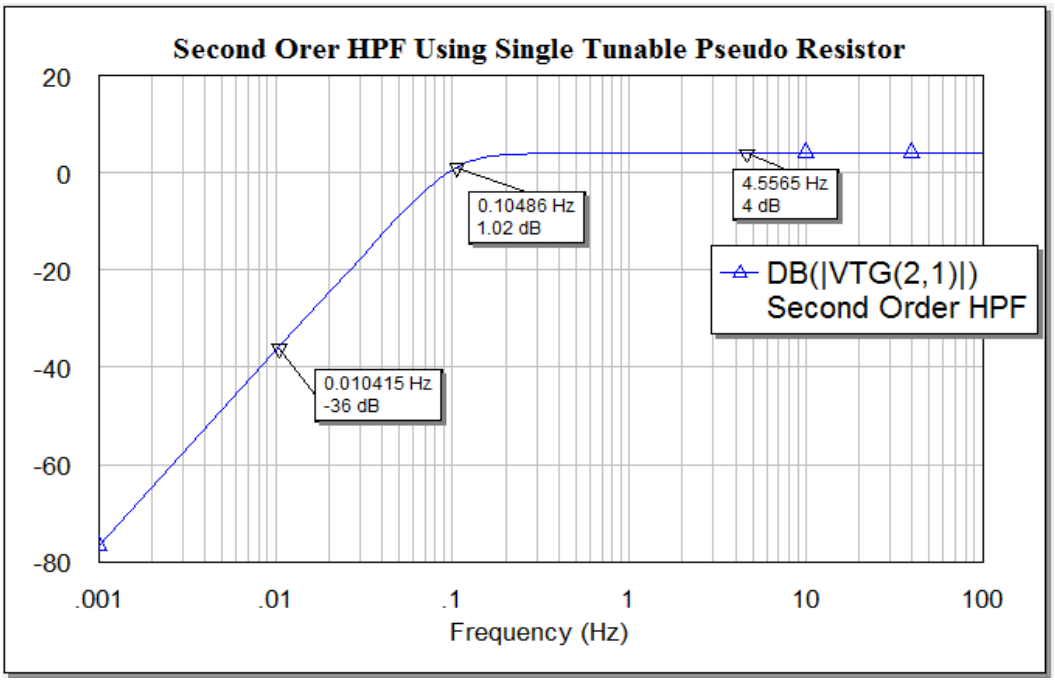


Figure 52: Second order HPF using single tunable pseudo resistor

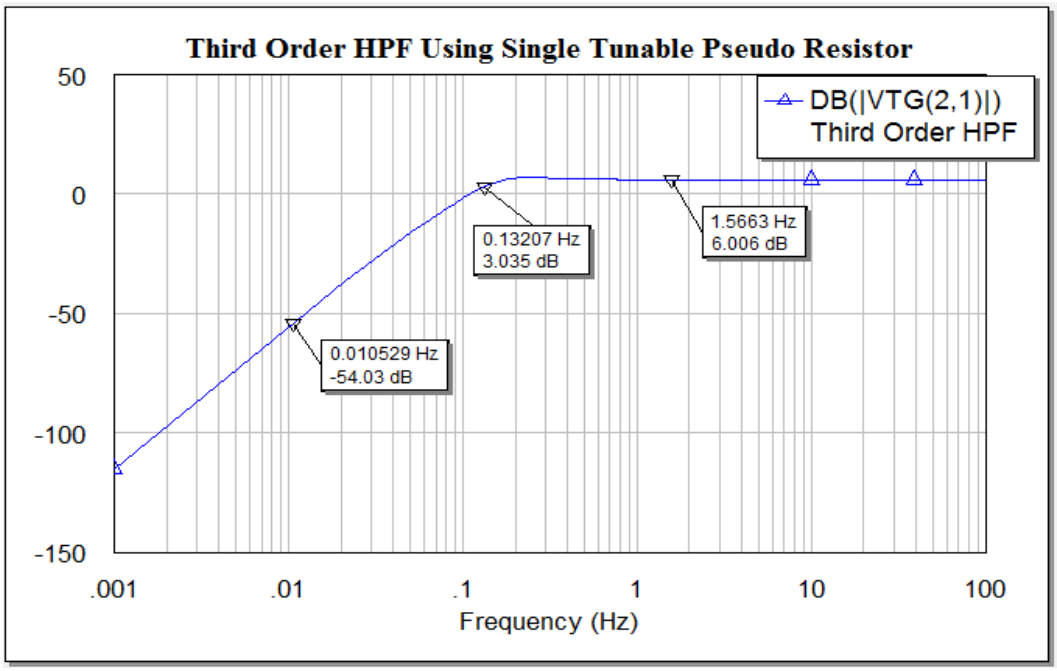


Figure 53: Third order HPF using single tunable pseudo resistor

4.3. LPF and HPF Using Double Tunable Pseudo Resistor:

In this method for design of a LPF with cut off frequency of 100 Hz using double tunable pseudo resistor, two identical PMOS are used. The source of both PMOS are linked together with bulk, the gates are coupled together to the biasing voltage where the drain of the transistors act as two end of a resistor at different potentials [11]. First, second and third order LPF are shown in the following schematics. All other the circuit elements are exactly the same as in the single tunable pseudo resistor.

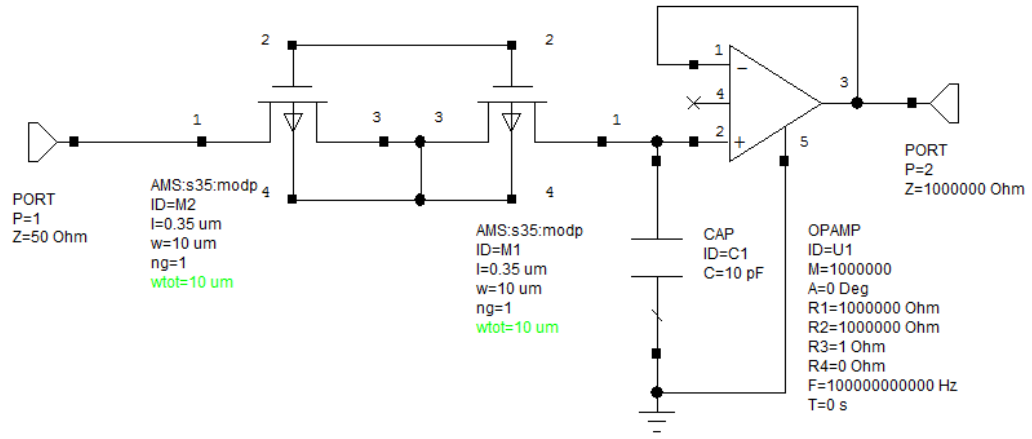


Figure 54: Schematic of the first order LPF using double tunable pseudo resistor

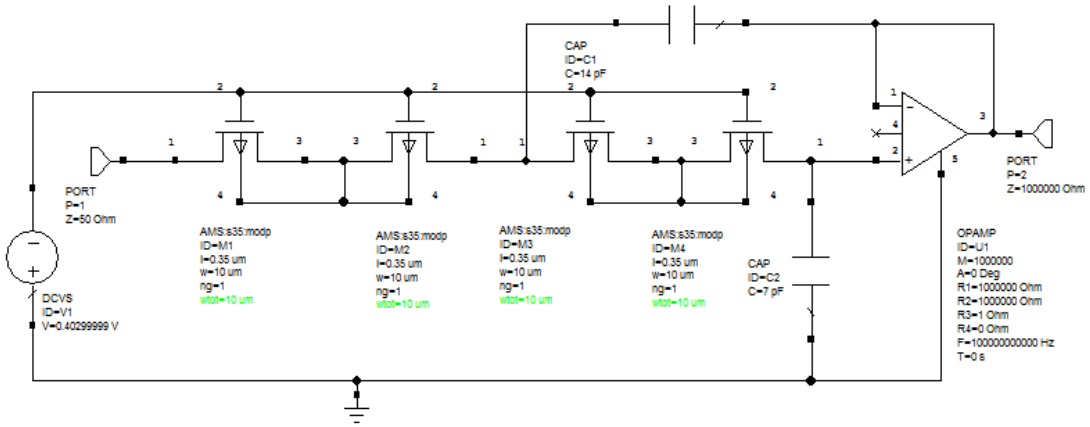


Figure 55: Schematic of the second order LPF using double tunable pseudo resistor

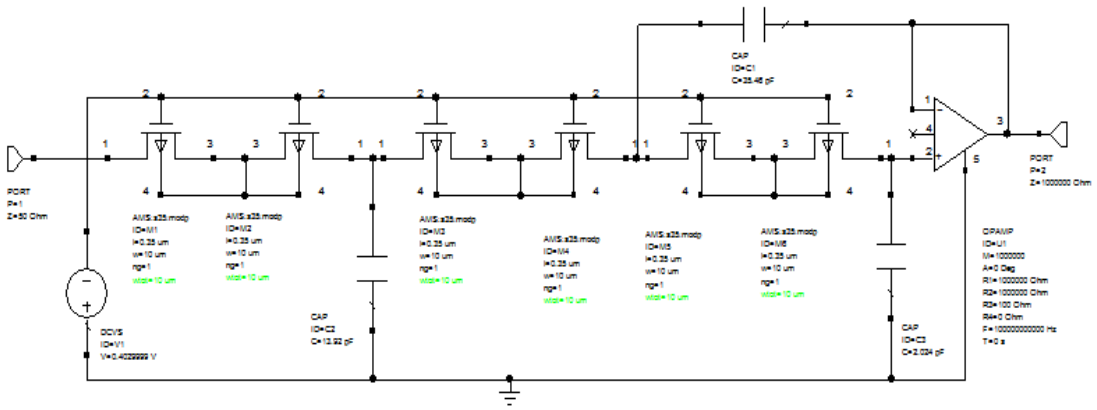


Figure 56: Schematic of the third order LPF using double tunable pseudo resistor

Therefore the resistance provided from double tunable pseudo resistor for 100 Hz cut off frequency is 0.159 GΩ. The result of first order LPF is shown in the following graph so that the 100 Hz cut off appears at – 3dB where -20 dB roll off per decay will appear at 1000 Hz.

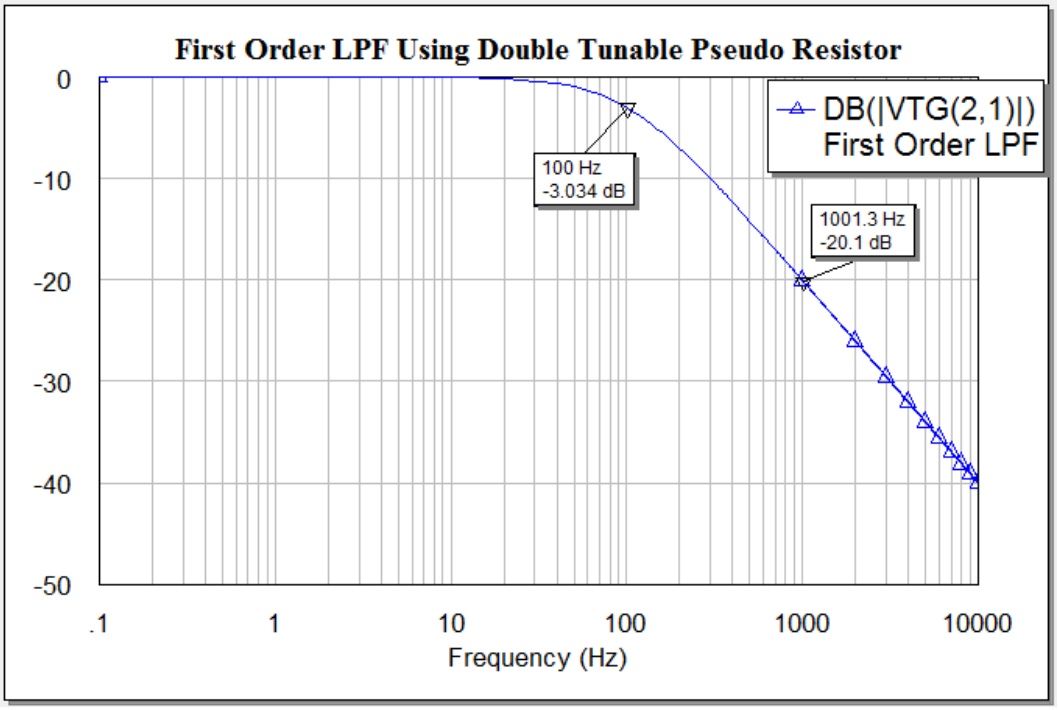


Figure 57: First order LPF using double tunable pseudo resistor

As shown in the schematics for the same value of cut off frequency, the same amount of gate voltage V_G = -0.403 V is used to provide the equal values of resistors.

Thus in the second order 100 Hz is at -3 dB and the roll off at -40 dB is 1000 Hz where the same cut off frequency in third order will have the roll off of -60 dB at 1000 Hz. These are shown in the next two graphs.

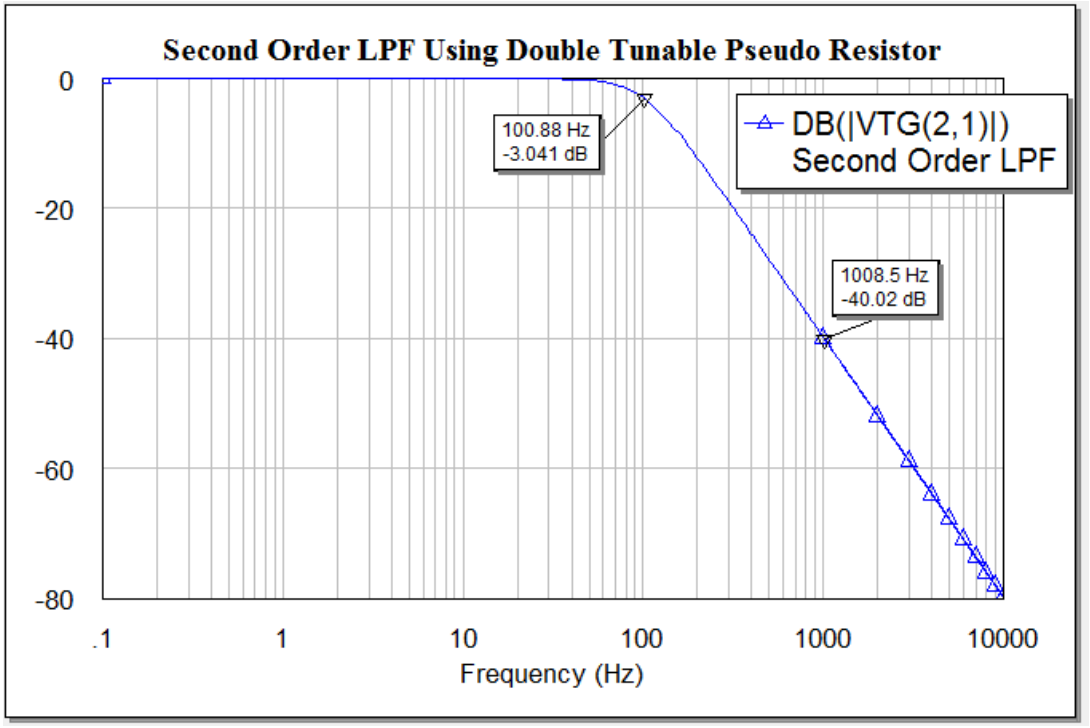


Figure 58: Second order LPF using double tunable pseudo resistor

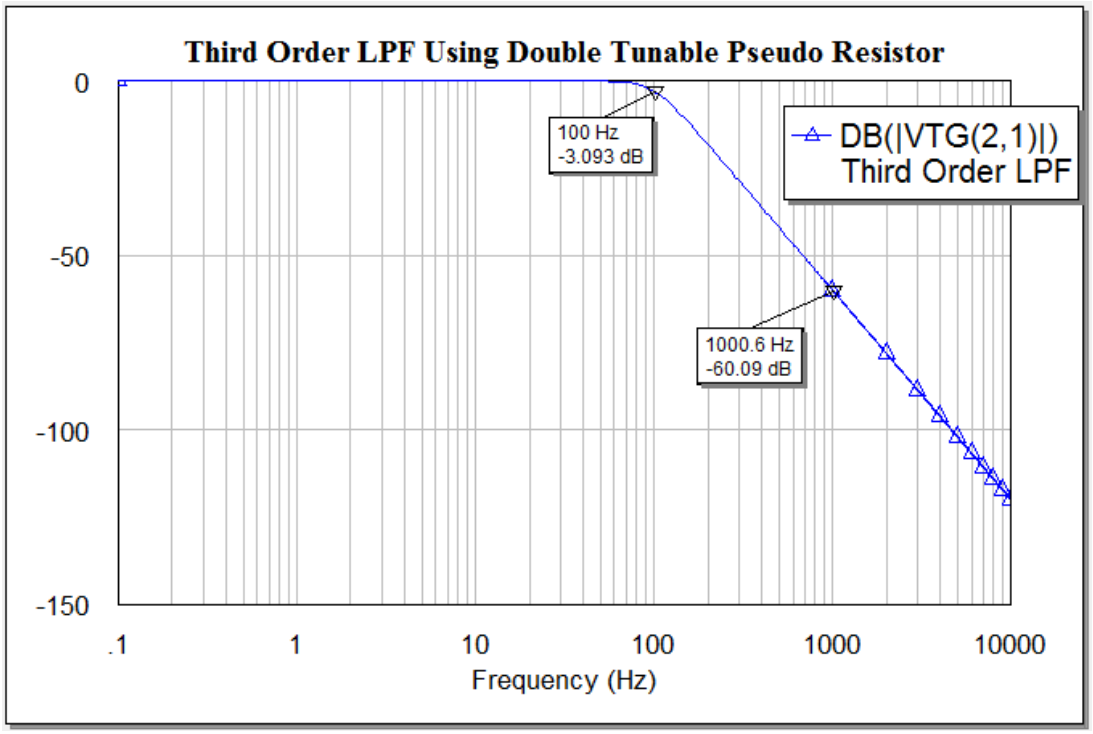


Figure 59: Third order LPF using double tunable pseudo resistor

As in the previous method, in design of HPF equal values of capacitors and resistors are used. The tuning gate voltage is what decides the cut off frequency and as the result the resistance of the circuit. Due to high sensitivity of the circuit, it is not advisable to provide different biasing for each pseudo resistor. In addition to that as an implantable device, the size is one of the primary concerns which should be as small as possible. Therefore having one biasing circuit would be more advisable than having several.

A summary of different gate voltages with their corresponding cut off frequencies will be given in section 4.6.

The 0.1 Hz cut off frequency is obtained by V_G = -0.16 V to provide the adequate resistance of 159 GΩ where C =10 pF.

The schematics of the first, second and third order HPF using double tunable resistor are shown below respectively.

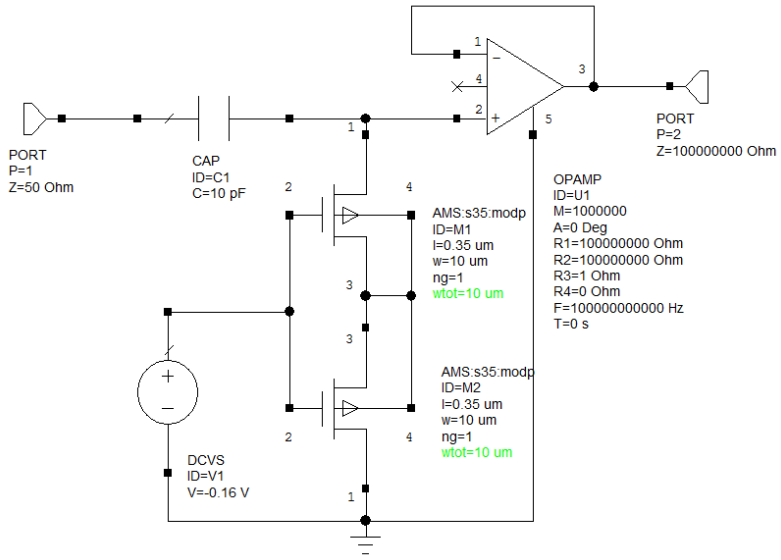


Figure 60: Schematic of the first order HPF using double tunable pseudo resistor

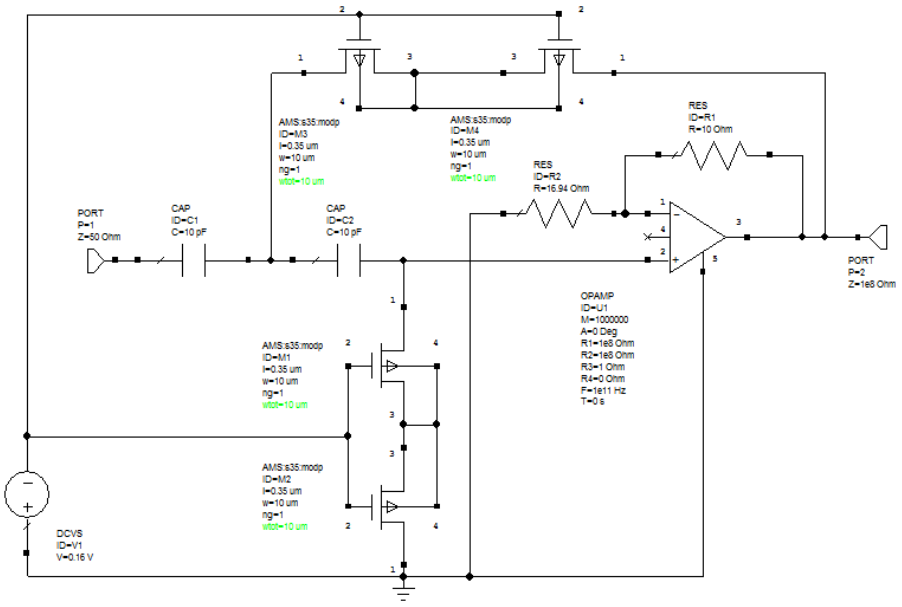


Figure 61: Schematic of the second order HPF using double tunable pseudo resistor

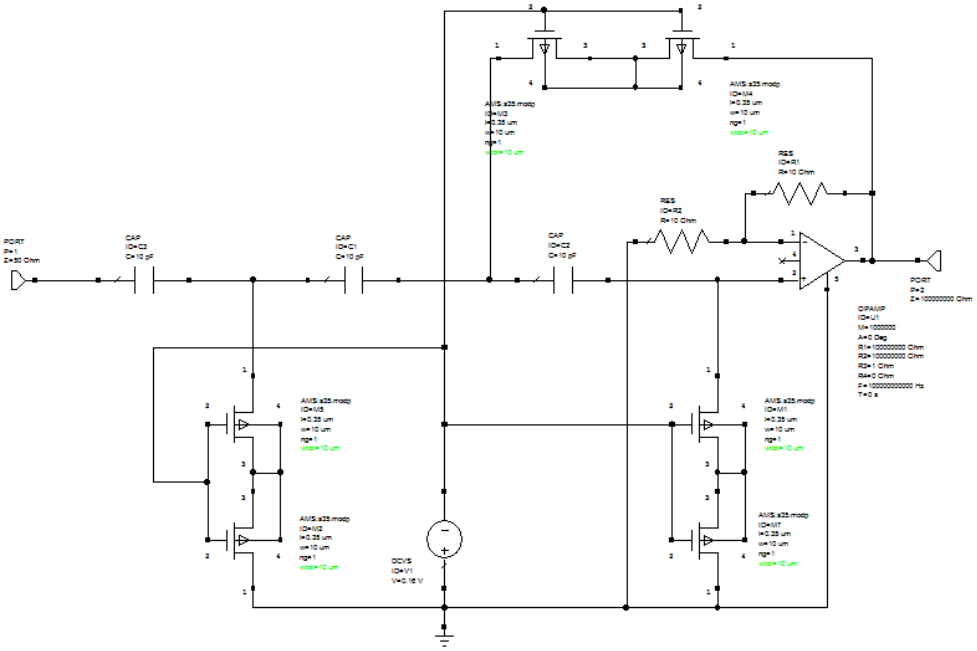


Figure 62: Schematic of the third order HPF using double tunable pseudo resistor

Illustrated in the above schematics, the same gate voltage has been used for the three cases of HPF since they have the same cut off frequency.

In the first order filter f_C =0.1 Hz is at – 3dB with the roll off of -20 dB at 0.01 Hz. This is presented in the next figure.

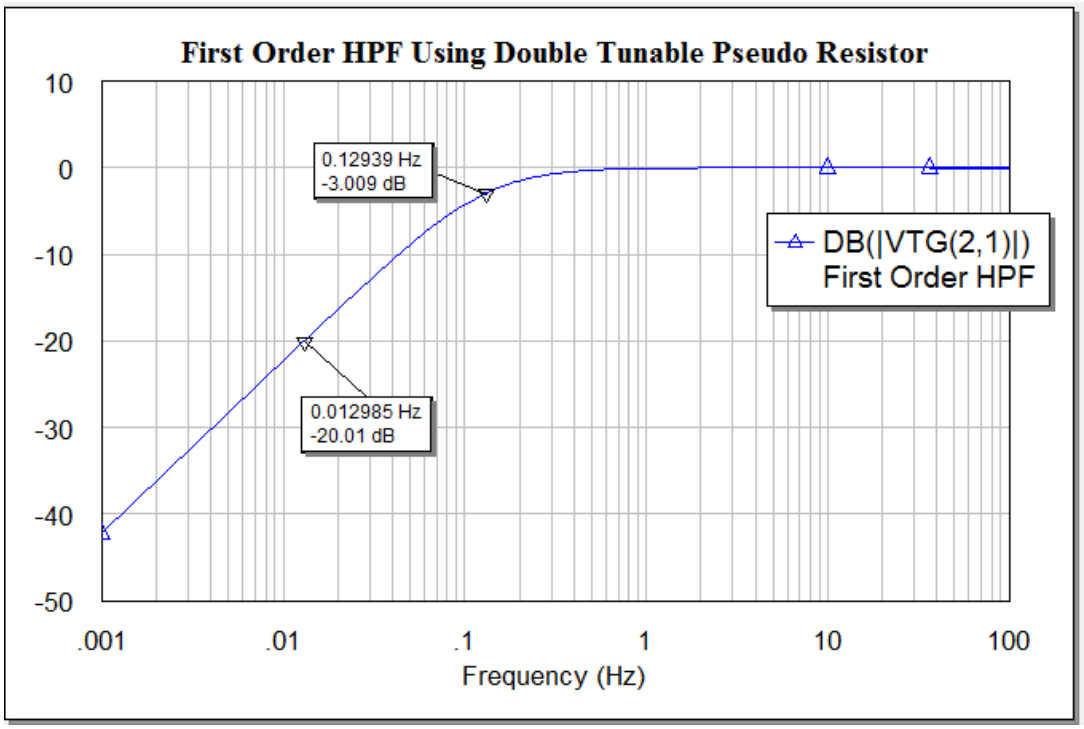


Figure 63: First order HPF using double tunable pseudo resistor

The second order HPF has 4 dB gain. Therefore the cut off frequency of 0.1 Hz will occur at 1 dB and the roll off per decay is 0.01 Hz at -36 dB. Third order HPF with gain of 6 dB will have f_C of 0.1 Hz at 3 dB and the roll off should be at -54 dB for 0.01 Hz. The results obtained from both graphs are consistent with expected response.

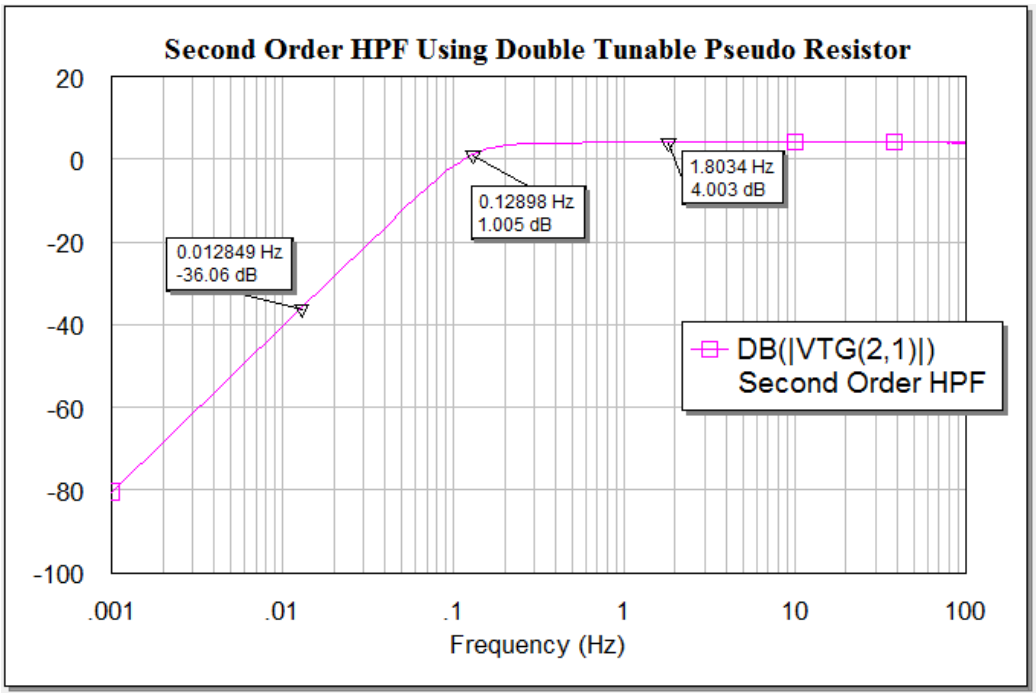


Figure 64: Second order HPF using double tunable pseudo resistor

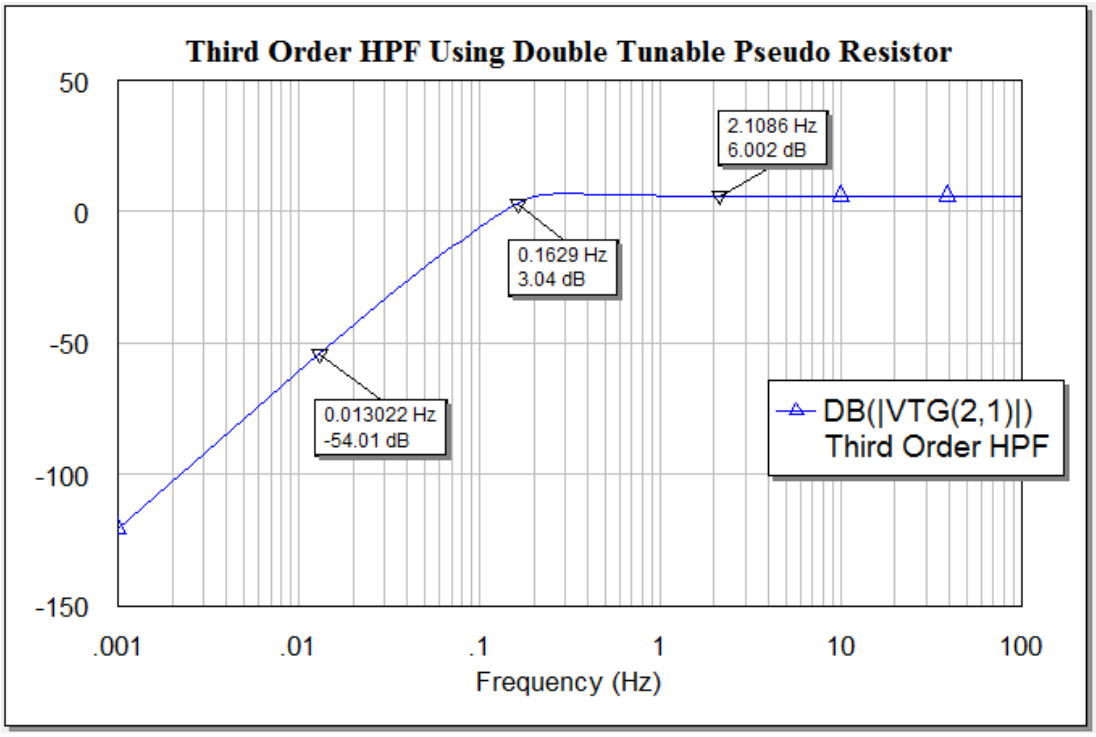


Figure 65: Third order HPF using double tunable pseudo resistor

4.4. Reference Voltage Circuits:

The goal of this section is to replace the independent DC sources used for tuning the filters with reference voltage circuits. There are different approaches to this task including band-gap references. The objective of reference generation is to establish a dc voltage or current that is independent of the supply and the processes and has a well defined behavior with temperature [6]. However in this design a simple approach is considered which is concentrating only on transistors. Cascading several diode connected MOSFET will result in the desired dc voltage that is required for biasing. The potential divider circuits for single tunable pseudo resistor LP and HP filters are shown in the following schematics. The transistor values are listed in the subsequent tables.

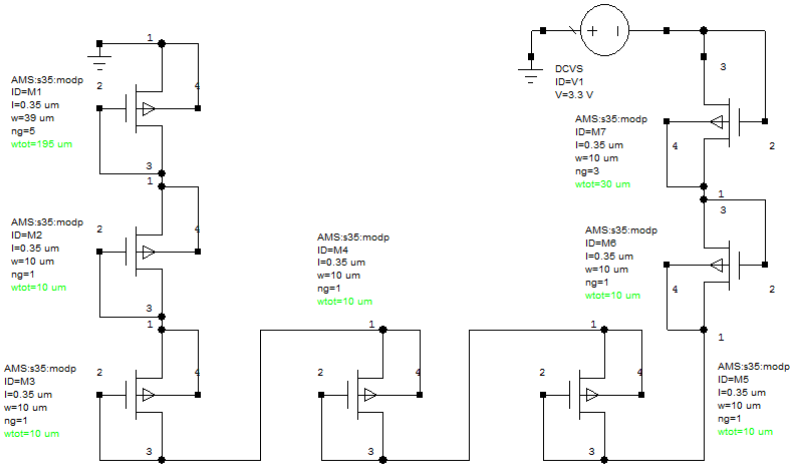


Figure 66: Potential divider for single tunable pseudo resistor in LPF

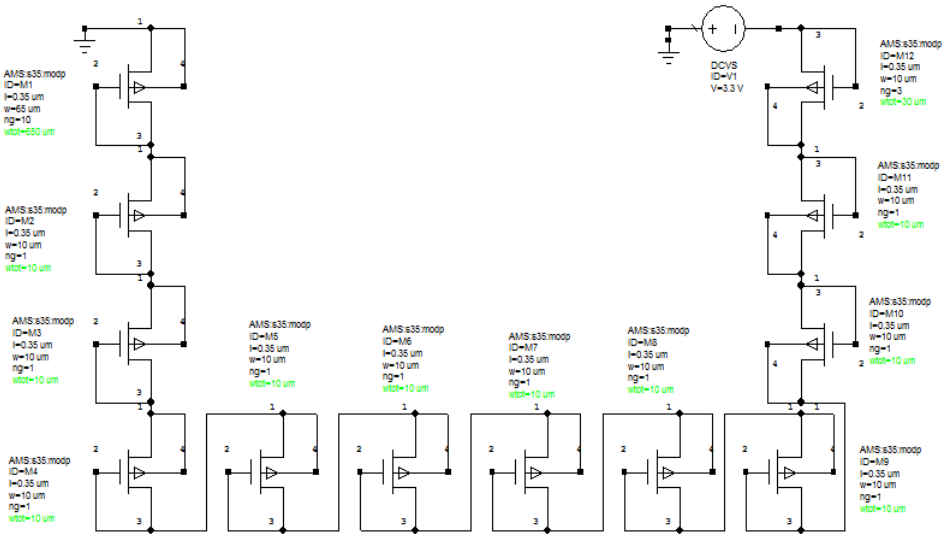


Figure 67: Potential divider for single tunable pseudo resistor in HPF

Table 12: Transistor sizes for potential divider in single tunable pseudo resistor

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12
LPF	W=195 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=30 L= 0.35					
HPF	W=650 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=30 L= 0.35

These potential divider circuits have been replaced in the filter schematics. The frequency response of the first, second and third order LPF and HPF are shown below respectively.

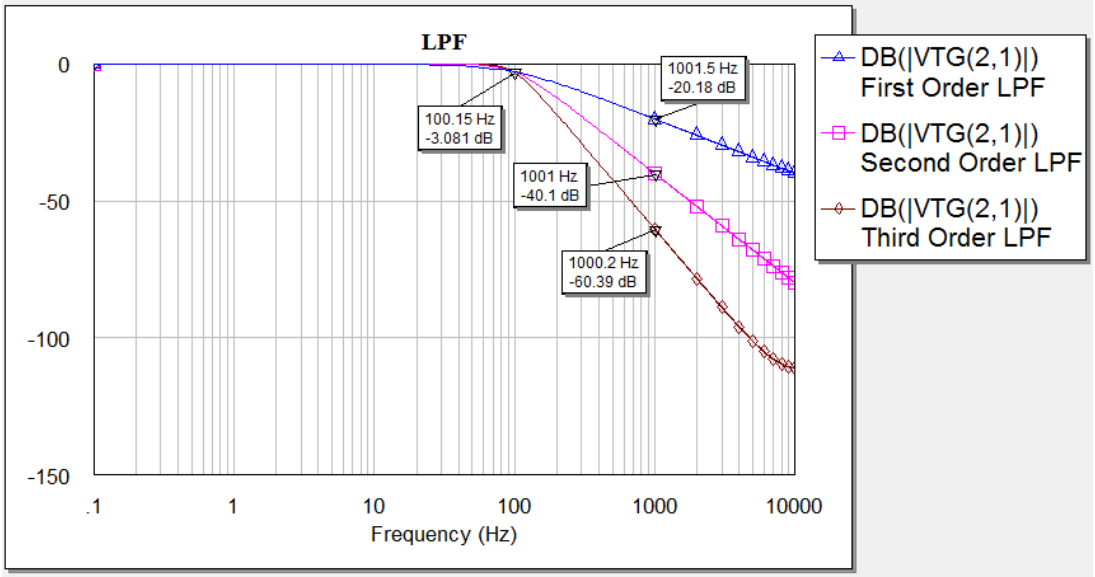


Figure 68: First, second and third LPF using single tunable pseudo resistor

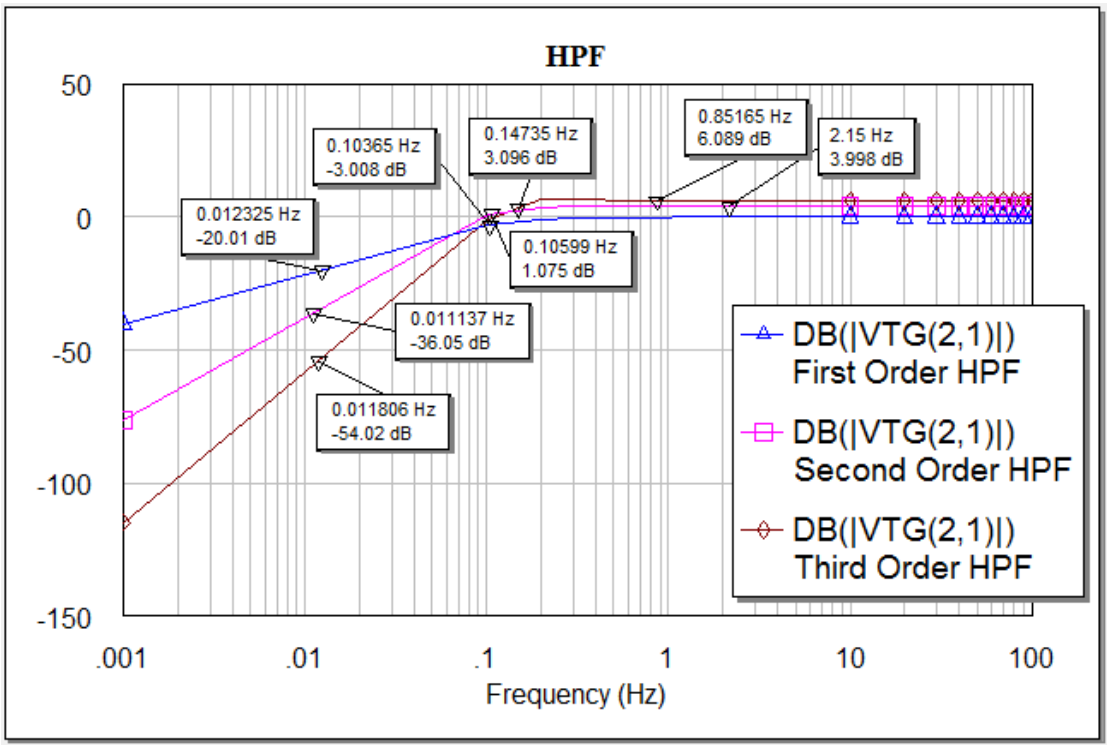


Figure 69: First, second and third order HPF using single tunable pseudo resistor

The same method is used for tuning the double tunable pseudo resistors but with different diode connected transistors sizes. These are shown in the following table.

Table 13: Transistor sizes for potential divider in double tunable pseudo resistor

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12
LPF	W=80 L= 0.35	W=40 L= 0.35	W=20 L= 0.35	W=20 L= 0.35	W=20 L= 0.35	W=20 L= 0.35	W=30 L= 0.35					
HPF	W=470 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=10 L= 0.35	W=30 L= 0.35

These potential divider circuits have been replaced in the filter schematics. The frequency response of the first, second and third order LPF and HPF are shown below respectively.

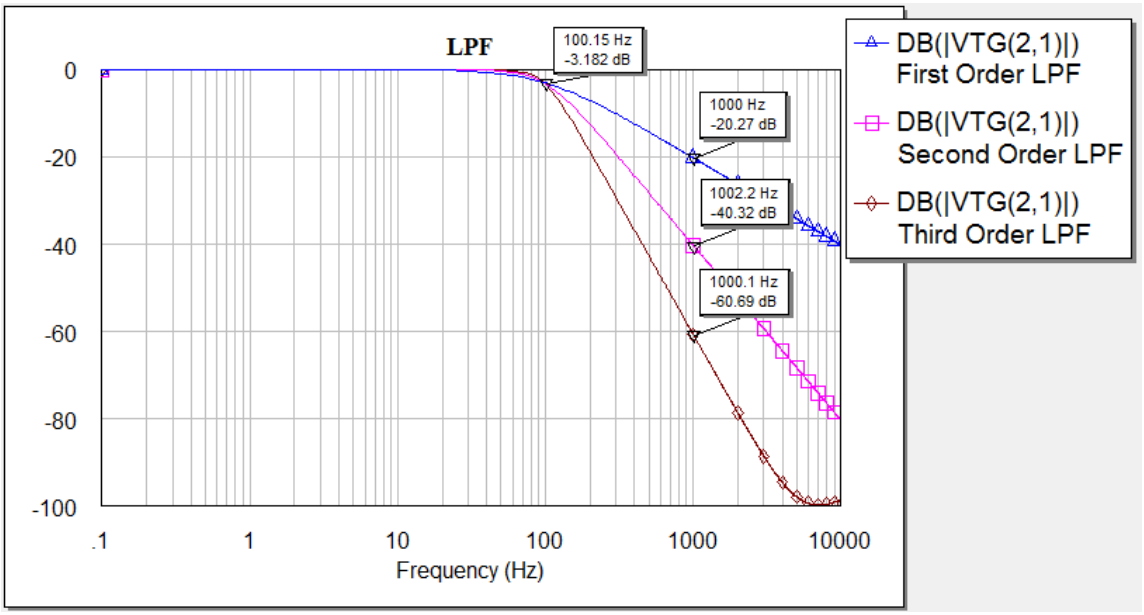


Figure 70: First, second and third order LPF using double tunable pseudo resistor

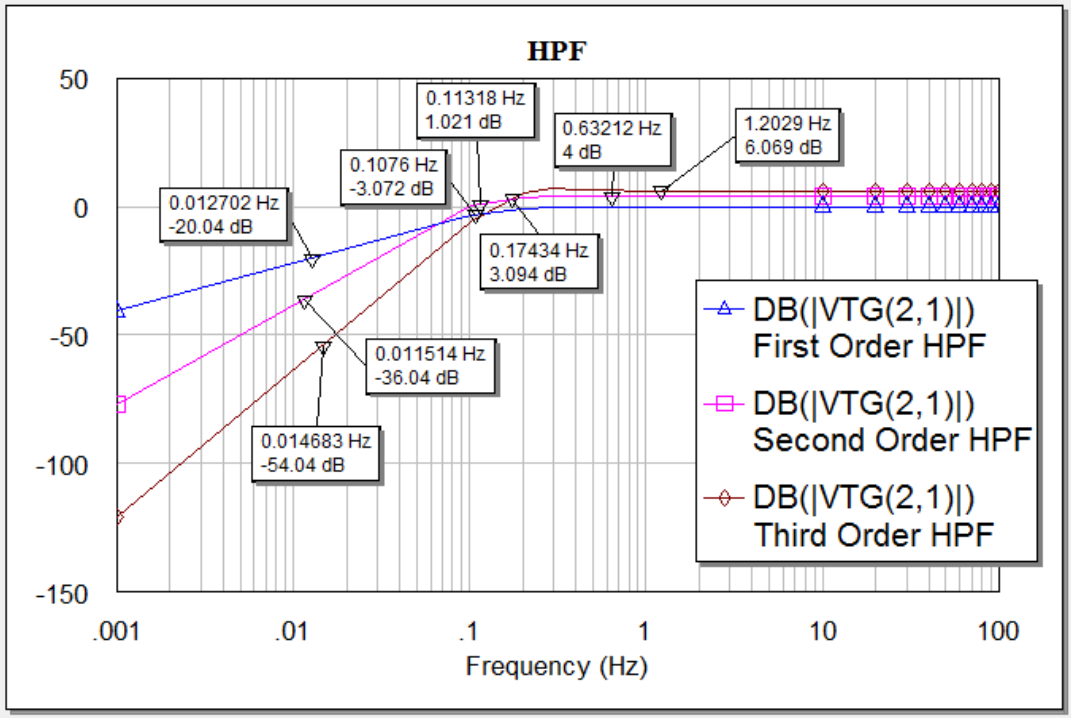


Figure 71: First, second and third order HPF using double tunable pseudo resistor

4.5. LPF and HPF Using Real AMS elements:

So far, all of the elements other than transistors were considered ideal in both approaches. However here the same schematics have been used but the capacitors and the resistors have been replaced by their corresponding AMS values. Therefore each component is defined in terms of width (W), length (L) and multiples (M) that needed to be used. All of these values are presented in the following tables.

Table 14: LPF and HPF AMS components using single tunable pseudo resistor

1st Order LPF Ideal	C = 10 pF		
1st Order LPF AMS	C = 10 pF W = 20 L = 39 M = 10		
2nd Order LPF Ideal	C = 7 pF	C = 14 pF	
2nd Order LPF AMS	C = 6.903 W = 30 L = 30 M= 6	C = 13.94 W = 31 L = 32 M = 11	
3rd Order LPF Ideal	C = 35.46	C = 2.024	C = 13.92
3rd Order LPF AMS	C = 35.44 W = 40 L = 41 M = 17	C = 2.068 W = 20 L = 20 M = 4	C = 13.92 W = 31 L = 32 M = 11
1st Order HPF Ideal	C = 10 pF		
1st Order HPF AMS	C = 10 W = 20 L = 39 M = 10		
2nd Order HPF Ideal	C = 10 pF	R = 10 Ω	R = 16.94Ω
2nd Order HPF AMS	C = 10 pF W = 20 L = 39 M = 10	R = 10 W = 40 L = 15 M = 9	R = 16.59 W= 31 L = 15 M = 7
3rd Order HPF Ideal	C = 10 pF	R = 10 Ω	
3rd Order HPF AMS	C = 10 W = 20 L = 39 M = 10	R= 10 W = 40 L = 15 M = 9	

Based on the presented values for single tubable pseudo resistors the following graphs for LPF and HPF are as the following:

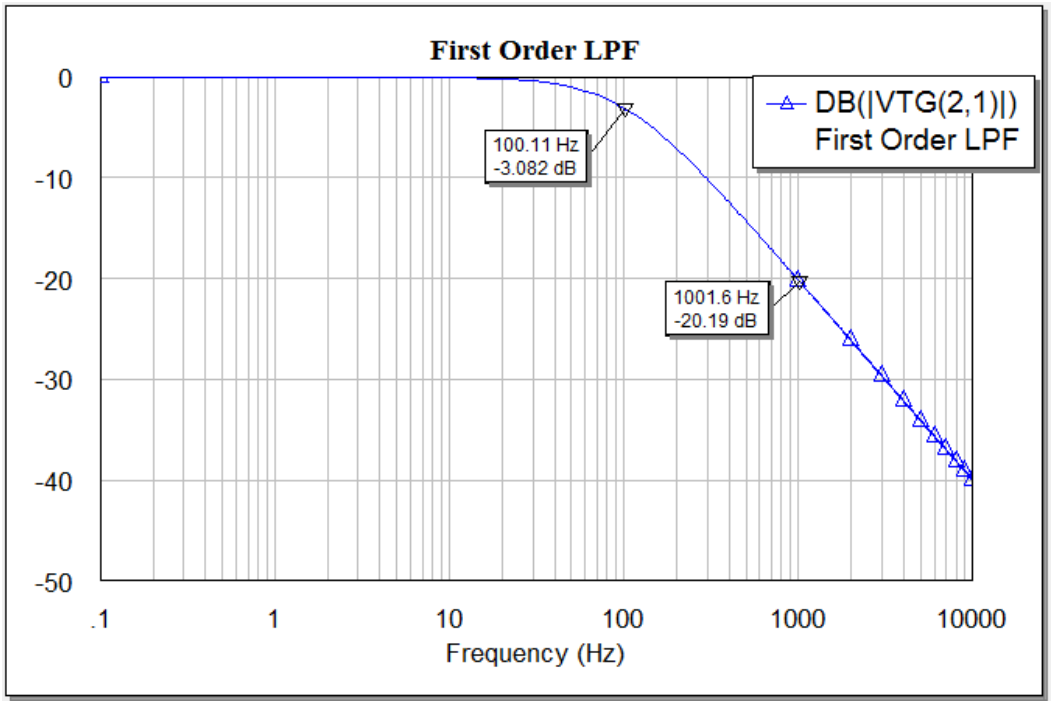


Figure 72: First order LPF using single tunable pseudo resistor with AMS components

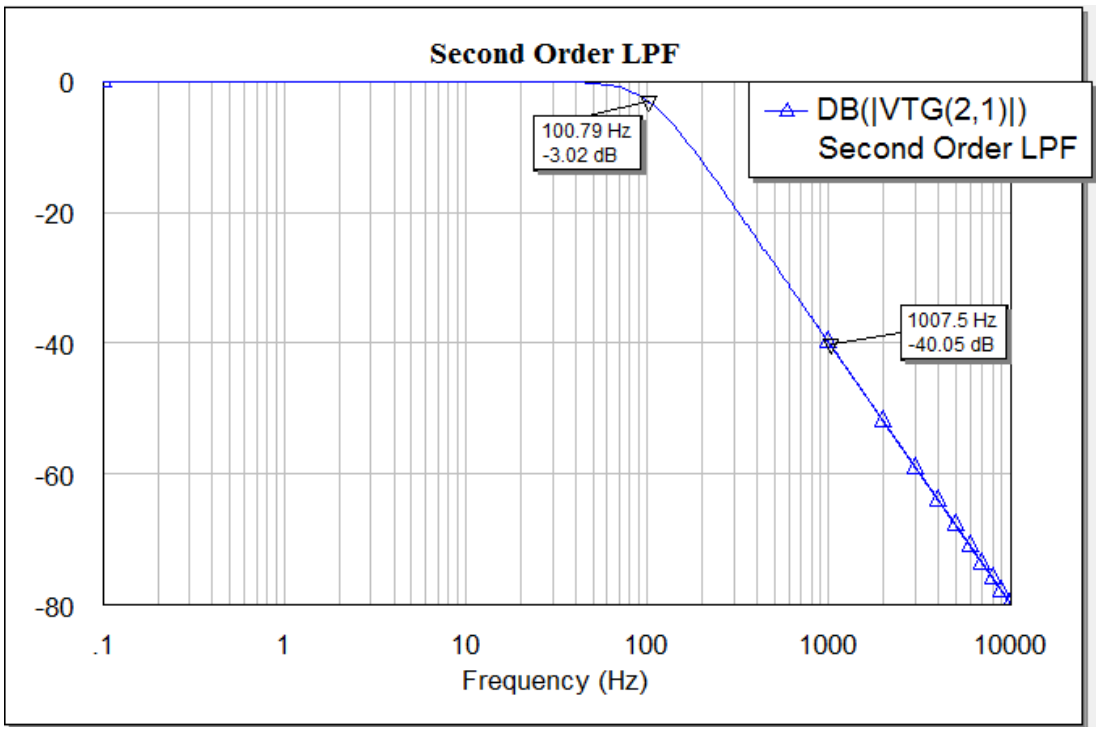


Figure 73: Second order LPF using single tunable pseudo resistor with AMS components

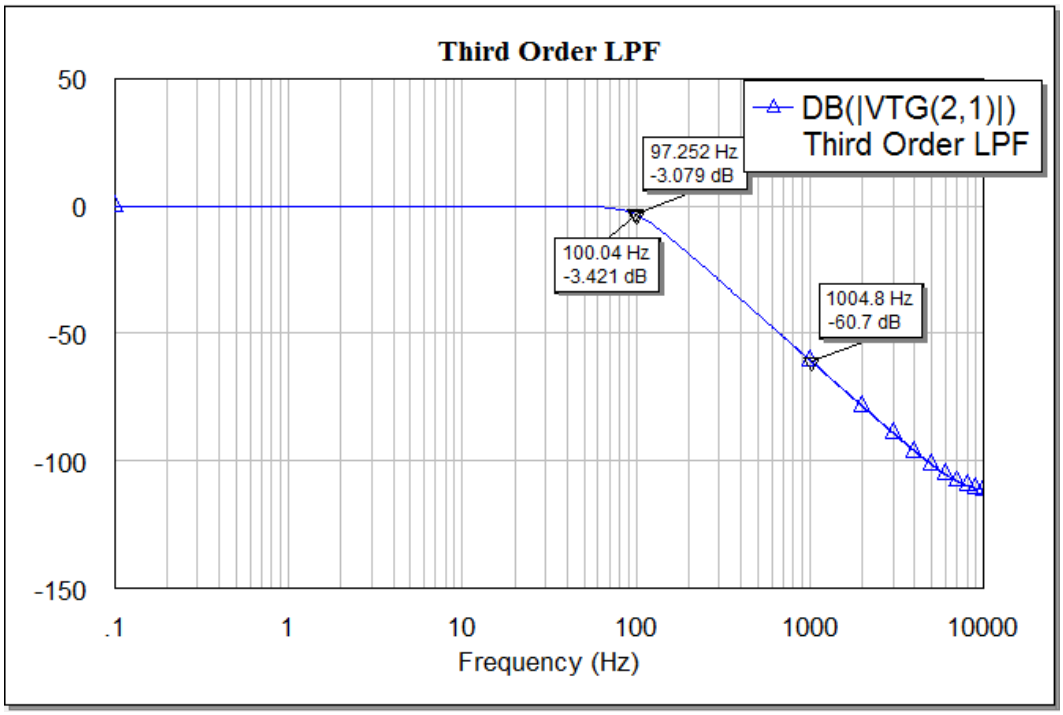


Figure 74: Third order LPF using single tunable pseudo resistor with AMS components

As it shown in the LPF graphs the cut off frequency is slightly shifted from 100 Hz in the third order filter. Not being able to achive exact values of capacitors as in the ideal components is the main resason for this small difference.

The following graphs are showing the HPF using single tunable pseudo resistor with AMS componets.

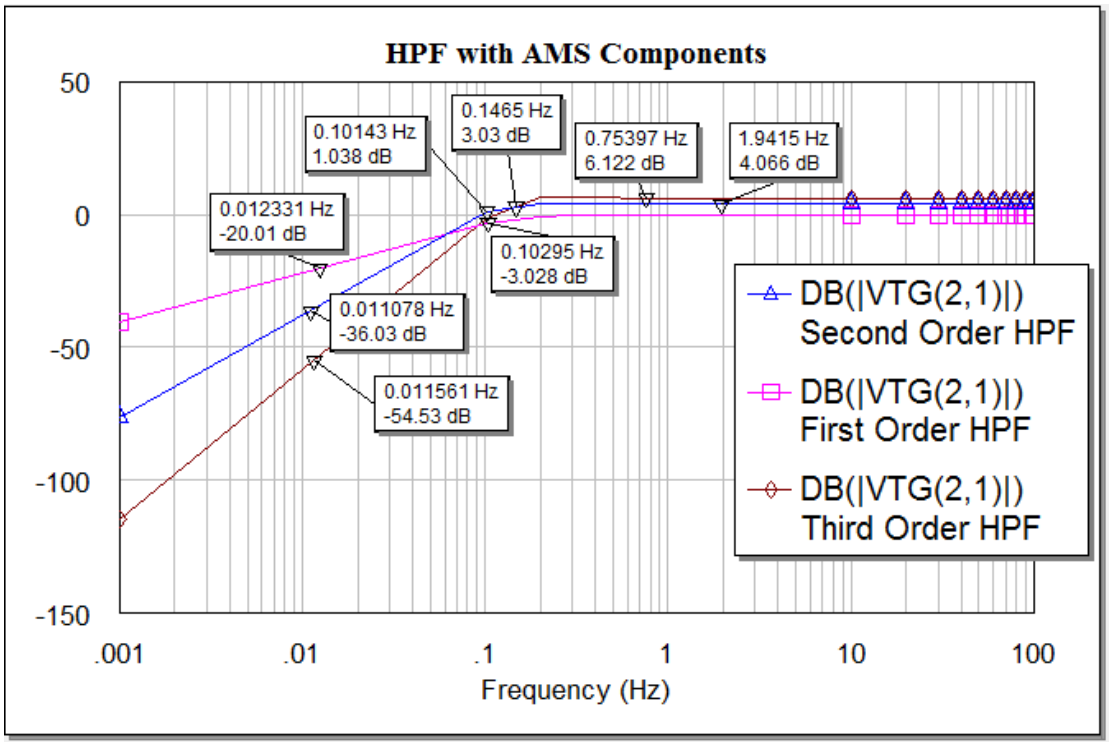


Figure 75: First, second and third order HPF using single tunable pseudo resistor with AMS components

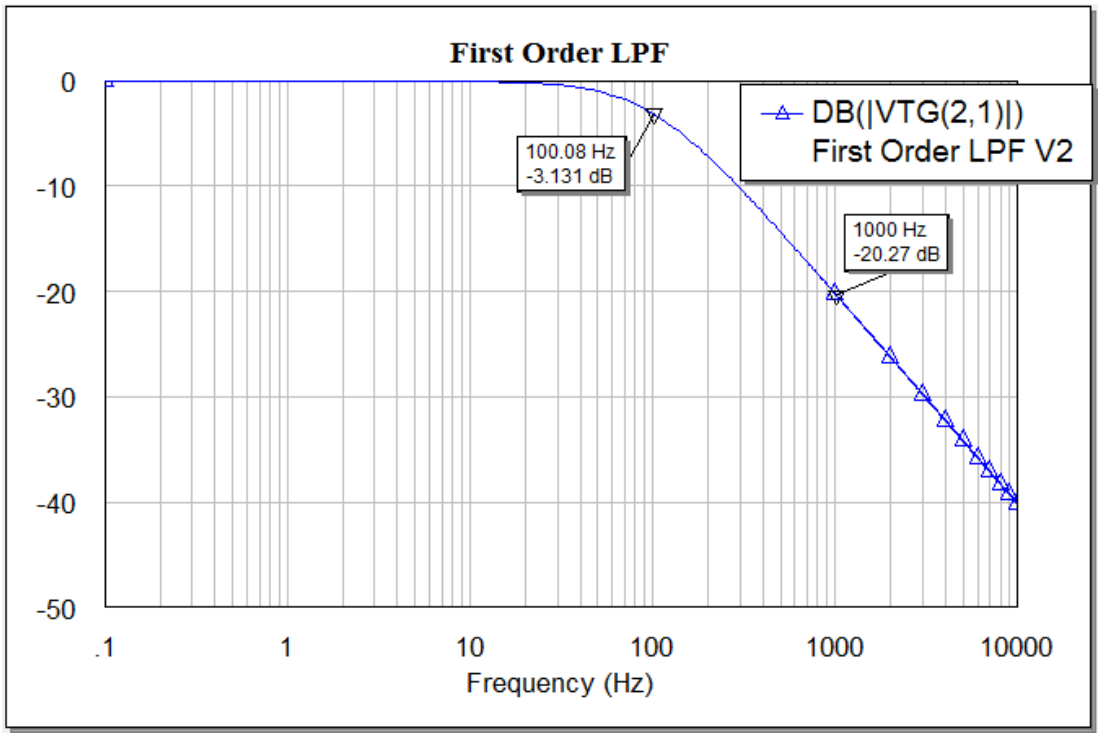
As seen in the graphs for HPF, the results are more consistent and the exact cut off frequency is achieved in all of the orders. This is due to the exact value of capacitor which is 10 pF .The AMS resistor used for gain are almost the same and do not contribute any change in the cut off frequency.

Next table will summarize the AMS components values for LPF and HPF using double tunable pseudo resistor.

Table 15: LPF and HPF AMS components using double tunable pseudo resistor

1st Order LPF Ideal	C = 10 pF		
1st Order LPF AMS	C = 10 pF W = 20 L = 39 M = 10		
2nd Order LPF Ideal	C = 7 pF	C = 14 pF	
2nd Order LPF AMS	C = 6.903 W = 30 L = 30 M= 6	C = 13.94 W = 31 L = 32 M = 11	
3rd Order LPF Ideal	C = 35.46	C = 2.024	C = 13.92
3rd Order LPF AMS	C = 35.44 W = 40 L = 41 M = 17	C = 2.068 W = 20 L = 20 M = 4	C = 13.92 W = 31 L = 32 M = 11
1st Order HPF Ideal	C = 10 pF		
1st Order HPF AMS	C = 10 W = 20 L = 39 M = 10		
2nd Order HPF Ideal	C = 10 pF	R = 10 Ω	R = 16.94Ω
2nd Order HPF AMS	C = 10 pF W = 20 L = 39 M = 10	R = 10 W = 40 L = 15 M = 9	R = 16.59 W= 31 L = 15 M = 7
3rd Order HPF Ideal	C = 10 pF	R = 10 Ω	
3rd Order HPF AMS	C = 10 W = 20 L = 39 M = 10	R = 10 W = 40 L = 15 M = 9	

Based on the values in the table the graphs for LPF using double tunable pseudo resistor with AMS components are shown below:



6: First order LPF using double tunable pseudo resistor with AMS components7Figure

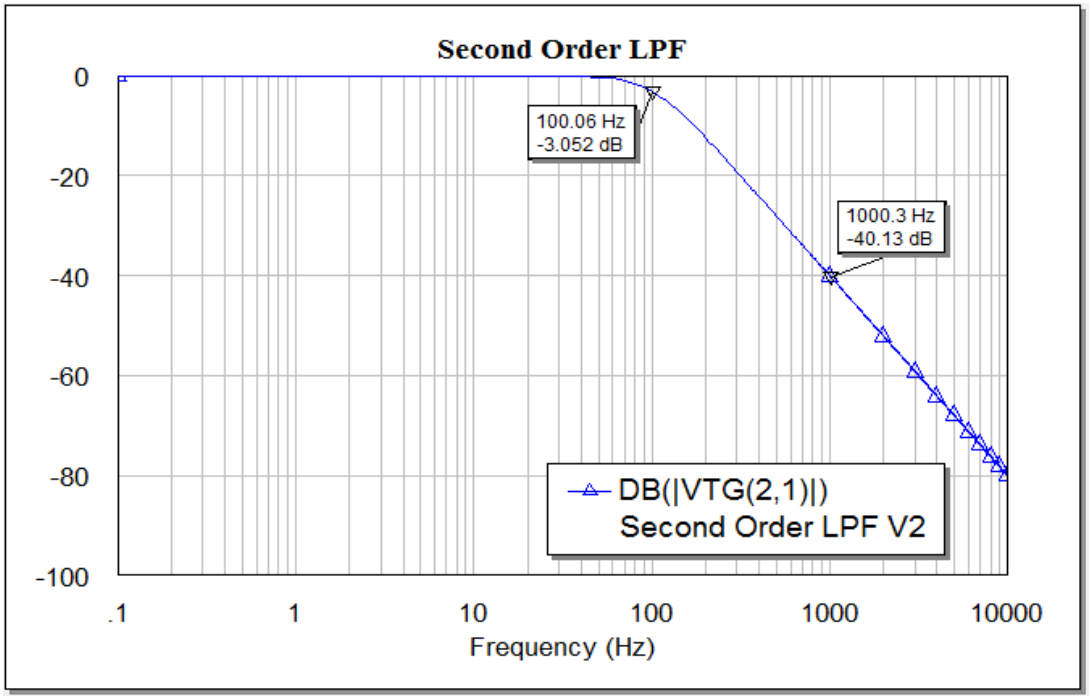


Figure 77: Second order LPF using double tunable pseudo resistor with AMS components

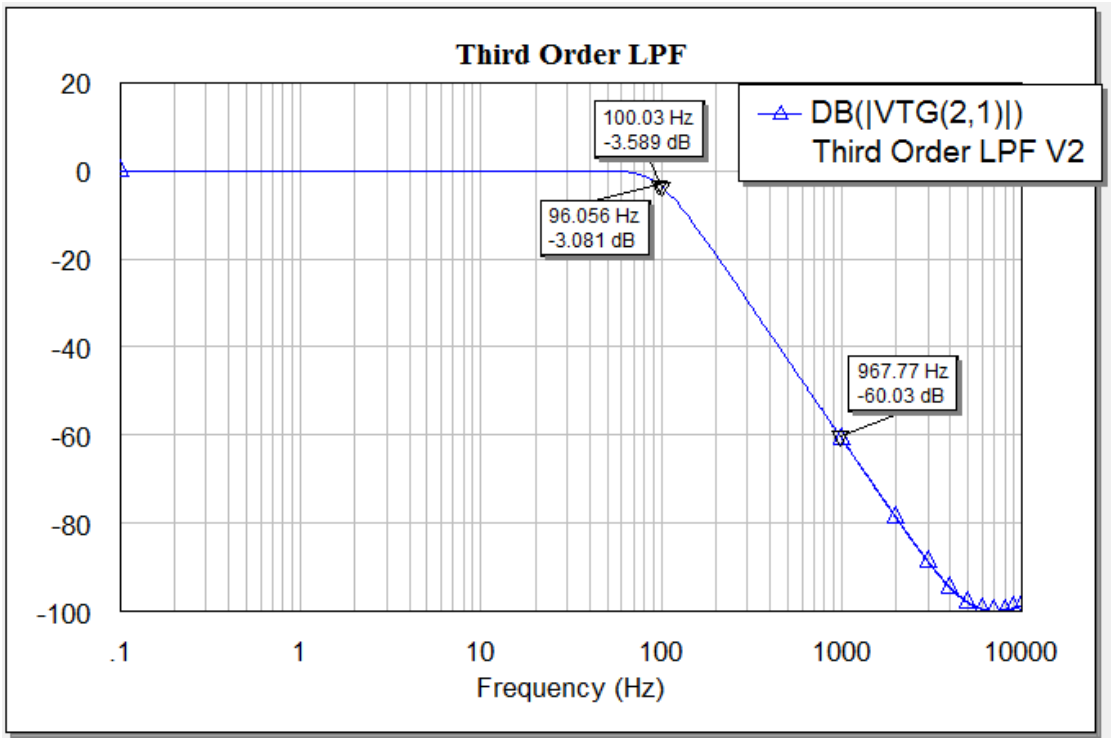


Figure 78: Third order LPF using double tunable pseudo resistor with AMS components

As it's shown in the LPF graphs the cut off frequency is slightly shifted from 100 Hz in the third order filter. Not being able to achive exact values of capacitors as in the ideal components is the main resason for this small difference.

Next the graphs for HPF using double tunable pseudo resistor with AMS components are presented.

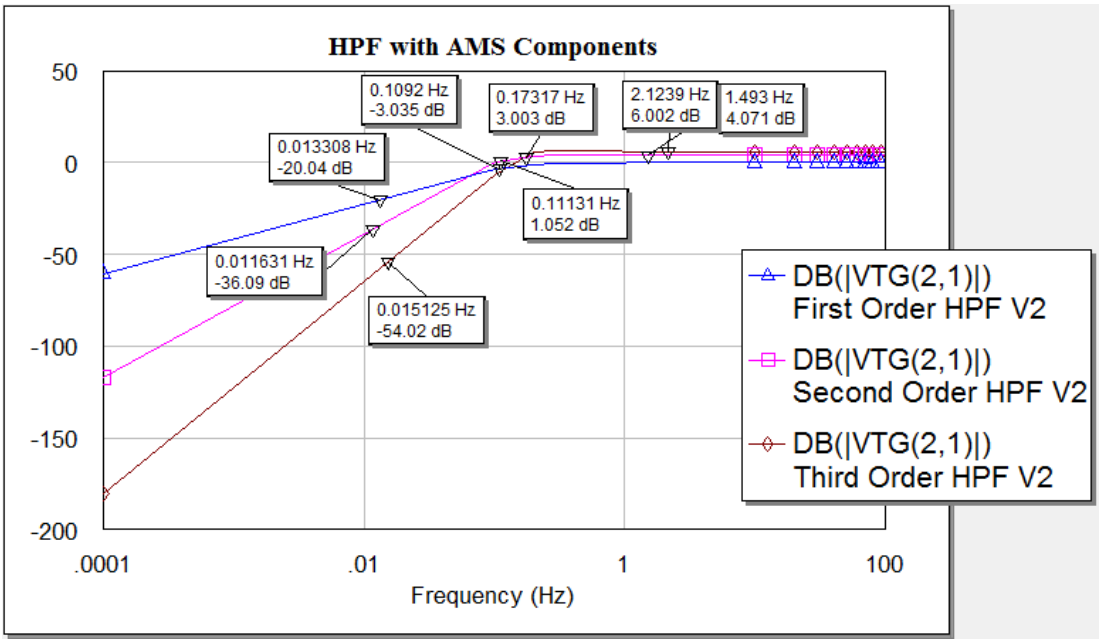


Figure 79: First, second and third order HPF using double tunable pseudo resistor with AMS components

As the result the cut off frequency for HPF is the same as the case for using ideal elements.

4.6. Different Frequencies with Their Corresponding V_G:

The following tables show a comparison of different cutoff frequencies with their corresponding gate voltages, using both single and double tunable pseudo resistors in third order LPF and HPF.

Table 16: Frequency comparison for third order LPF and HPF using single tunable pseudo resistors

3rd Order	V_g = 0.3 V	V_g = 0.35V	V_g = 0.378V	V_g = 0.4V	V_g = 0.42V
LPF f_C	10.6 Hz	54 Hz	100 Hz	183 Hz	319 Hz
3rd Order	V_g =0.135V	V_g =0.14 V	V_g = 0.145V	V_g =0.2 V	V_g =0.25 V
HPF f_C	0.1 Hz	0.16 Hz	0.18 Hz	0.8 Hz	3.4 Hz

Table 17: Frequency comparison for third order LPF and HPF using double tunable pseudo resistors

3rd Order	V_g = 0.39V	V_g = 0.4 V	V_g = 0.4029	V_g = 0.42V	V_g = 0.45V
LPF f_C	84 Hz	91 Hz	100 Hz	160 Hz	367 Hz
3rd Order	V_g =0.16 V	V_g =0.165 V	V_g =0.18 V	V_g =0.2 V	V_g =0.3 V
HPF f_C	0.1 Hz	0.16	0.24	0.4	7 Hz

Based on the outcome of table 16 and 17, it can be concluded that the rate of change in corner frequency in LPF filter in both approaches is faster than HPF. However in both cases the system is very sensitive to small variation of the gate voltage. In addition, these results show that the tunable filters can also be used for other biomedical signal processing applications with different bandwidths.

4.7. Linearity, Noise and Power Consumption of Pseudo Resistor Devices:

In this section Linearity, noise and power consumption of single and double tunable pseudo resistor for both third order LP and HP filters is determined.

Linearity: In order to check the linearity of a system, several approaches can be implemented. The most common tests are two tone test, third order inter modulation (IIP3) and 1dB Compression Point test.

In the two tone test, an input consisting of two sine waves is applied to the system. This can be shown as

$$v_{in} = v_1 cos\omega_1 t + v_2 cos\omega_2 t = X_1 + X_2 \quad (57)$$

Any nonlinear transfer function can be written as a series expansion of power terms unless system has memory, therefore the result of this input is [17]

$$v_0 = k_0 + k_1(X_1 + X_2) + k_2(X_1 + X_2)^2 + k_3(X_1 + X_2)^3 \quad (58)$$

Where $k_1(X_1 + X_2)$ are the desired frequencies, $k_2(X_1 + X_2)^2$ are the second order nonlinearity and $k_3(X_1 + X_2)^3$ are the third order nonlinearity. Each term is composed of dc and harmonics. These harmonics will appear as the sum and difference frequencies of the two input signals. Third order nonlinearity results in third harmonics and third order intermodulation. Of all the unwanted terms, the last two at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, are the most troublesome, since they can fall in the band of desired output if the two are close and cannot be filtered out [17]. These two tones are referred to as third order intermodulation terms.

In third order intercept point, two signals are applied to the input of the circuit having equal amplitude and offset by some frequency. Then, the fundamental output and intermodulation output power are plotted as a function of input power. The third order intercept point is a theoretical point where the amplitudes of the fundamental tones are equal to the amplitudes of the intermodulation tones [17].

The 1 dB compression point is more directly measurable that IP3 and needs only one tone. This is basically the power level, specified either at the input or output, where the output power is 1 dB less than it would have been in an ideally linear device.

It is anticipated that for a single tone, the compression point is about 10 dB below the intercept point, while for the two tones it is about 15 dB below the intercept point [17].

Here 1dB compression point test is used to simulate the nonlinearity of both LPF and HPF. A single tone signal at 70 Hz is applied to the input of the LPF and 100 Hz for the HPF. The following figures show the non linearity of LPF and HPF using single tunable pseudo resistor.

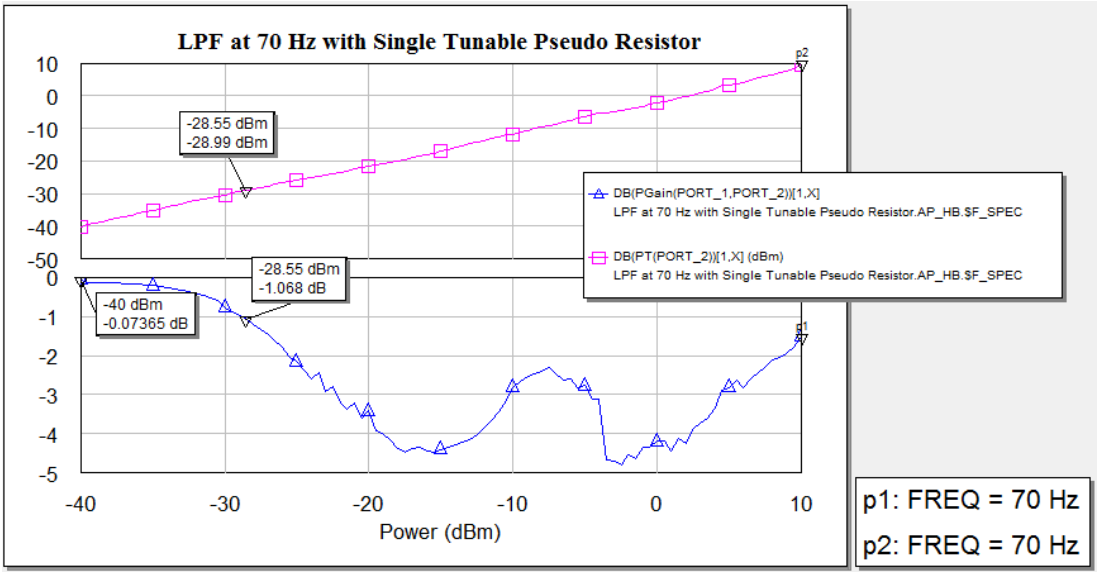


Figure 80: 1dB compression point for LPF using single tunable pseudo resistor

As explained previously

$$IIP_3(dBm) = 10 + P_{1dB}(dBm) \tag{59}$$

For low pass filter using single tunable pseudo resistor: $IIP_3 = 10 - 28.55 = -18.55\ dBm$

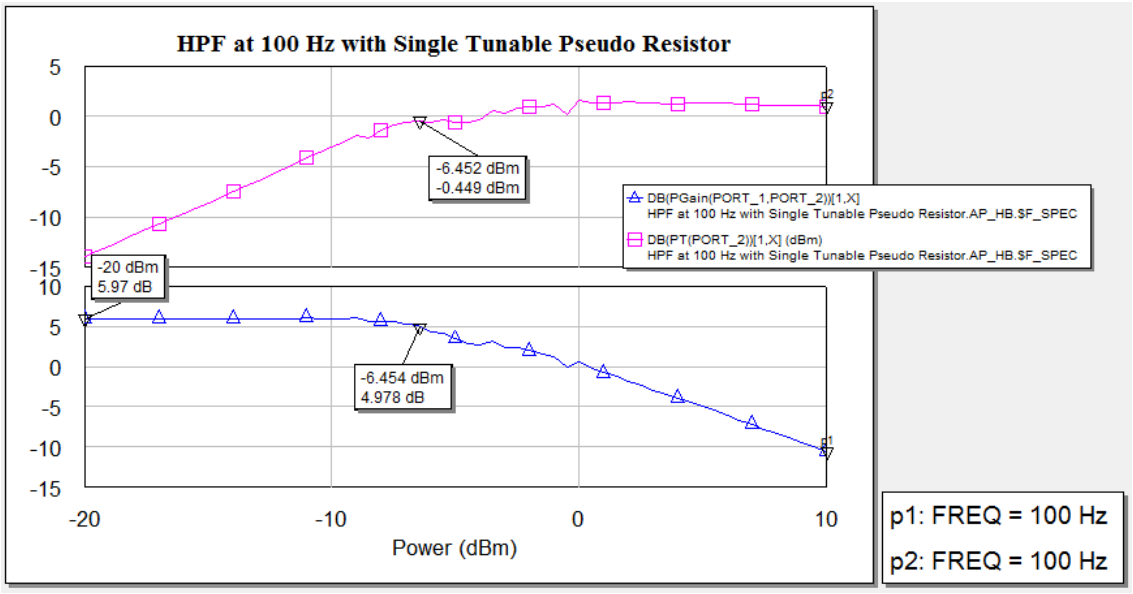


Figure 81: 1dB compression point for HPF using single tunable pseudo resistor

For high pass filter using single tunable pseudo resistor: $IIP_3 = 10 - 6.454 = 3.546\ dBm$

Assuming an input signal of 1µV is almost equal to -60 *dBm*.

$\left[V(dBm) = 20log\left(\frac{V}{1mV}\right)\right]$

To have a system as linear as possible, the amplitude of the fundamental should be as far as possible from the amplitude of the third order intercept point. Here the high pass filter provides better linearity in comparison with LPF.

The same procedure is followed for the LP and HP filters with double tunable pseudo resistors. This is shown in the following figures.

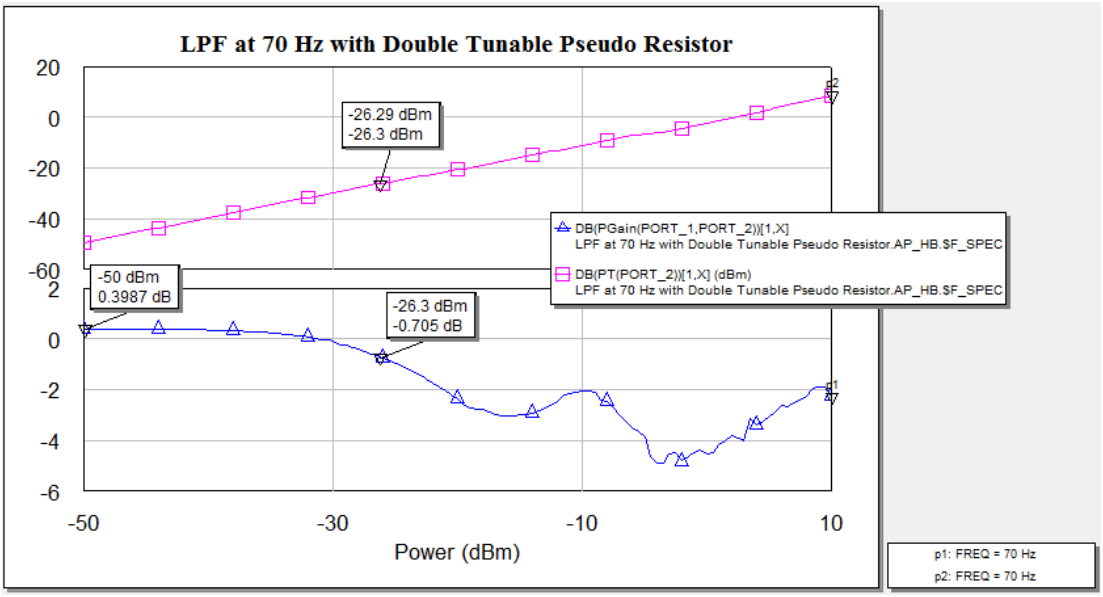


Figure 82: 1dB compression point for LPF using double tunable pseudo resistor

For low pass filter using double tunable pseudo resistor: $IIP_3 = 10 - 26.3 = -16.3\ dBm$

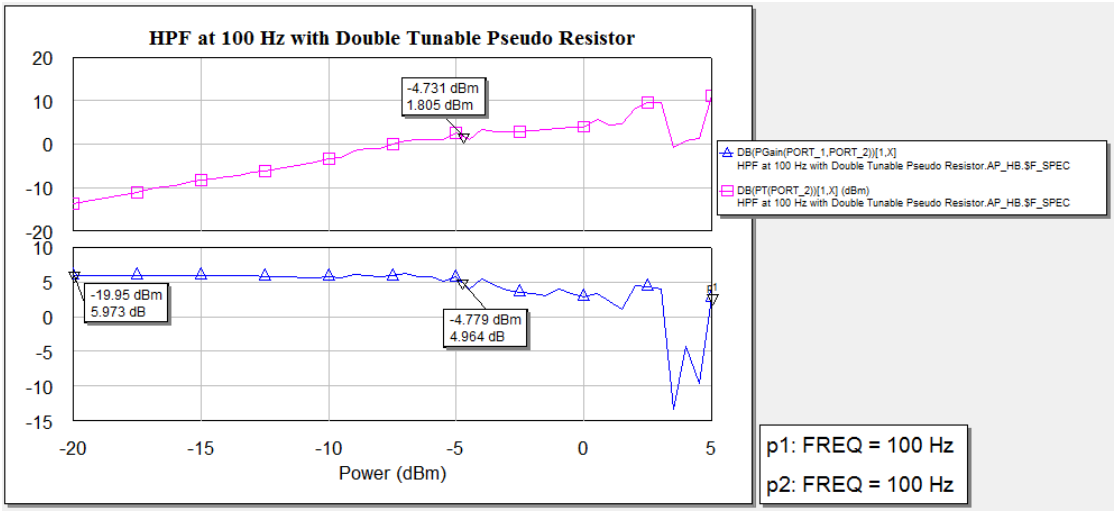


Figure 83: 1dB compression point for HPF using double tunable pseudo resistor

For high pass filter using double tunable pseudo resistor: $IIP_3 = 10 - 4.779 = 5.221\ dBm$

HPF filter provides better linearity in comparison with LPF.

Noise: The noise contribution of the system, here pseudo resistors, is mainly due to MOSFET thermal noise and Flicker noise. Thermal noise is the outcome of ohmic sections of MOSFET. The gate, source and drain material, exhibit finite resistivity, thus introducing noise. For a relatively wide transistor, the source and drain resistance are typically negligible whereas the gate resistance may become noticeable [6]. The most significant noise is generated in the channel which can be modeled by a current source connected between the drain and source terminals.

$$I_n^2 = 4KT\gamma g_m \tag{60}$$

Where K = $1.38*10^{-23}$ is the Boltzmann constant, T=300 is temperature in Kelvin, coefficient γ = and g_m is the transconductance of the transistor.

When the silicon crystal reaches an end at the interface between the gate oxide and the silicon substrate, many dangling bonds appear giving rise to extra energy states [14]. As charge carriers move at the interface, some are randomly trapped and later released by such energy states introducing flicker noise in the drain current. The flicker noise is modeled as a voltage source in series with the gate and roughly given by [6]

$$V_n^2 = \frac{K}{C_{ox}WL}.\frac{1}{f} \tag{61}$$

Where K is a process dependent constant on the order of 10^{-25} V^2 and one Hertz bandwidth is assumed around f. The inverse dependence on WL suggests that the device size should be increased in order to reduce noise. In addition to that PMOS devices exhibit less 1/f noise than NMOS transistors because the former carry the holes at some distance from the oxide silicon interface.

The following graphs show noise spectrum for output of LPF and HPF using single tunable pseudo resistor over the bandwidth of 100 Hz. In order to check the input and output noise generated by circuit elements the input is shorted to the ground and the output noise is measured. The input noise results from output noise divided by square of the gain of the system.

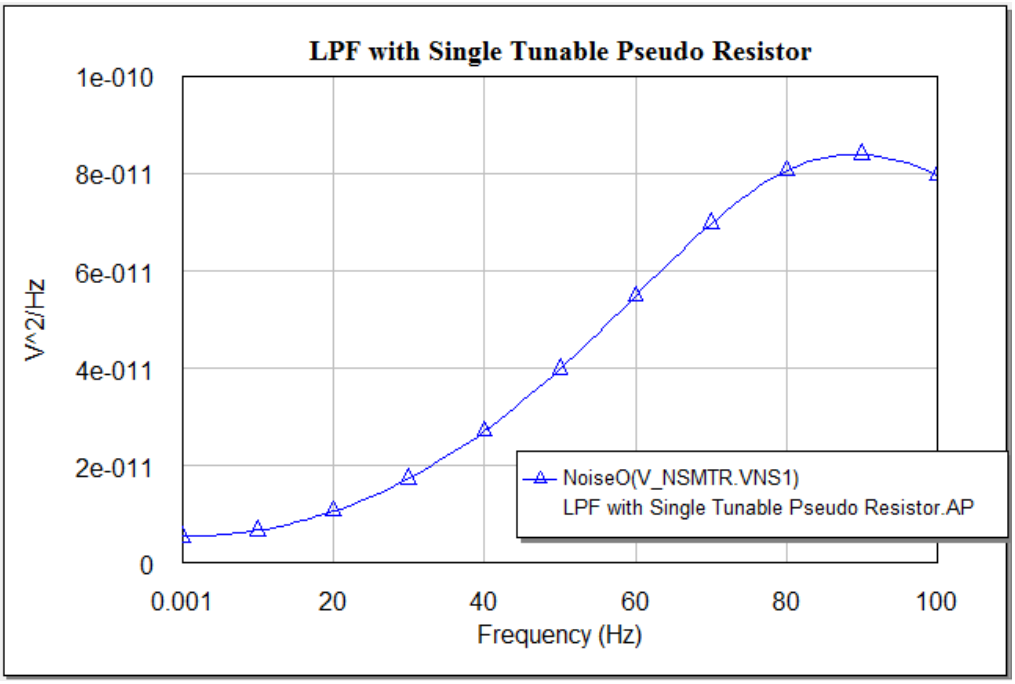


Figure 84: Output noise spectrum for LPF using single tunable pseudo resistor

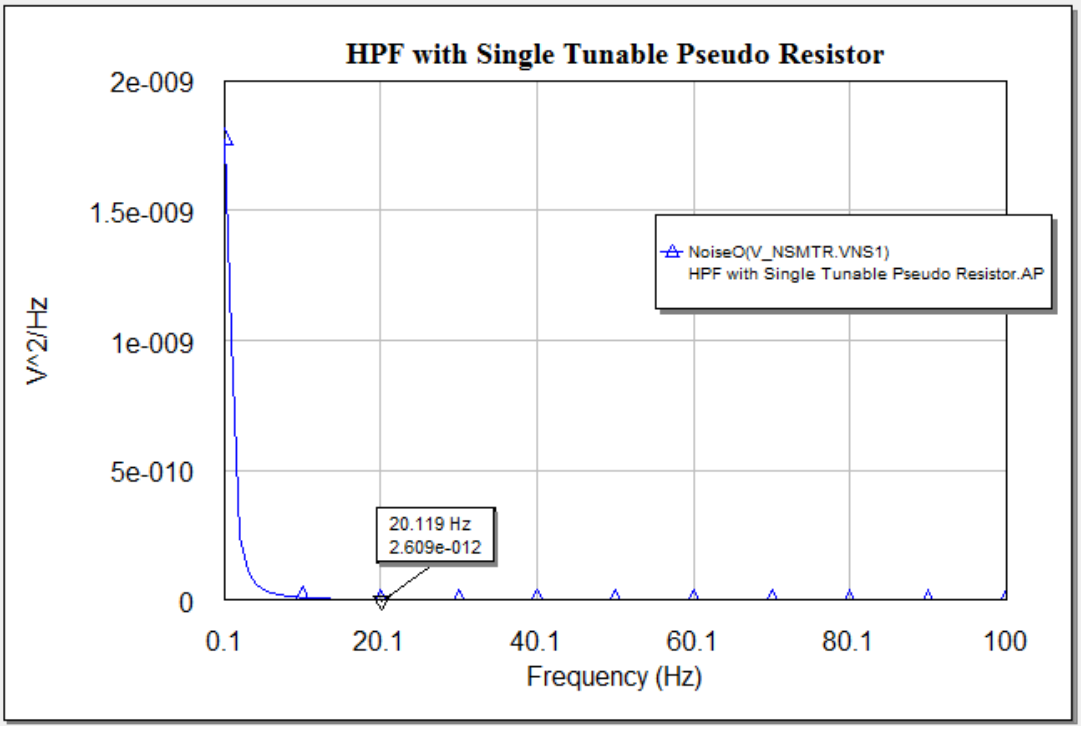


Figure 85: Output noise spectrum for HPF using single tunable pseudo resistor

The total noise power for output of LP and HP filters is the area under the curve for 100 Hz bandwidth in each case.

Since in low pass filter, the cutoff frequency is 100 Hz, the bandwidth required for noise measurement is up to 100 Hz.

Input noise power from LPF with single tunable pseudo resistor: **4.38 nV^2 → 66.2 µV**

Output noise power from LPF with single tunable pseudo resistor:**4.38n V^2 → 66.2 µV**

The input and output noise are equal due to the unity gain of the system.

In high pass filter the cut off frequency is 0.1 Hz, so we are interested in frequencies higher than this value. However since the result will be fed to the low pass filter later, only noise up to 100 Hz is considered in calculations.

Input noise power from HPF with single tunable pseudo resistor: **0.857 nV^2 → 29.3 µV**

Output noise power from HPF with single tunable pseudo resistor: **3.43n V^2 → 58.5 µV**

The input noise is calculated based on the output noise divided by the gain square which is 4.

The next two graphs illustrate the noise spectrum for LPF and HPF using double tunable pseudo resistor.

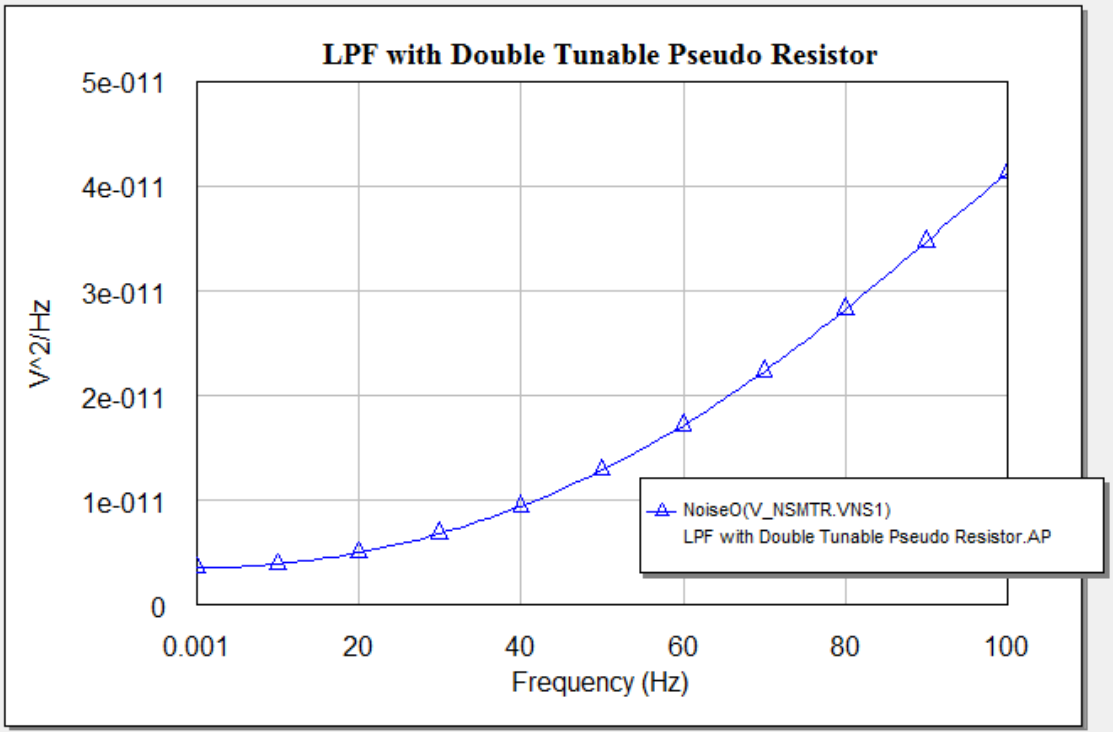


Figure 86: Output noise spectrum for LPF using double tunable pseudo resistor

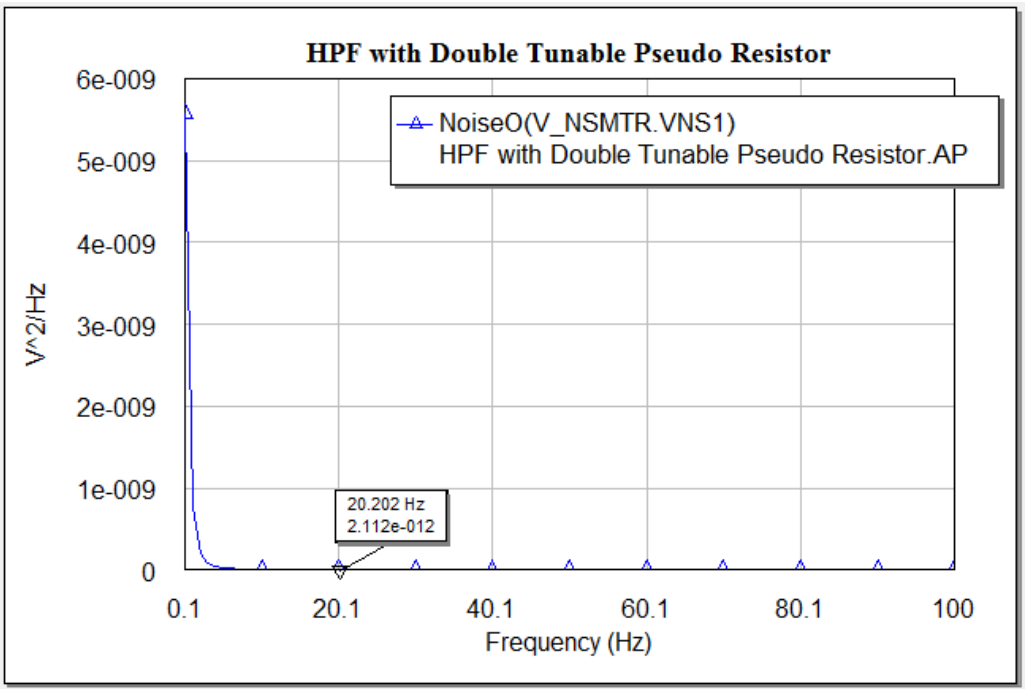


Figure 87: Output noise spectrum for HPF using double tunable pseudo resistor

The total noise power for output of LP and HP filters is the area under the curve for 100 Hz bandwidth in each case.

Since in low pass filter the cutoff frequency is 100 Hz, the bandwidth required for noise measurement is up to 100 Hz.

Input noise power from LPF with double tunable pseudo resistor: **1.65n V^2 → 40.6 µV**

Output noise power from LPF with double tunable pseudo resistor:**1.65n V^2 → 40.6 µV**

In high pass filter the cut off frequency is 0.1 Hz, so we are interested in frequencies higher than this value. However since the result will be fed to the low pass filter later, only noise up to 100 Hz is considered in calculations.

Input noise power from HPF with double tunable pseudo resistor: **1.71 nV^2 → 41.3 µV**

Output noise power from HPF with double tunable pseudo resistor:**6.84n V^2→ 82.7 µV**

Power Consumption: The power consumption of the pseudo resistor is calculated based on the biasing transistors. Accordingly in each case the current passing through the transistors in multiplied by the overall voltage.

Power consumption for single tunable pseudo resistor in 3rd order LPF:

P = IV = **17.061 nW** → V_{SD} = 3.3 V $I_D = 5.17*10^{-9}$ A

Power consumption for single tunable pseudo resistor in 3rd order HPF:

P = IV = **7.656 pW** → V_{SD} = 3.3 V $I_D = 2.32*10^{-12}$ A

Power consumption for double tunable pseudo resistor in 3rd order LPF:

P = IV = **14.982 nW** → V_{SD} = 3.3 V $I_D = 4.54*10^{-9}$ A

Power consumption for double tunable pseudo resistor in 3rd order HPF:

P = IV = **8.415 pW** → V_{SD} = 3.3 V $I_D = 2.55*10^{-12}$ A

CHAPTER 5

CONCLUSIONS

In this work, the concept of pseudo resistors has been utilized in the design of LP and HP filters successfully. Pseudo resistors are gate controlled MOSFETs that provide large values of resistors where the transistor is biased in weak inversion region. In such a transistor, the drain current saturates to its forward value as soon as V_S-V_D > 2U_T to 3U_T, Where U_T is the thermal voltage equal to 26 mV. In this case the transistor is saturated and the drain current is independent of the drain voltage, so the transistor can be modeled as a current source. However for values less that 3U_T the drain current is strongly dependant on drain voltage and the transistor acts as pseudo resistor. Given that different resistance is provided by tuning the gate voltage ,the pseudo resistors are called single tunable pseudo resistor if one MOSFET is used or double tunable pseudo resistor in case of employing two identical MOSFETs.

Both concepts have been used in design of LPF and HPF with cut off frequencies of 100 Hz and 0.1 Hz respectively. The results are perfectly matched with the expectations of the filters. In order to show consistency, not only third order but also first and second orders in both LPF and HPF were simulated. Then in each case the DC biasing has been replaced by a potential divider circuit to provide the proper DC basing needed for pseudo resistors. The results show that the desired cut off frequency in both filters is achieved accurately. Substituting the ideal capacitor and resistor elements in the filters by their AMS counterparts showed that there will be slight changes in the f_c if these values are not the same as ideal ones. In case of HPF all the components have the same size and as a result the same cut off frequency is achieved. However in case of LPF since different values of capacitors cannot match with the ideal ones slight difference in f_c of the third order LPF was shown in the results section. It is also illustrated that the system is very sensitive to gate voltage

variations so that small changes in the gate voltage can shift the cut off frequency drastically. This was shown in detail in the results section.

The HPF provides better linearity than LPF in both single and double tunable pseudo resistor based on 1 dB compression point as shown in the graphs in section 4.7; where in single tunable pseudo resistor (STPR) is 3.546 dBm and in DTPR is 5.22 dBm. In general the LPF and HPF employing double tunable pseudo resistor provide better linearity than in single tunable pseudo resistor as expected.

As explained in section 4.7, with the exception of the input noise in HPF with single tunable pseudo resistor which is 29.3 μV , the noise performance in both LP and HP with double tunable pseudo resistor is much better.

In terms of power consumption, both HPF and LPF with single and double tunable pseudo resistors are considered ultra low power devices since they consume tens of nW in LPF and tens of pW in HPF. To be more specific, the LPF with DTPR utilizes less power than in single tunable pseudo resistor which is 14.982 nW; where in HPF with single tunable pseudo resistor the power consumption is more. This power will be degraded when the ideal OP AMP is replaced by a real device by twice or three times of specified values but will still be categorized as ultra low power devices.

As part of the future work the ideal OP AMP can be replaced with a two stage operational amplifier .Moreover the biasing voltage for pseudo resistors may be replaced with more sophisticated circuits.

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APPENDIX A

Resistor and capacitor value calculation for third order LPF with f_C = 100 Hz

If C= 10 pF then for f_c= 100 Hz from the above equation R= 0.159 GΩ.

Resistor and capacitor value calculation for third order LPF with f_C = 0.1 Hz

If R= 0.159 G then

APPENDIX B

Second order HPF Gain and Q Factor:

Third order HPF Gain and Q Factor:

VITA

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