POWER CHARACTERISTICS OF SELECTIVE BURIED OXIDE MOSFET

by

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Dedication

I dedicated this thesis to my beloved family, I hope this achievement will make you proud of me and may GOD bless you all…

Abstract

Power dissipation is an important factor in electronic circuit design due to the decreasing feature size of microelectronic devices, high clock frequencies, and large die size, as well as the growing number of mobile, battery-operated systems. The aim of low-power design for battery-powered devices is thus to increase battery service life while meeting performance requirements. Reducing power dissipation is a design goal for portable and non-portable devices since extreme power dissipation results in increased packaging and cooling costs as well as potential reliability problems. Recently, Silicon On Insulator (SOI) devices have been used that exhibit vertical and horizontal isolation of active devices from the substrate, which leads to higher speed operation and low leakage current. However, SOI devices have serious drawbacks such as the kink effect and self-heating. In this thesis, a new Metal-Oxide Semiconductor Field-Effect-Transistor (MOSFET) structure design is introduced to eliminate the kink effect and self-heating, and to reduce power dissipation while still keeping in consideration the advantages of others such as Bulk and SOI MOSFETs. The new structure is called SELective Buried OXide MOSFET (SELBOX). This transistor combines the advantages of the Bulk and SOI while eliminating the drawbacks.

This thesis reviews the various power dissipation reduction methods available in the literature. Next it proposes the structures of Bulk, SOI, and SELBOX for NMOS, PMOS, and CMOS over the first stage followed by a simulation to obtain current-voltage characteristics and static power dissipation. The various MOSFET structures are evaluated in terms of power dissipation. Simulation results will show that the static power dissipation of the Bulk MOS as a single transistor is less than others due to the slow increase in the drain current. Also, SELBOX behavior is very close to Bulk with the advantages of SOI. Simulation results of the CMOS devices show that the static power dissipation of Bulk MOS is very high due to well leakage. SOI has the lowest power dissipation and SELBOX is very close to it. In all cases, SELBOX structure succeeded in reducing power dissipation with a high operating speed, elimination of self-heating, and without a kink effect.

Search terms: *Bulk, SOI, SELBOX, kink effect, self-heating, power dissipation, internal capacitance, threshold voltage.*

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List of Abbreviations

MOSFET	-	Metal-Oxide-Semiconductor Field-Effect-Transistor
SELBOX	-	Selective Buried Oxide MOSFET
CMOS	-	Complementary Metal Oxide Semiconductor
NMOS	-	N-channel MOSFET
PMOS	-	P-channel MOSFET
SOI	-	Silicon On Insulator
PD SOI	-	Partially Depleted Silicon On Insulator
FD SOI	-	Fully Depleted Silicon On Insulator
IC	-	Integrated Circuit
RDF	-	Random Dopant Fluctuation
SHE	-	Self-Heating Effect
CL	-	Active Load

Chapter 1: Introduction

Microelectronic integrated circuit chip complexity continues to increase with more added operations, which require more power consumption. In modern mobile communication systems, there are several operations taking place in one device including video streaming, multimedia operations, Wi-Fi connections, memory transfer, and computer programs. These operations increase power dissipation and decrease efficiency, and may even damage the system. Therefore, power dissipation reduction is required to increase battery life, reduce energy costs, reduce the use of natural resources, and increase system reliability.

1.1 Problem statement

Static Complementary Metal Oxide Semiconductor (CMOS) devices in relatively long transistor channel technologies are very power efficient. But, in modern technologies, static power consumption is a primary design constraint because of the gradually decreasing transistor feature size. Technology scaling is increasing both the relative and absolute contributions of static power dissipation [1]. A closer look at the current state of the art technology will reveal that static power dissipation is growing at a faster rate than dynamic power dissipation. Before few processor generations, the curves were intersected as shown in Figure 1.

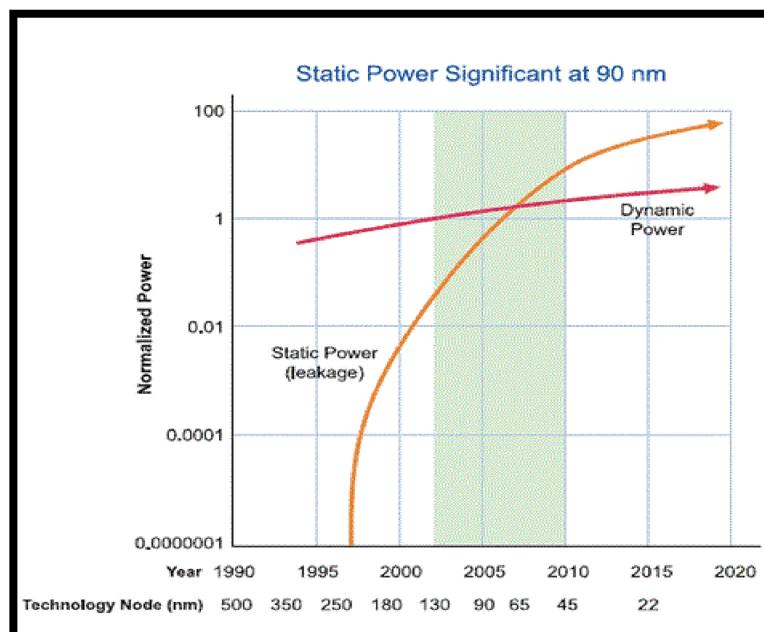

Figure 1: Increasing power dissipation at shrinking process nodes [2]

Using scaling theory, Borkar predicts that leakage power increases five times every generation, while active power remains approximately constant [3]. Because leakage current flows from every transistor that is powered on, with decreasing die sizes and integration, static power will become an important part of the total consumed power.

Static power dissipation happens due to the following: subthreshold conduction during the OFF state of the transistors, tunneling current through the gate oxide layer, leakage through the reverse-biased diodes, and contention current in rationed circuits. In this thesis, we will focus on subthreshold conduction, which has a valuable effect on power dissipation and is reversely proportional to the gate size. In this region of operation, the gate voltage has exceeded the weak inversion point, but is still below the threshold voltage. Subthreshold conduction will be explained in detail in Chapter 2.

Several efforts have been made to reduce power dissipation, including changing the architecture of the circuit design. These efforts were successful, but they also had a significant drawback by increasing the cost and density on chips. One of these techniques is the stack effect method [4] [5] [6], where the subthreshold leakages can be reduced by forcing series transistors to be simultaneously off, or using reverse body biasing to increase threshold voltages. Another method is called the several dual-threshold voltage technique [7] [8]. In this technique, the threshold voltages of the transistors stay with no changes during the active mode. However, during the standby mode, the threshold voltages of the transistors increase so the leakage current is reduced. A switched-source-impedance (SSI) CMOS circuit was also proposed as a way to reduce the exponential increase of the leakage current with changing the threshold voltage [9].

For logic circuits, there are several proposed techniques, one of which is the sleep approach method [10] [11] [12]. In this technique, an additional "sleep" PMOS transistor is located between the supply and the pull-up network of a circuit, and an additional "sleep" NMOS transistor is located between the pull-down network and the ground. These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is in active mode and turned off when the circuit is in sleep mode. Another method for logic circuits is inserting an extra

transistor in the large leakage path [13]. This procedure reduces the leakage current by reducing the applied input. There was a journal article published in the same year, which discussed leakage minimization using minimum leakage vector (MLV) control [14] [15], in this technique, the leakage reduction is done only when the circuit is in standby mode.

Going back to analog circuits, the GALEOR (gated leakage transistor) method is proposed to reduce the static power dissipation in CMOS [16]; this technique requires an additional two transistors for each CMOS. There were also techniques done by changing something in the transistor such as using a low voltage supply [17] [18] [19] [20] [21]. This method is about choosing an accepted low voltage supplier so that the threshold voltage will decrease and according to this change, the leakage current will be reduced. Another proposed method involves resizing the gate of the MOSFET [22] [23]. Other authors introduced papers which suggested increasing gate oxide thickness [24] [25] [26] [27]. A modern design for logic circuits was introduced [28]. The design employs dynamic voltage scaling to reduce the leakage power and it recalls the data during the no action mode. The main idea behind this technique is that it uses two leakage control transistors with different ground levels. These Three techniques helped to reduce the power dissipation effectively.

Different fabrication techniques were also presented, such as designing new fully depleted silicon on insulator (FD SOI) [29]. This process is done practically and it helped to reduce power dissipation. However, it also has disadvantages that cannot be ignored, like the kink effect and the self-heating effect. After that, the fabricated transistor was improved by designing the Double Gate MOSFET [30] [31]. This transistor was then used in circuits with an auxiliary MOSFET [32]. In [33], the dynamic threshold-voltage SOI transistor was introduced. All these techniques will be briefly explained in Chapter 3 with their advantages and drawbacks. The approach that will be presented here takes another viewpoint, changing the fabricated SOI to another structure which can eliminate the disadvantages and combine the Bulk's and SOI's advantages. This method will save both money and space.

1.2 Thesis methodology and outline

To illustrate how circuit design can reduce power dissipation, consider the power dissipation in a standard N-channel Metal-Oxide-Semiconductor (NMOS) with channel length equal to 0.4 µm used in an inverter circuit. Using computer simulation, it is observed that during the ON state, an average power of 0.5 mW is consumed. This power value drops to around 4 nW during the off state when the gate source voltage V_{GS} is reduced to 50% of the threshold voltage V_{TH} and the drain source voltage V_{DS} is less than 3.5 V as shown in Figure 2. To reduce power dissipation further, a Complementary Metal Oxide Semiconductor (CMOS) circuit is used.

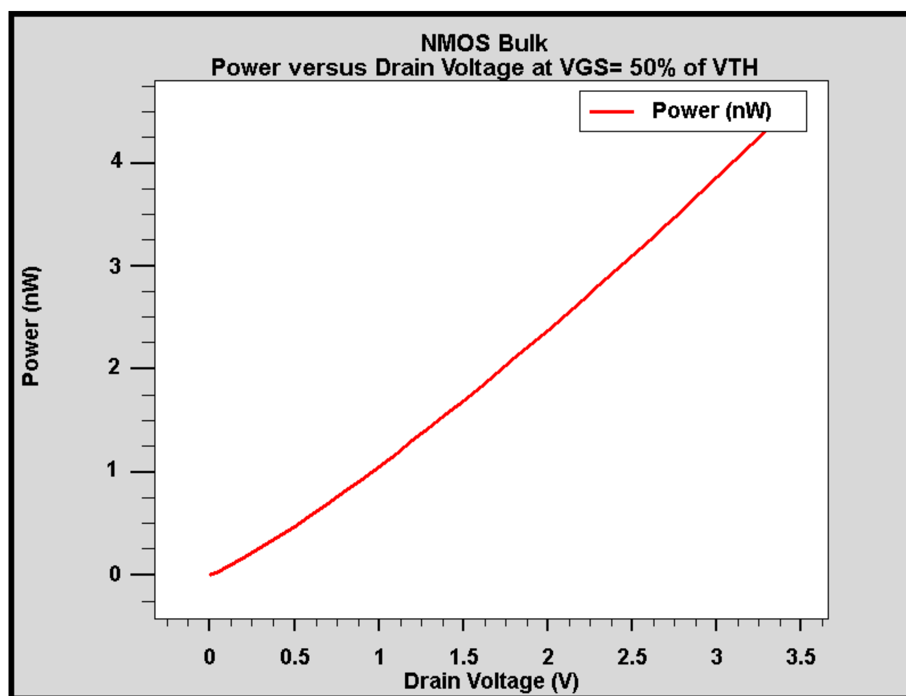

Figure 2: Power dissipation of N-channel Bulk MOSFET at V_{GS} = 50% of V_{TH}

The CMOS dissipates power when both transistors are on during the short switching time period. In a typical ON/OFF operation, the total average power dissipation in a CMOS with channel length equal to 0.4 µm would be in the order of 0.35 nW at V_{GS} close to V_{TH} [34]. This relatively low power value illustrates the effectiveness of the circuit solution in reducing power dissipation.

One main factor in CMOS static power dissipation is the leakage current which occurs due to the subthreshold conduction during the off state of the transistor, where the current leakage flows from drain to source in the cutoff state ($V_{GS}<V_{TH}$). Furthermore, ideally there should be no leakage through the isolated gate oxide layer but typically there will be some, called “tunneling current”. There is also leakage through the reverse biased diodes, where leakage happens between diffusion regions and wells or between the substrates and wells. This leakage is very small compared to the sub threshold and tunneling currents [35].

Unfortunately, the Bulk MOSFET shown in Figure 3 has some disadvantages including high power dissipation, current leakage, low speed in operation due to the high internal capacitance, and short channel effects.

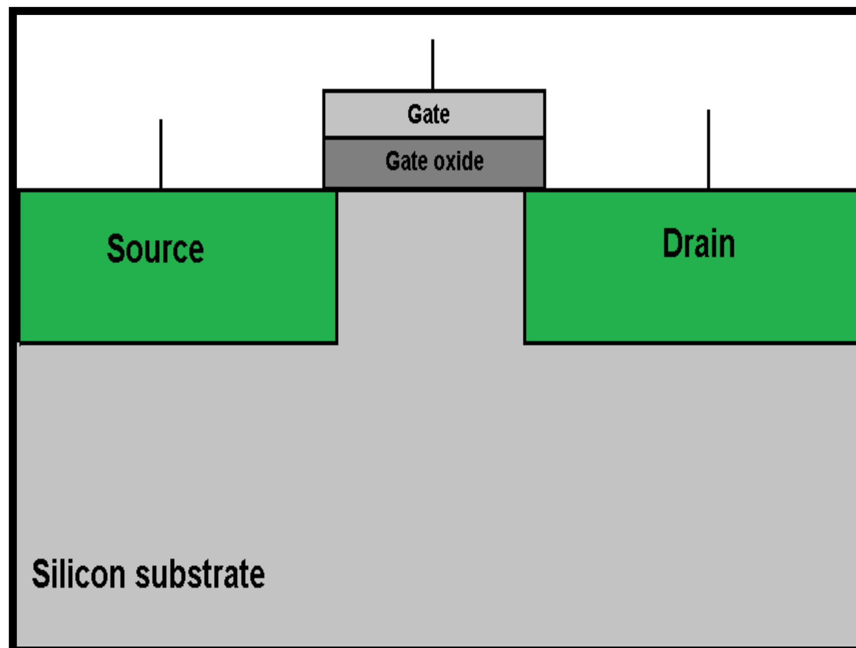

Figure 3: Bulk MOSFET structure

To solve these issues, the SOI MOSFET shown in Figure 4 was introduced. The SOI has succeeded in reducing leakage current, increasing the speed of operation due to the reduction in the internal capacitance (specifically the drain-body capacitance), and reducing the short channel effects [36] [37]. Nevertheless, the SOI has several disadvantages including the kink effect, high power dissipation, and self-heating.

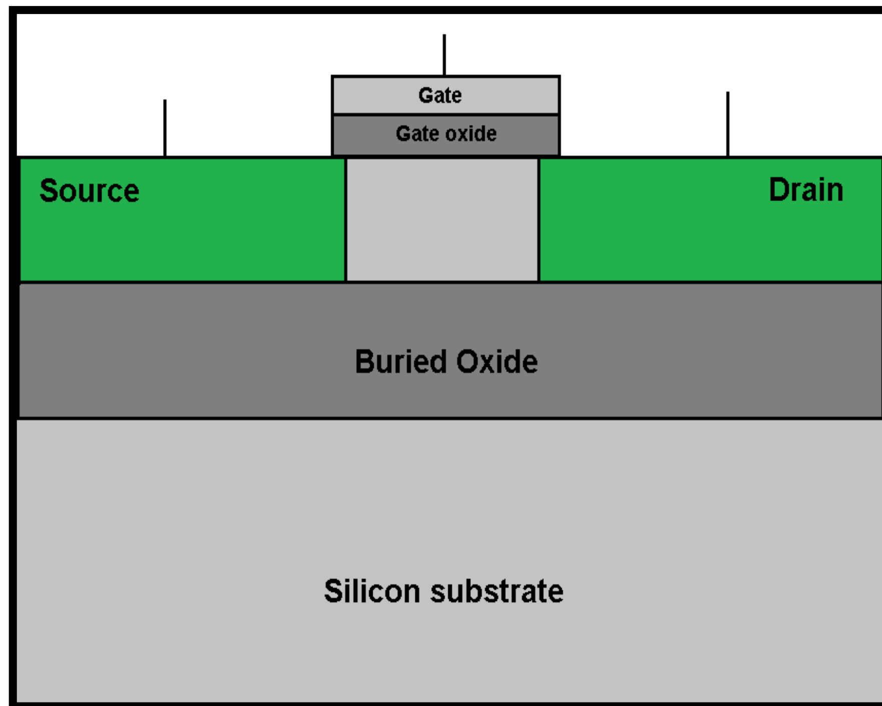

Figure 4: SOI MOSFET structure

The SOI device consists of a dielectric layer between the two silicon layers; the dielectric layer can be made of silicon dioxide. The top layer is known as the active layer and the bottom layer provides mechanical support. SOI devices are fabricated on the top layer as shown in Figure 4.

There are many advantages of SOI devices including reduction in the parasitic capacitances that improves the operation speed. The gate capacitance remains the same but with the buried oxide the parasitic capacitances in bulk MOSFETs will be reduced: C_{GS}, C_{SS}, and C_{DS}. Also, SOI devices have vertical isolation so that they are isolated by dielectrics from each other and also from the underlying substrate, which eliminates leakage. In addition, isolation from the substrate and from the adjacent devices in the SOI CMOS gives the units a chance to function without latch up issues and increases the density of integration. In the radiation field, the radiation is minimized in SOIs due to the reduction in the exposed silicon volume. The active silicon is very thin in SOI devices, so the majority of the charges that are generated by the radiation will exist in the lower substrate and will be blocked by the buried oxide. Hence, it will not affect the charges in the active layer.

However, there are some disadvantages of SOI devices such as self-heating that happens in fully depleted (FD) SOIs and the partially-depleted (PD) SOI devices, and the kink effect, that happens only in PD SOI devices. The kink effect causes nonlinearity in the device due to the sharp increase in the drain current due to the increase in the body potential and the associated drop in threshold voltage. This operation happens because of the high electric field near the drain due to high drain voltage as shown in Figure 5.

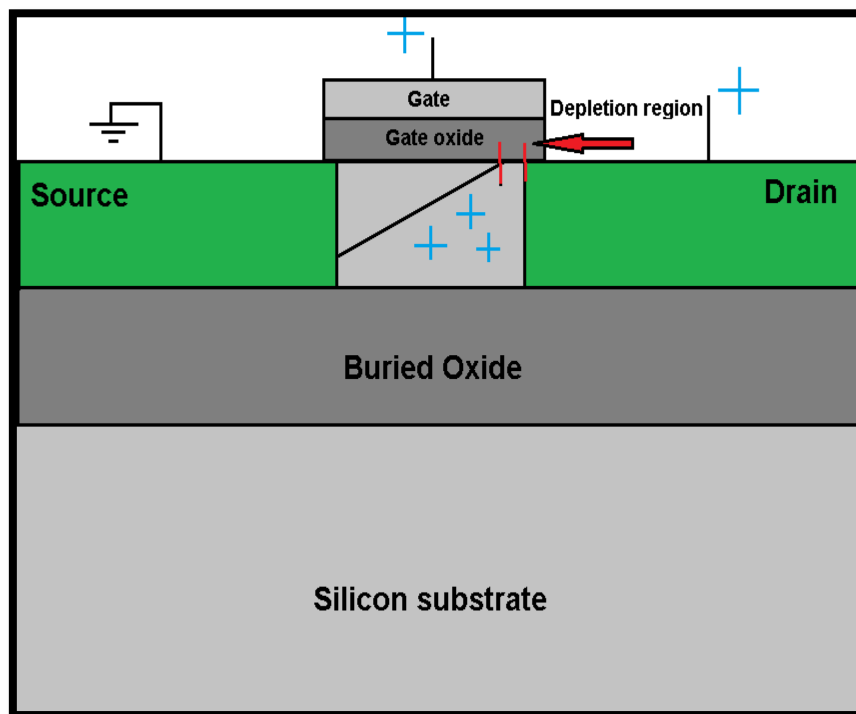

Figure 5: Kink effect in SOI

To reduce the kink effect and to have better performance in power dissipation, a selective buried oxide (SELBOX) MOSFET was introduced as shown in Figure 6. The solution to the kink effect was explained in [38].

Instead of covering the region below the device from the lower substrate completely with oxide, we cover the regions below the drain, the source, and parts of the region below the channel leaving a small gap under the channel to minimize the increase in the body potential. That will lead to reduction in the kink effect; this reduction depends on the selection of the gap width.

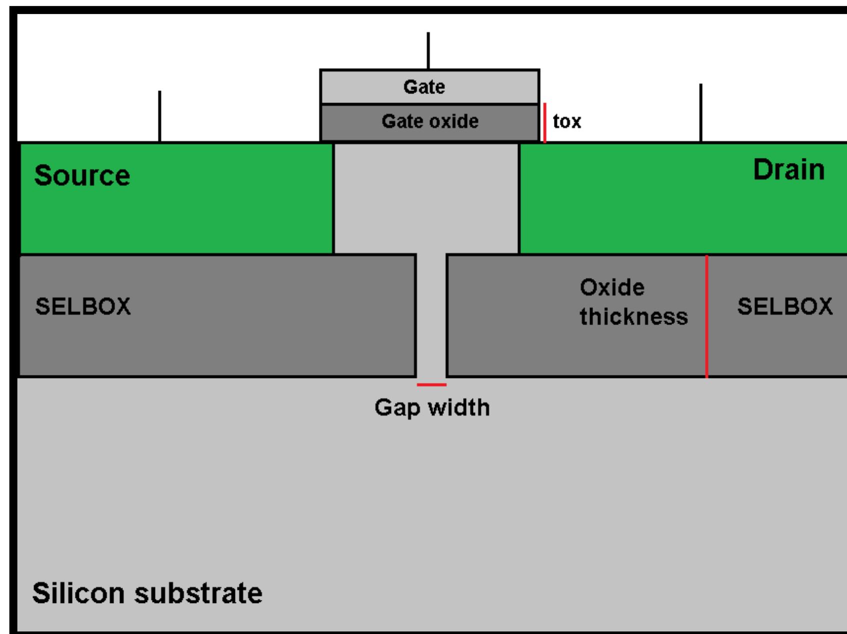

Figure 6: SELBOX MOSFET structure

The SELBOX is fabricated by following a specific procedure [39] [40]:

1. Silicon is used as a basic material for the substrate. Substrate is converted to P-substrate if an NMOS is going to be fabricated or N-substrate if a PMOS is going to be fabricated.
2. Box layer is inserted in several steps:
    a. A thermal oxide layer is placed over the channel region as a mask with its width proportional to the gap width.
    b. The masked wafer is implanted with oxygen ions. The depth of the oxygen ions depends on the energy used in implantation.
    c. The mask is removed and the substrate is heated to convert the oxygen implanted layer to an SIO_2 layer to yield the SELBOX substrate as shown in Figure 7.
3. Oxidation over the wafer is done by using high-purity oxygen and hydrogen at 1000 degree centigrade.
4. Polysilicon is deposited over the gate oxide layer to create a connected gate.
5. The oxide layer is removed except the small area of the Gate.
6. Oxidation process is done again to form an oxidation layer on the wafer with small region for the formation of the gate.

7. Masking and diffusion are done by making small areas for the purpose of diffusion then dopants are diffused or ion implanted to create the drain and source terminals.
8. The remaining oxidation layer is removed.
9. Thick field oxide is formed in all regions except the terminals of the device.
10. Metallization is done by inserting aluminum on the whole wafer.
11. The excess metal is removed from the wafer layer.
12. The terminals of the device are made and labeled with their names.

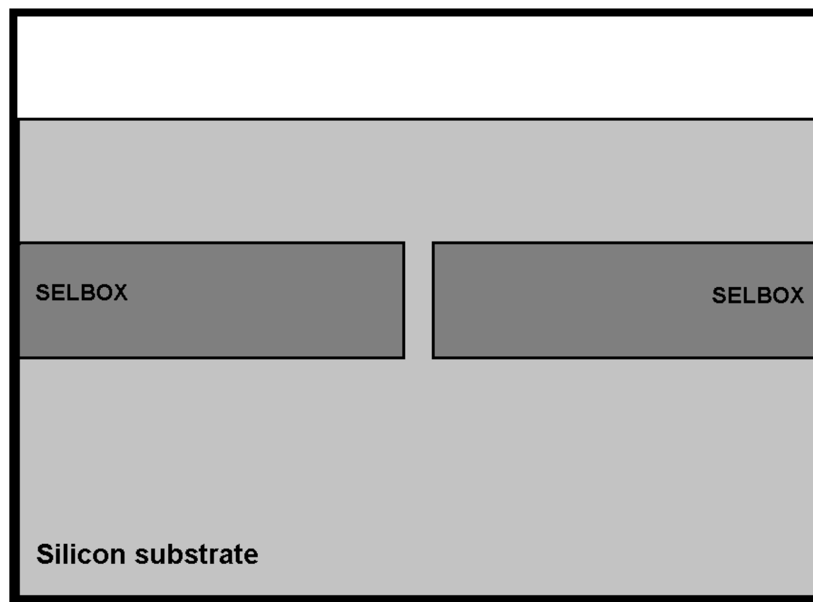

Figure 7: SELBOX substrate

After these steps, the structure will be ready for testing as shown in Figure 6.

In simulation, all previous steps are done to build the structure except the box is inserted in a different way – the silicon has to be etched from the desired places where the box will be fixed. The area under the channel where the gap has to be is kept filled with silicon, and then the oxide layer is injected in the substrate from the two edges to fill the etched parts.

SELBOX, as mentioned earlier, has a small gap with length equal to 10% of the channel length. This gap helps the lower part of the substrate to absorb the holes generated by the electric field in the depletion region and keep them away from the channel as shown in Figure 8. As a result, the device will have a body voltage lower

than the SOI and the kink effect will be eliminated. SELBOX also reduces the self-heating effect [41]. The gap will reduce thermal connections by working as a parallel low resistor so the overall resistance will be reduced as shown in Figure 9. SELBOX works as a Bulk but with high speed in operation due to the low internal capacitance and with reduced short channel effect. In the next chapters, SELBOX will be illustrated briefly.

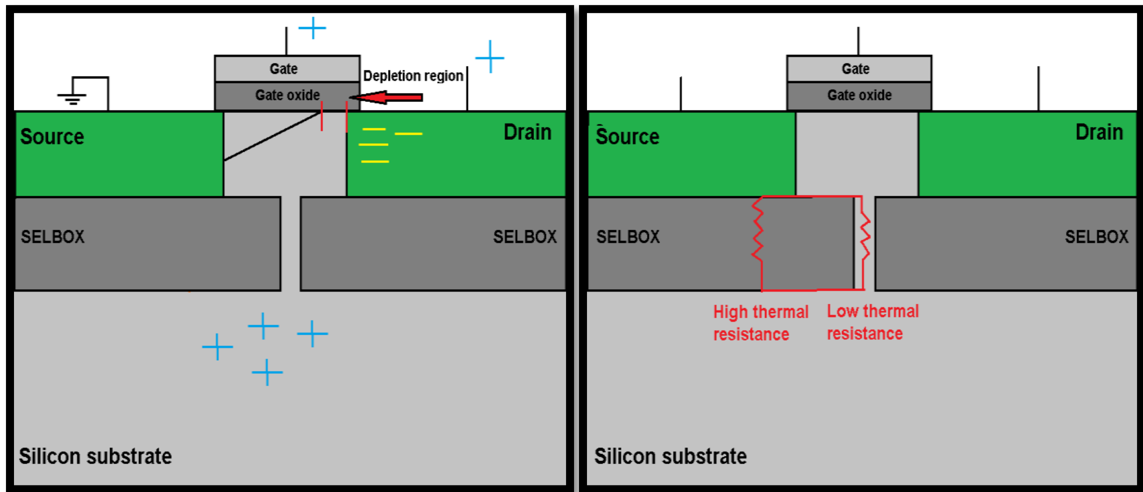

Figure 8: Kink effect reduction in SELBOX

Figure 9: Self- heating reduction in SELBOX

1.3 Thesis organization

In this thesis, an introduction about different types of MOSFETs will be discussed with illustrating their power dissipation. After that, a literature review about different efforts which were done to reduce power dissipation will be presented. Then, the proposed method with the needed mathematical models will be shown followed by description of the devices and the results.

The rest of the thesis is organized as follows:

Chapter 2 provides information about the Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) that is required to understand the topic. Bulk MOSFETs and Silicon on Insulator (SOI) MOSFETs are introduced.

Chapter 3 includes the literature review conducted on various existing techniques used to solve the power dissipation problem. Many approaches are presented on the

design of the circuit. The advantages and drawbacks of each of these techniques are also briefly mentioned in this chapter.

Chapter 4 introduces the device parameters. The parameters used in this study are related to the standard parameters published in various literature sources.

Chapter 5 covers the power dissipation of single devices. The NMOS and PMOS are shown with their current-voltage and power characteristics. Bulk Structure will be introduced followed by the SOI and the proposed SELBOX structure, respectively.

Chapter 6 presents the power dissipation of the CMOS device. Bulk Structure will be illustrated, followed by the SOI and the proposed SELBOX structure, respectively.

Chapter 7 includes the conclusion with some recommendations for future work.

Chapter 2: MOSFET Devices

2.1 Introduction

A Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is the building block of integrated circuits (ICs). Today's most complex ICs, such as microprocessors, graphics, and digital signal processing chips, have about 1.4 billion transistors, each measuring down to 22 nm [42]. Intel's recent road map shows that they have developed a 14 nm transistor [43].

2.2 History

The idea behind MOSFET was developed before 1930. In 1926, Julius Lilienfeld filed a patent describing a three-electrode amplifying device based on the semiconducting properties of copper sulfide. Challenges to building such a device continued through the 1930's [44]. However, it was not successfully produced until 1959 when Mohammad Attalla and Dawon Kahng proposed their successful MOSFET at Bell Labs [45]. The main problem was control and reduction of the surface states at the interface between the oxide and the semiconductor. The MOSFET transistor evolved from the P-channel MOSFET in the 1960's to the N-channel MOSFET in the 1970's [46].

2.3 MOSFET technology

In MOSFETS, there are fundamental parameters that have to be taken into consideration. These parameters include threshold voltage, body effect, channel length modulation, subthreshold leakage, and internal capacitance. In this section, the parameters are discussed briefly.

2.3.1 MOSFET threshold voltage.

The threshold voltage is a major parameter for MOSFET characterization and modeling [47]. This parameter may be understood as the gate voltage at which the transition between the OFF and ON modes takes place in the MOSFET channel [48].

In an N-channel MOSFET, the substrate is P-type silicon containing positively charged mobile holes. When a positive charge is applied to the gate, an electric field

causes the holes to be repelled from the interface, creating a depletion region containing negatively charged immobile ions. When the gate voltage increases further, the electron concentration will increase at the silicon interface surface (inversion layer). The gate voltage at which the electron density at the interface surface is the same as the hole density in the bulk material is called the threshold voltage. In other words, the threshold voltage is the voltage at which there are sufficient electrons in the inversion layer to make a low resistance conducting path between the MOSFET source and drain. When the voltage between the transistor gate and source (V_{GS}) exceeds the threshold voltage (V_{TH}), it is known as overdrive voltage [49].

The threshold voltage is affected by the following factors [50]:

1. Oxide thickness: the thinner the oxide thickness, the lower the threshold voltage
2. Temperature.
3. Random Dopant Fluctuation (RDF): a form of process variation resulting from variation in the implanted impurity concentration.

For the Bulk MOSFET, the threshold voltage is calculated as follows [50]:

$$V_{TH} = \Phi_{ms} + 2\,\Phi_f + \frac{\sqrt{2qN_S * 2|\Phi_f|\varepsilon_s}}{C_{ox}} \quad (1)$$

where V_{TH} is the threshold voltage in volts, Φ_{ms} is the metal-semiconductor work function difference in volts, Φ_f is the difference in voltage between two energy levels (Fermi and intrinsic Fermi) in volts, N_S is the doping concentration of substrate in cm^{-3}, q is the electric charge density in coulombs, ε_s is the permittivity of silicon in F/m, and C_{ox} is the oxide capacitance in F/m^2.
The metal-semiconductor work function difference equation is

$$\Phi_{ms} = \Phi_m - \left(X_s + \frac{E_g}{2q} + \Phi_f \right) \ \text{(V)} \quad (2)$$

where

$$\Phi_f = \frac{KT}{q} \ln \frac{N_S}{n_i} \ \text{(V)} \quad (3)$$

where K is Boltzmann's constant in J/K, T is temperature in degrees Kelvin, X_s is electron affinity of the semiconductor in volts, E_g is the conduction band energy in

joules, q is the electric charge density in coulombs, Φ_m is the bulk potential in volts, and n_i is the intrinsic doping concentration in cm^{-3}.

The Oxide capacitance equation is

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \ (F/m^2) \quad (4)$$

where ε_{ox} is the permittivity of oxide in F/m, and t_{ox} is the oxide thickness in meter.

2.3.2 MOSFET body effect.

The MOSFET body effect is the influence of the body to source voltage in the threshold voltage of the MOSFET.

If a body to source voltage greater than zero is used, a decrease in threshold voltage and an increase in the drain current will happen.

If a positive gate to source voltage is applied, then an inversion layer will be gotten. Furthermore, if a positive source to body voltage is applied, then reverse bias will happen: the width of the inversion layer will increase, and the inversion charges will also increase [51].

The body effect upon the channel can be described using a modification of the threshold voltage, approximated by the following equation [52]:

$$V_{TB} = V_{T0} + \gamma \left(\sqrt{V_{SB} + 2\varphi_B} - \sqrt{2\varphi_B}\right) \quad (V) \quad (5)$$

where V_{TB} is the threshold voltage with substrate bias present in volts, V_{T0} is the zero-value of threshold voltage in volts, γ is the body effect parameter in $V^{1/2}$, V_{SB} is the source-body voltage in volts, and $2\varphi_B$is the approximate potential drop between surface and bulk across the depletion layer in volts when $V_{SB} = 0$ and gate bias is sufficient to ensure that a channel is present.

2.3.3 Channel length modulation.

Channel length modulation happens when the drain voltage increases, causing the width of depletion region to rise. As a result, the channel length will drop, and the drain current will increase as we increase the drain to source voltage as shown in Figure 10.

When the device is operated in saturation (drain to source voltage is greater than saturation drain voltage), the channel gets pinched off and the depletion region will be extended into the inversion layer. Electrons in the channel will move quickly and will enter the depletion region before reaching the drain. If the drain voltage is high, then the electric field in the space charge region will be strong. The magnitude of the electric field depends on the drain to source and the saturation drain voltages. Electrons gain energy from the electric field as they drift towards the drain inside the depletion region. These electrons will generate secondary electron-hole pairs through impact ionization [53].

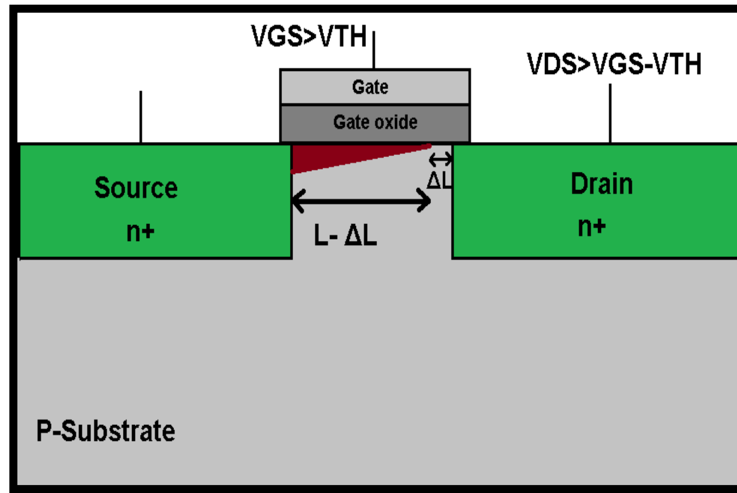

Figure 10: Channel length modulation

2.3.4 Subthreshold leakage.

Leakage power dissipation has become a significant part of the total power dissipated in modern technologies. It is expected that by the year 2020, leakage power is going to increase 32 times per device. Subthreshold leakage current is one of the most dominant leakage current components. It is the drain-to-source leakage current when the transistor is off, if the applied voltage V_{GS} is less than the threshold voltage V_{TH} of the transistor [54]. The following equation relates subthreshold current I_{SUB} with other device parameters:

$$I_{SUB} \approx \alpha \frac{1}{L_{EFF}} exp(\frac{q(V_G - V_T)}{kT}) \qquad (6)$$

where α is constant, L_{EFF} is the effective length in meters, V_G is the input voltage in volts, V_T is the threshold voltage in volts, and $\frac{kT}{q}$ is the thermal voltage in volts.

From the equation we can note that the subthreshold current depends on the transistor parameters as shown in Table 1.

Table 1: Dependence of subthreshold leakage on device parameters

Parameters	Dependence
Transistor effective length (L_{EFF})	Inversely proportional
Thermal voltage ($\frac{kT}{q}$)	Exponential decrease
Difference between input voltage (V_G) and Transistor threshold voltage (V_T)	Exponential increase

The previous parameters face many challenges nowadays because of shrinkage in device sizes. To solve some of these challenging issues, the Silicon on Insulator (SOI) was fabricated. The next section will introduce this device.

2.3.5 Internal capacitance.

It is an inescapable and usually annoying capacitance that exists between the parts of an electronic device as shown in Figure 11. Internal capacitance is divided into two categories: gate capacitance and junction capacitance [55].

The first category is gate capacitance, where the gate electrode forms a parallel plate capacitor with the channel and with the other electrodes using the oxide layer as a dielectric. We have a gate-source capacitor (C_{gs}), gate-drain capacitor (C_{gd}), and gate-body capacitor (C_{gb}).

The second category contains the source-body and drain-body depletion-layer capacitances. When the capacitance of the reverse-biased P-N junction is formed by N-source and P-substrate, source diffusion (C_{sb}) will happen. But when the capacitance of the reverse-biased p-n junction is formed by N-drain and P-substrate, drain diffusion (C_{db}) will occur. These capacitances are presented based on the changes in the charges associated with the space charge regions.

Primary device operation is achieved through the action of the gate capacitance. The junction capacitors in the device are undesirable, which sets an upper limit to the operating speed of the device.

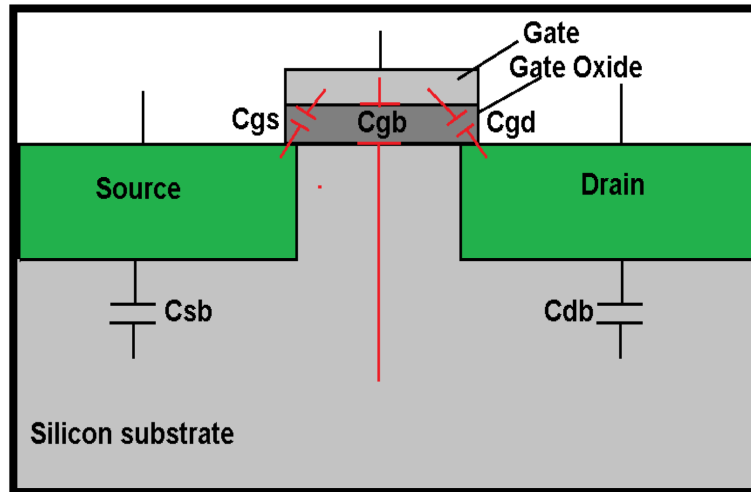

Figure 11: Distribution of the internal capacitances in Bulk MOSFET

2.4 Silicon on Insulator (SOI)

SOI Structure Consists of a buried oxide (BOX) layer between two silicon layers; the layer is made of silicon dioxide. The top layer is known as the active layer and the bottom is known as the mechanical support. SOI devices are fabricated on the top layer.

The single gate SOI MOSFET is divided into two categories [38]: partially depleted silicon on insulator (PD SOI MOSFET), and fully depleted silicon on insulator (FD SOI MOSFET).

In PD SOI MOSFETs, the depletion region does not reach through the entire silicon channel/body region. The thickness of silicon above silicon dioxide is greater than twice the width of the depletion region. The applied gate voltage will never deplete the active silicon completely. It is known also as the thick film device because the active silicon thickness is greater than 0.15 µm.

In FD SOI MOSFETs, the silicon thickness is less than 0.1 µm. The active silicon layer is thin enough so the gate voltage can deplete it completely. These are also called thin film devices.

The PD SOI MOSFET is more interesting than the FD SOI MOSFET in fabrication because the thickness of PD is close to the bulk silicon thickness and also the threshold voltage is less sensitive to uniformity of silicon thickness. In FD SOI MOSFETs, the threshold voltage depends on the thickness and also the ultra-thin film is difficult to control. But in PD, the kink effect is observed which is considered a disadvantage.

2.4.1 Advantages and disadvantages of SOI devices.

In this part, the advantages and drawbacks of SOI devices are briefly illustrated [56] [57] [58] [59] [60].

- **Advantages of SOI devices**

1. Reduced capacitance

SOI offers reduction in the parasitic capacitances which improves the operation speed. The gate capacitance remains the same but with buried oxide; the parasitic capacitances in bulk MOSFETs will be reduced: C_{gb}, C_{sb}, and C_{db}.

As shown in Figure 12, SOI can reduce the capacitance at the drain and source junctions significantly by eliminating the depletion regions extending into the substrate. This results in a reduction in the RC delay due to parasitic capacitance, and hence a higher speed performance of the SOI CMOS devices compared to bulk CMOS.

2. Latch up free operation

Latch up is a type of short circuit. It is the result of a low-impedance path between the power supply rails of a MOSFET circuit, triggering a parasitic structure which disturbs appropriate functioning of the part, possibly even leading to its damage due to overcurrent.

The SOI process creates an oxide layer over the silicon substrate and around all device wells, eliminating the parasitic paths that can lead to latch up.

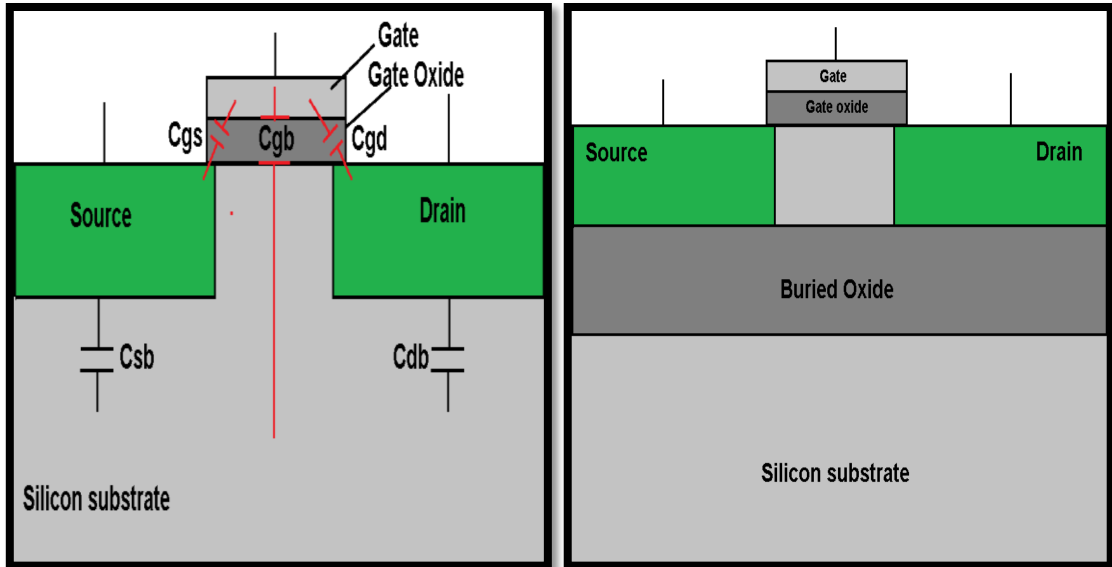

Figure 12: Cross section of Bulk and SOI MOS devices

3. <u>High density of integration</u>

This happens because we can place N+ and P+ regions next to each other, and also because the units in SOI need relatively small layout areas as compared to bulk CMOS.

4. <u>Radiation hardness</u>

The radiation in semiconductor materials will cause ionization of atoms leading to the generation of positive and negative charges. These charges lead to unwanted currents and instability in the charge distribution.

The effect of radiation is minimized due to the reduction in the exposed silicon volume. As active silicon is very thin in SOI devices, the majority of the charges generated by the radiation will exist in the lower substrate and will be blocked by buried oxide. That is why it will not affect the charges in the active layer.

5. <u>Number of process steps is reduced</u>

- **Disadvantages of SOI devices**

1. <u>Self-heating: happens in FD SOI and PD SOI devices</u>

For SOI MOSFET, the thick buried-oxide below the Si layer increases the Self-Heating Effect (SHE), which sometimes results in an undesirable output [61].

2. Power dissipation

Power consumption depends on the power dissipated in the transistor. The consumed power includes static and dynamic powers. Static power is consumption during the off state of the device. It happens because of the leakage current. Dynamic power is the consumption only during the on state and it depends on the capacitance active load (CL).

3. Kink effect: happens only in PD SOI devices

The kink effect causes nonlinearity in the device due to the sharp increase in the drain current because of the increase in body potential and associated drop in threshold voltage. This operation happens because of the high electric field near the drain due to the high drain voltage.

There are many solutions to solve the kink effect problem [38]. One way is by controlling the carrier lifetime in the floating body region with high dose silicon implantation or using SELBOX structure where the gap resistance will decrease due to the increase in the gap length. This treatment increases the drain voltage value at which the kink occurs. Therefore, for larger values of gap length the kink will disappear.

The idea behind the SELBOX MOSFET is to cover the regions below the drain, the source, and parts of the region below the channel leaving a small gap under the channel rather than covering the region below the device from the lower substrate completely. This process will allow heat to flow from the channel to the lower substrate and also minimize the increase in body potential. This will lead to reduction in the kink effect; these reductions depend on the selection of the gap width [38].

2.5 Complementary Metal–Oxide– Semiconductor (CMOS)

2.5.1 Bulk CMOS.

A Bulk CMOS has slow speed in operation due to the weak frequency characteristics as in the single device and also has very high power dissipation due to the well junction [62]. The well junction is the main source of the thermal generation current. This current is leaking from the N-substrate to the P-substrate, as shown in Figure 13, which leads to high power dissipation during the off state. In addition, there is also the drain leakage current which is leaking from the drain to the substrate of the N-channel transistor. This is why the Bulk as a CMOS has very high power dissipation compared to SOI and SELBOX.

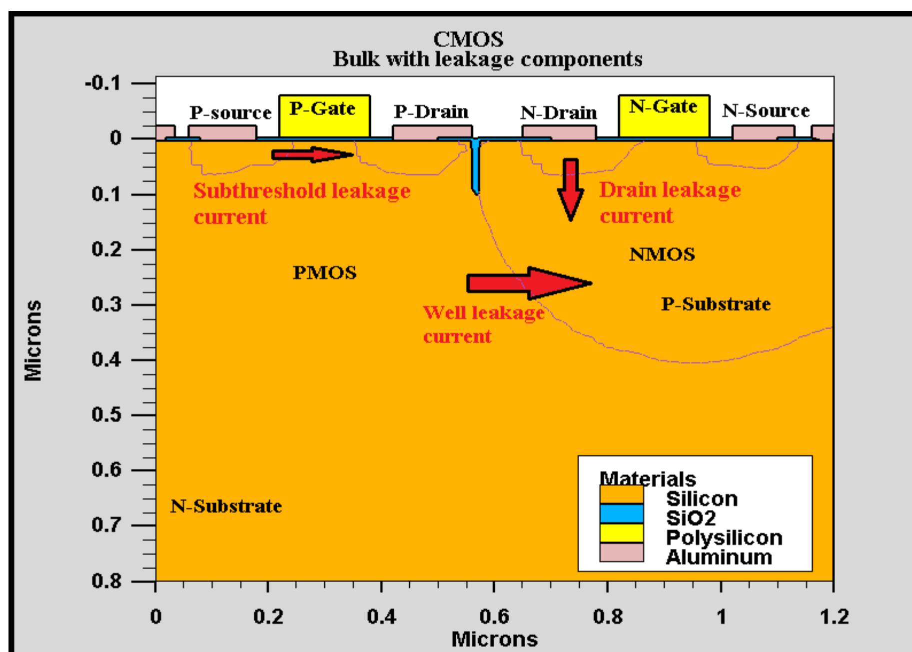

Figure 13: Cross section of Bulk CMOS inverter illustrating leakage components

2.5.2 SOI CMOS.

In SOI CMOS, the main advantage is the elimination of leakage. Leakage current in low voltage is any current that flows when the ideal current is zero. But in medium or high voltage, leakage is a current that flows either through the body or over the surface of an insulator. The SOI structure blocks the leakage between the two transistors of a CMOS by the inserted oxide layer as shown in Figure 14. SOI devices also have vertical isolation so they are isolated by dielectrics from other devices. This also eliminates leakage between CMOS transistors.

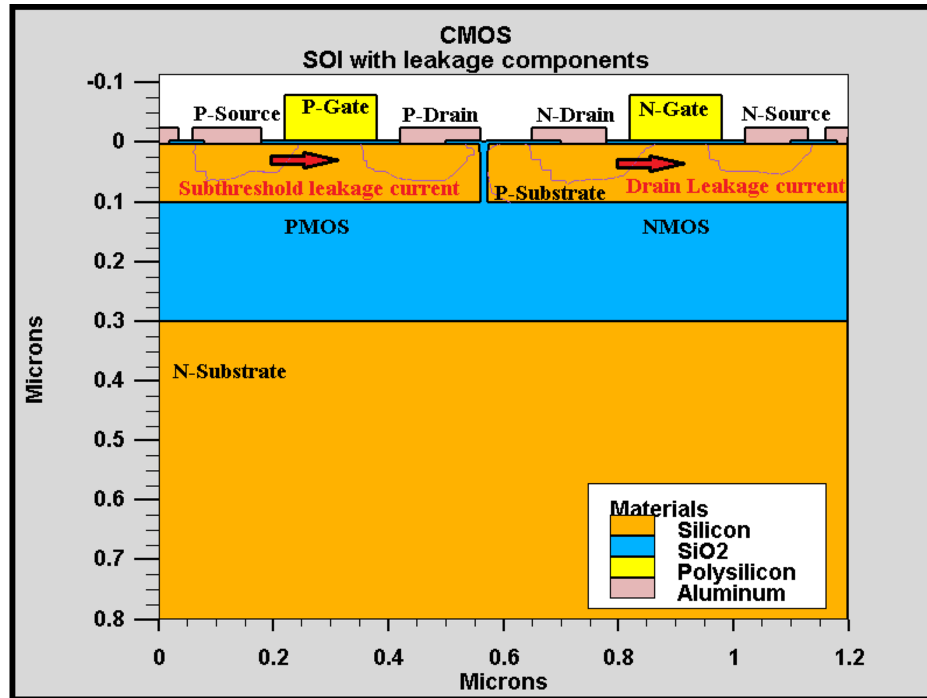

Figure 14: Cross section of SOI CMOS inverter illustrating leakage components

As a CMOS, SOI has low power dissipation with high speed in operation, but, unfortunately, it suffers again from the kink effect and self-heating. The kink effect in CMOS SOI cannot be observed clearly, but it can be noticed in the transistor as an N-channel SOI. As known, in the CMOS the drain voltage of the N-channel transistor is higher than its source. Therefore the electric field near the drain is high causing high body potential and leading to the kink effect. However, the source in the P-channel transistor is higher than the drain, so the electric field near the drain is low and that will not cause any kink effect. So when the two transistors are connected to each other, the kink effect will not be clear. Also to reduce the self-heating effect, there were some solutions tried by engineers. As a sample, there was a reduction done by using multi-layered insulator structures. Instead of using the normal SOI with SIO_2 layer alone, they tried to use $SiO_2/Si_3N_4/SiO_2$ buried insulators, and this procedure succeeded in removing the SHE [63]. However, this method needs a very long fabrication procedure to create multi layers.

To overcome these issues, we did a simulated fabrication for the SELBOX, and it succeeded in eliminating the kink effect [38], reducing the self-heating problem [41] while keeping low power dissipation and high speed in operation. This structure was

done by changing the SOI transistor to a new one with a gap under the gate. So this operation does not need long procedures and it gives acceptable results.

In this thesis, the parameters used for device simulation and the simulation results are illustrated in Chapters 4, 5, and 6.

Chapter 3: Literature Review

In this chapter, an introduction to power dissipation is presented followed by a discussion of some previous efforts on reducing power dissipation of CMOS with the advantages and disadvantages of each.

3.1 Power dissipation

Mechanisms of power dissipation are usually divided into two classes: static and dynamic. Static power dissipation becomes a problem when the circuit is in the off state or in a power-down mode. But the dynamic power dissipation mainly reflects the operational mode of a circuit; for example, the circuit is performing some operation on data [35].

CMOS is preferred for its low static power. But by decreasing the gate oxide thickness, the leakage current increases leading to more power dissipation [9].

Power dissipation in a CMOS can be categorized into three types:

1. **Leakage power dissipation** which happens due to leakage currents in the off state; we have the sub- threshold leakage, the gate-induced drain leakage, band-to-band tunneling, and gate tunneling leakage [64] [65].

The different types of leakage currents are shown in Figure 15:

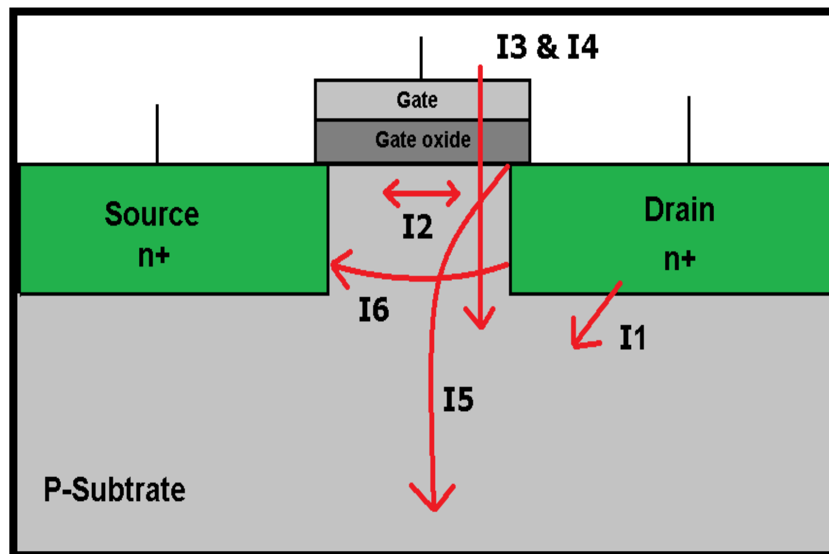

Figure 15: Leakage currents directions in Bulk MOSEFT

Where

I_1: reverse P-N junction (both ON & OFF)

I_2: sub threshold leakage (OFF)

I_3: gate leakage current (both ON & OFF)

I_4: gate current due to hot carrier injection (both ON & OFF)

I_5: gate induced drain leakage (OFF)

I_6: channel punch through current (OFF)

2. **Short-circuit power** happens in CMOSs when both transistors are on. There will be direct current flowing from V_{DD} to the ground creating a short circuit. This dissipation increases with increases in switching frequency. The short-circuit power dissipation is no longer a negligible factor, because with decreasing the size of the transistor and the threshold voltage, the short-circuit power dissipation becomes significant, especially in high performance circuits with large gates, small loads, and long transition times [66].

3. **Dynamic power or switching power** which happens due to the charging and discharging of the load capacitance [64]. The total dynamic power can be calculated through the supplied current over the entire circuit. When the output changes from logic '0' to logic '1', a small amount of current is used to charge the capacitances, while another amount is wasted through the PMOS as heat, also through the NMOS due to the short-circuit. When the output transitions from logic '1' to logic '0', the charge stored in the capacitances is discharged by the NMOS while the voltage source supplies a small amount of current due to the short-circuit [67]. The main factors influencing dynamic power dissipation are clock frequency, load capacitance, and power supply voltage.

3.2 Power reduction techniques

Several efforts have been made to reduce power dissipation, including changing the architecture of the circuit design. These efforts positively influenced behavior, but they also had significant drawbacks in increasing the cost and the density on chips.

Leakage control with efficient use of transistor stacks was proposed by Johnson et al. [4]. This control did not need substrate biasing or multiple threshold voltages and it contains the advantage of stacks of MOSFET [5]. In this journal article, authors described the circuit design methodology. They determined an input vector that kept most of the circuit operating at low leakage. This state happens when most of the transistors are turned off in each leakage path. Then, they determined where leakage control could be inserted to have as low leakage current as possible. The authors proved that for low-threshold voltage and low-supply voltage, the use of a minimum leakage vector (MLV); with stacking transistor is a great method for leakage control.

The stack effect method was introduced by Saxena and Soni [6]. As mentioned previously; the subthreshold current depends exponentially on the threshold voltage, drain-source voltage, and gate-source voltage. This means that the terminal voltages have to be controlled in order to control the subthreshold current. The main idea is to increase the source voltage so that they can get lower gate-source voltage which reduces the subthreshold current exponentially. The leakage of transistors in a stack is a function of the input pattern and number of transistors, where the source voltage can be increased by forcing series transistors to be simultaneously off, or using reverse body biasing to increase threshold voltages. Another outcome of raising the source is that it also reduces the body-source voltage, resulting in a higher threshold voltage due to the body effect. However, the stack effect only gives narrow reduction over leakage currents, and body biasing effectiveness reduces with technology scaling.

Several dual-threshold voltage techniques for reducing standby power dissipation were presented by Kao and Chandrakasan [7]. During active mode, the threshold voltages of the transistors stay with no changes. However, during standby mode, the threshold voltages of the transistors are increased so the leakage current is reduced. The multi-threshold CMOS technique is used for static logic design, and the dual-threshold domino logic technique is used for dynamic logic solutions. The dual threshold voltage transistor stacking technique was presented by Udaiyakumar and Sankaranarayanan [8]. This technique takes into consideration the advantages of sleep transistor and stack effect techniques. Sleep transistors are designed with stack effect. The new sleep transistor has high threshold voltage with reduced size.

A switched-source-impedance (SSI) CMOS circuit was proposed by Horiguchi et al. [9] as a way to reduce the exponential increase of the leakage current with changing the threshold voltage. Adding switched impedance at the source of a MOSFET will reduce the standby power dissipation due to reduction in subthreshold current. The reduction will be around three to four orders of magnitude if the operation were done at room temperature. This system is valid for any combinational and sequential CMOS logic circuit as long as the voltages are easy to predict.

The sleep approach for logic circuits was proposed by Kim and Mooney [10], Mutoh et al. [11], and Powell et al. [12]. In this technique, an additional "sleep" PMOS transistor is located between the supply and the pull-up network of a circuit and an additional "sleep" NMOS transistor is located between the pull-down network and the ground. These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is in the active mode and turned off when the circuit is in the sleep mode. By cutting off the power source, this method can reduce power dissipation effectively. However, the output voltage will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage.

In, the effect of inserting an extra transistor into the large leakage path in logic circuits was proposed by lin et al. [13]. This structure induces low leakage current under all possible inputs with good performance. However, the number of transistors will increase. In the same period of time, Abdollahi et al. [14] published an article which proposed applying a minimum leakage vector (MLV) control to a circuit. The leakage reduction can be done only when the circuit is in standby mode. The applying MLV for leakage reduction does not depend on the source of leakage, which can be gate tunneling leakage or subthreshold current. However, the circuits of large logic depth are less effective due to the small impact of this technique at high logic levels [15].

In, the static power reduction technique known as GALEOR (gated leakage transistor) was illustrated by Katrue and Kudithipudi [16]. It reduces the leakage current flowing through the circuits. Two gated leakage transistors with high threshold voltages are inserted between NMOS and PMOS with low threshold voltage circuitry of the existing circuit. The gates of the inserted transistors are connected to

their respective drain regions. This technique reduces the area by eliminating the use of control logic to switch between the active and the standby states. However, the area is not minimized perfectly because of using extra transistors--two transistors for each CMOS.

A technique to reduce power dissipation using low supply voltage was presented by Gonzalez et al. [17], and Chandrakasan et al. [18]. This technique involves choosing an accepted low voltage as a supply for MOSFET. According to the gate voltage, the threshold voltage will decrease and, similarly, the power dissipation will also decrease. It is conjugated to logic style, architectural, technology and circuit optimizations. This technique is not sufficient for switching operations because when the voltage supply goes under a certain range, the procedure will not give the desired results [19]. This technique has many limitations such as the following: the electric field between different junctions must be below a certain level to avoid short channel effect; also the electric field across the gate oxide has to be limited to maintain high carrier mobility in the channel area. If one of the parameters exceeds its limit, the gate leakage current will increase static power dissipation [20] [21].

Resizing the gate method was proposed by Girard et al. [22] [23], which can decrease power dissipation. The main idea was to replace some gates of the circuit with devices having smaller area which have smaller gate capacitance with less power dissipation. Experimental results on some circuits have shown that power dissipation is reduced by 27.9% compared to circuits without resizing, which will cut off only 4.2% of the total power dissipation.

Mohanty et al. [24] proposed a technique that require an increase in the gate oxide thickness to decrease tunneling current, which is the dominant component of leakage current. As a result, static power dissipation will be reduced. In addition, this way will increase the propagation delay. According to the International Technological Roadmap for Semiconductors (ITRS) [25], in 2006, oxide thickness (T_{ox}) values of 7–12˚A were required for high performance CMOS circuits. Changing T_{ox} can make a big change in leakage current. For example, in an MOS device with SIO_2 gate oxide, a small decrease in $T_{ox,}$ like 2^oA, can increase gate leakage current 1000 times [26]. But subthreshold leakage current decreases with oxide thickness [27].

A design for logic circuits was introduced by R. Lorenzo and S. Chaudhary [28] to reduce power dissipation. The design employs dynamic voltage scaling to reduce leakage power and recalls the data during the no action mode. The main idea behind this technique is that it uses two leakage control transistors with different ground levels. When the output voltage is equal to the source voltage (which means the pull-up network is ON and the pull-down network is OFF), there is a leakage current flow in the pull-up network. The output voltage turns off the PMOS and turns on the NMOS transistor and supplies positive ground level voltage (Vs) to the pull-down network, thus cutting the subthreshold leakage path from source voltage to ground. Subthreshold leakage current is reduced because of the increase in threshold voltage due to the body effect; this also increases source voltage. The reduction of leakage current is due to the reduction of drain and consequently the reduction in the drain-induced barrier lowering effect. On the other hand, if the output voltage is low, then the NMOS transistor turns off and the PMOS transistor turns on, providing ground voltage to the pull-down network. So here, leakage is due to only the pull-up network and the remaining circuit works the same as the gate bias circuit.

A design of a Fully Depleted SOI for low power dissipation was introduced by Mendez [29]. In this paper the author addressed technology attributes, cost, and manufacturability considerations. The author's aim was to get low power dissipation with high performance and low cost. Unfortunately, the kink effect was the disadvantage in that device. Hence, we believe that if the kink effect is reduced, we may be able to produce an SOI MOSFET with low power dissipation.

A study of a Double Gate MOSFET was presented by Ruchika et al. [30]. The objective was to improve the performance of the MOSFET and to reduce power consumption by studying the MOSFETs with double gates. The design was done by connecting two Single Gate MOSFET transistors in parallel in such a way that their source and drain were connected together [31]. This design functioned properly and operated efficiently in subthreshold regions to achieve low power. However, this design required a double space on a chip which is not suitable for modern designs.

A new SOI transistor with an auxiliary MOSFET was proposed by Lee et al. [32]. The gate and drain were connected to the gate of the basic transistor and the source

connected to the channel body of the basic transistor. This new transistor applied a good bias to the channel body of the basic transistor. The dynamic threshold-voltage SOI transistor was introduced by Assaderaghi et al. [33]. In this transistor, the threshold voltage depended on the gate voltage of the device; as the gate voltage increased the threshold voltage decreased, resulting in very high current compared with the standard MOSFET for low-power supply voltages. On the other hand, the threshold voltage was high at zero input voltage; therefore the leakage current was low.

In summary it can be stated that many efforts were done to minimize power dissipation. Unfortunately, these studies concentrated on the power issue without taking into consideration the density on chips or the cost. The approach in this thesis takes another viewpoint: changing the fabrication process of the SOI transistor itself to get a new transistor called a Selective Buried Oxide (SELBOX) MOSFET. This new structure will combine the Bulk's and SOI's advantages and eliminate the drawbacks of each, saving money and reducing chip density.

Chapter 4: Simulation of Device Fabrication

One of the main objectives of the present work is to explore the fabrication of a MOSFET with low power dissipation. Fabricating a SOI MOSFET was essentially suggested to achieve low power dissipation [36]. Then a Fully Depleted SOI was produced to operate at very low power with high performance and with low overall cost [29]. But this solution suffered from the kink effect. In this research work, we propose the fabrication of the SELBOX MOSFET structure to reduce power consumption more than the SOI with the advantages of the Bulk I-V characteristics of having no kink effect. To compare the performance of SELBOX architecture with the other devices, we simulated the fabrication of Bulk, SOI, and SELBOX for both NMOS and PMOS transistors. This is followed by combining the N type with the P type MOSFETs to simulate a CMOS.

Following the simulation of various devices, the current–voltage characteristics were determined followed by estimating the static power dissipation of the Bulk, SOI, and SELBOX for NMOS and PMOS devices. This was then followed by investigating the static power dissipation of the CMOS structure.

4.1 Device dimensions

The simulated devices have different dimensions according to the threshold voltage. To be able to combine NMOS with PMOS, the absolute threshold voltages have to be similar (around 0.6V). For all devices in this thesis, the total height of the device was 0.8 µm, the total width 1.2 µm, and the depth equals to the channel length – 0.4 µm for single devices and 0.09 µm for CMOS as shown in Figure 16.

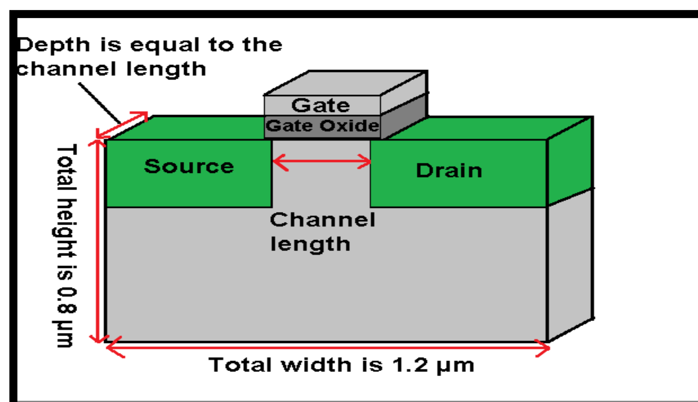

Figure 16: Bulk structure with illustrated dimensions

4.1.1 Single device.

The fabrication of Bulk MOSFET was simulated using the dimensions chosen from previous literature to be able to compare our results with other published studies [38].

The simulated fabrication of Bulk devices was carried out for both PMOS and NMOS using the dimensions shown in Table 2. The PMOS Bulk had dimensions slightly different from the NMOS to reach the same absolute threshold voltage.

Table 2: Bulk's dimensions as single device

Dimensions	NMOS	PMOS
Channel length	0.4 µm	0.4 µm
Average gate oxidation thickness	15 nm	7 nm
Doping depth	0.173 µm	0.138 µm

The SOI devices were simulated for both PMOS and NMOS using the dimensions listed in Table 3.

Table 3: SOI's dimensions as single device

Dimensions	NMOS	PMOS
Active layer	0.18 µm	0.18 µm
Channel length	0.4 µm	0.4 µm
Average gate oxidation thickness	9 nm	3 nm
Doping depth	0.18 µm	0.14 µm
Isolation thickness	0.2 µm	0.2 µm

Then, SELBOX devices for PMOS and NMOS were simulated using the dimensions in Table 4.

Table 4: SELBOX's dimensions as single device

Dimensions	NMOS	PMOS
Channel length	0.4 µm	0.4 µm
Average gate oxidation thickness	10.7 nm	7.5 nm
Doping depth	0.18 µm	0.14 µm
Isolation thickness	0.2 µm	0.2 µm
Gap width	0.04 µm	0.04 µm

As shown in Table 4, the dimensions between NMOS and PMOS have clear differences because, as mentioned before, the priority is for the absolute threshold voltage to be the same for both devices.

4.1.2 CMOS devices.

After conducting all the simulations for the suggested transistors as single devices, we simulated the fabrication of the CMOS structure for all three different devices but with technology of 90 nm to compare them with state of the art transistors.

The simulated fabrication of CMOS Bulk was carried out using the dimensions shown in Table 5.

Table 5: CMOS Bulk dimensions

Dimensions	NMOS	PMOS
Channel length	90 nm	90 nm
Average oxidation thickness	6.3 nm	6.3 nm
Average doping depth	50 nm	50 nm
Isolation length in between	100 nm	

After that, the simulated fabrication of CMOS SOI device was done using the dimensions in Table 6.

Table 6: CMOS SOI dimensions

Dimensions	NMOS	PMOS
Channel length	90 nm	90 nm
Average oxidation thickness	6.3 nm	6.3 nm
Average doping depth	50 nm	50 nm
Isolation length in between	100 nm	
Isolation width	0.2 µm	

Then, the CMOS SELBOX was simulated using the same dimensions as the CMOS SOI but with two added gaps in the isolation layer with the dimensions in Table 7.

Table 7: CMOS SELBOX dimensions

Dimensions	NMOS	PMOS
Channel length	90 nm	90 nm
Average oxidation thickness	6.3 nm	6.3 nm
Average doping depth	50 nm	50 nm
Isolation length in between	100 nm	
Isolation width	0.2 µm	
Gap length	9 nm	9 nm

4.2 Device parameters

In this thesis, three important device parameters were considered: threshold voltage, mobility, and oxide capacitance. They were calculated using estimated parameters from simulated single devices. Table 8 shows the device parameters used in simulating the devices.

Table 8: Device parameters

Parameters	Values	Units
Doping concentration of poly silicon ($N_{(poly\ silicon)}$)	2.26E20	cm^{-3}
Doping concentration of substrate (N_S)	1.0E17	cm^{-3}
Intrinsic doping concentration (n_i)	1.02E10	cm^{-3}
Boltzmann's constant (K)	1.38E-23	J/K
Room temperature (T)	300	K
Charge density (q)	1.6E-19	coulomb
Permittivity of oxide (ε_{ox})	34.515E-12	F/m
Permittivity of silicon (ε_S)	103.545E-12	F/m
Electron affinity of the semiconductor (X_S)	4.05	V
Bulk potential (Φ_M)	4.05	V
Oxide thickness (t_{ox})	15	nm

4.3 Calculation of threshold voltage for Bulk NMOS

For the Bulk NMOS, the threshold voltage was calculated using the equations described in Chapter 2; (1), (2), (3), (4), (5)

To calculate the threshold voltage, the following steps were followed:

$$\mathrm{V}_t = \frac{KT}{q}$$

$$= \frac{1.38\mathrm{E}-23 * 300}{1.6\mathrm{E}-19} = 0.026\,V$$

$$\Phi_f = \mathrm{V}_t \ln \frac{N_S}{n_i}$$

$$= 0.026 \ \ln \frac{1 * \mathrm{E17}}{1.02\mathrm{E10}} = 0.419\,V$$

The oxidation capacitance had to be calculated to be used in the threshold voltage equation:

$$\mathrm{C}_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$= \frac{3.9 * 8.85\text{E} - 12}{15\text{E} - 9} = 0.0023\ F/m^2$$

$$\Phi_{ms} = \Phi_m - \left(X_s + \frac{E_g}{2q} + \Phi_f \right)$$

$$= 4.05 - \left(4.05 + \frac{1.12}{2} + 0.419 \right) = -0.979\ V$$

$$V_{TH} = \Phi_{ms} + 2\ \Phi_f + \frac{\sqrt{2qN_S * 2\left|\Phi_f\right|\varepsilon_s}}{\text{C}_{ox}} =$$

$$-0.979 + 2 * 0.419 + \frac{\sqrt{2*1.6\text{E}-19*1*\text{E}23*2*0.419*11.7*8.85\text{E}-12}}{0.0023} = 0.58\ V$$

4.4 Calculation of mobility for N- channel and P-channel MOSFETs

N-channel MOSFETs have some inherent performance advantages over P-channel MOSFETs. The mobility of electrons, which are carriers in the case of an N-channel device, is about two times greater than that of holes, which are the carriers in the P-channel device.

The mobility equation can be given by [68]:

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1+(\frac{N}{N_{ref}})\alpha}\ \text{cm}^2/\text{V.s} \qquad (7)$$

By using the constant parameters in Table 9, we can get:

Table 9: Parameters for calculation of the mobility as a function of the doping density [68]

Constants	Phosphorus	Boron	Units
μ_{min}	68.5	44.9	$\frac{cm^2}{V.s}$
μ_{max}	1414	470.5	$\frac{cm^2}{V.s}$
N_{ref}	9.2E16	2.23E17	cm^{-3}
α	0.711	0.719	Null

$$\mu_n = 68.5 + \frac{1414 - 68.5}{1 + \left(\frac{1 * \mathrm{E}17}{9.2\mathrm{E}16}\right) * 0.711} = 758.957\ \mathrm{cm}^2/\mathrm{V.s}$$

$$\mu_p = 44.9 + \frac{470.5 - 44.9}{1 + \left(\frac{1 * \mathrm{E}17}{2.23\mathrm{E}17}\right) * 0.719} = 321.833\frac{\mathrm{cm}^2}{\mathrm{V}}.\mathrm{s}$$

The N-channel mobility is twice that of the P-channel; this will affect the resistivity of the MOSFET. Thus an N-channel device is faster than a P-channel device. However, PMOS circuits have advantages such as being easy to control, and having low cost processing, good yield and high noise immunity.

Since electron mobility is twice that of hole mobility, an N-channel device will have one-half the on-resistance of an equivalent P-channel device with the same geometry and under the same operating conditions. Thus N-channel transistors need only half the size of P-channel devices to achieve the same impedance. Therefore, N-channel ICs can be smaller for the same complexity or, even more importantly, they can be more complex with no increase in silicon area.

NMOS circuits offer a speed advantage over PMOS due to having smaller junction areas. Since the operating speed of a MOS IC is largely limited by internal RC time constants, and capacitance of a diode is directly proportional to its size, an N-channel junction can have smaller capacitance. This, in turn, improves its speed.

The next two chapters will show the results of the simulation for the three devices as single and as CMOS with illustrations.

Chapter 5: Power Dissipation of Single Devices

In this chapter, the steps of single device processing are presented. The simulation results obtained are then discussed and compared. Simulations were performed in different steps using the Silvaco software, starting from the Bulk MOSFET to the SELBOX MOSFET. The procedure can be summarized as follows:

1. Simulate the fabrication of the three devices: Bulk, SOI, and SELBOX for NMOS and PMOS
2. Obtain the I-V characteristics for all devices:
    - Drain current versus gate voltage.
    - Drain current versus drain voltage in the ON state.
    - Leakage current versus drain voltage.
3. Compare the static power dissipation of the three devices.

In simulation, the devices were fabricated in such a way to reduce power dissipation by controlling the doping level for each, the channel length, the oxidation thickness, and the gap length of SELBOX.

The structures were simulated and tested under specific absolute threshold voltage around 0.6 V for Bulk, SOI and SELBOX. In this chapter we intend to demonstrate the advantages of SELBOX as a single device over the other two devices in terms of low power dissipation, no kink effect and high operation speed.

The technology used in this test was 0.4µm in order to compare with the results published in the literature [38]. In the next chapter, 90 nm technology was used to simulate CMOS devices.

5.1 N-channel MOSFET

In the beginning, N-channel single devices were fabricated and tested through simulation with different dimensions according to the needed threshold voltage. The structure of the Bulk MOSFET is shown in Figure 17 with illustrated dimensions. The drain current versus the gate voltage for the N-channel Bulk MOSFET at drain voltage equals 1V as shown in Figure 18.

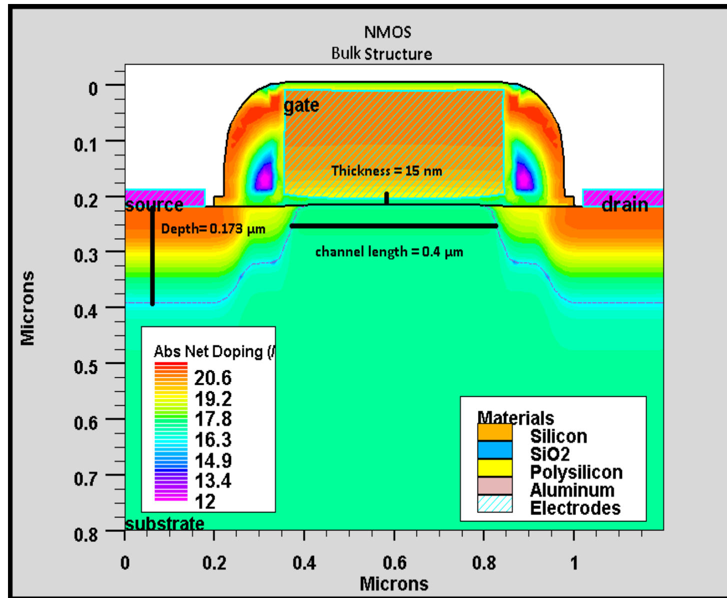

Figure 17: N-channel Bulk structure

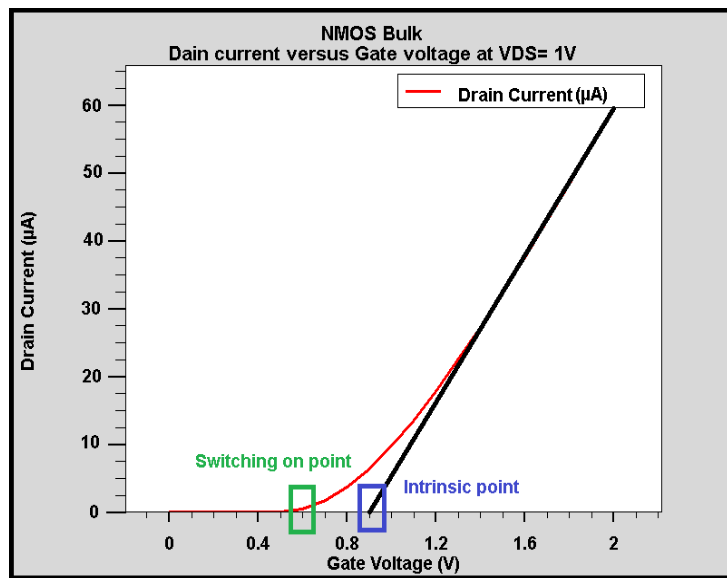

Figure 18: Drain current versus gate voltage for N-channel Bulk MOSFET at VDS=1V

The threshold voltage can be obtained through different ways [68] [69]. Theoretically, threshold voltage can be defined as the minimum required gate voltage to switch the transistor on. By this definition, we can say that threshold voltage is 0.6 as shown in Figure 18. On the other hand, the threshold voltage can be defined practically from the graph by the intrinsic point between the gate voltage axis and the tangent line of the curve. By using this definition, we can say that the threshold

voltage is 0.9 V as shown in Figure 18. In this thesis, we will consider the intrinsic point which is 0.9 V for comparison between the devices.

Drain current versus drain voltage for different gate voltages is shown in Figure 19. The power dissipation at the off state is due to the leakage current, so the device was tested at VGS = 0.4 (less than threshold voltage) and the leakage current–drain voltage curve is shown in Figure 20.

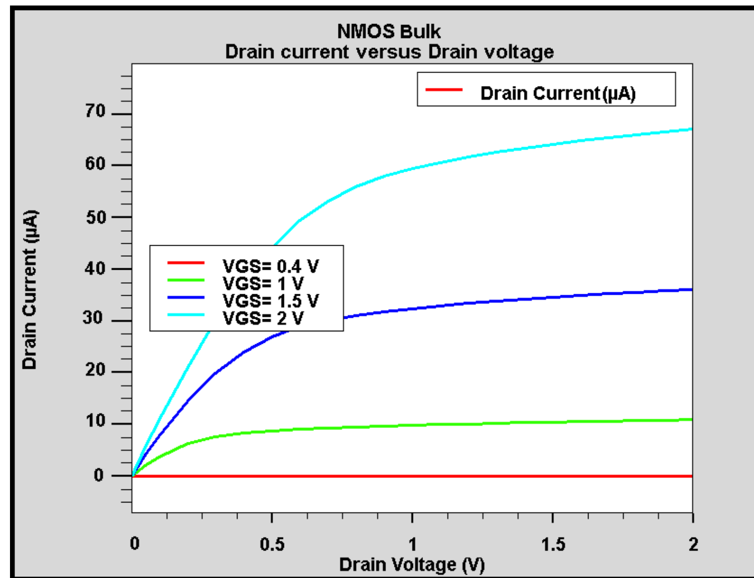

Figure 19: Drain current versus drain voltage for N-channel Bulk MOSFET

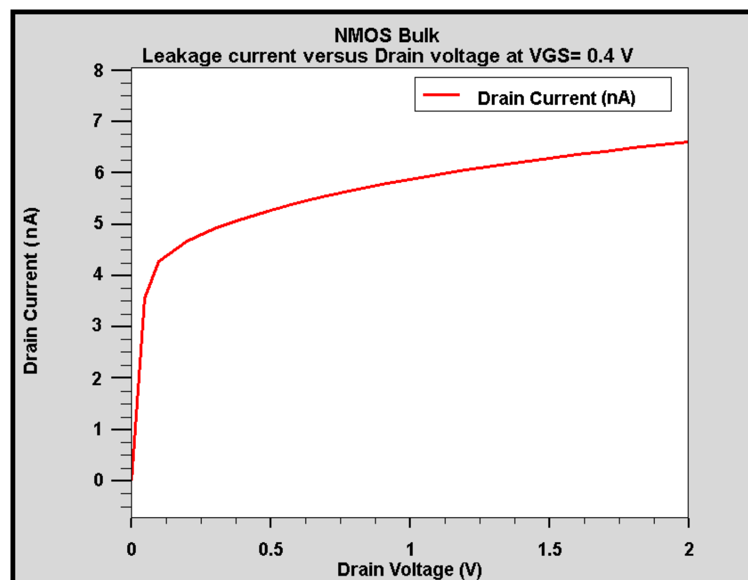

Figure 20: Leakage current versus drain voltage for N-channel Bulk MOSFET at VGS=0.4V

To reduce power dissipation, a SOI MOSFET was simulated. The structure of the SOI MOSFET is shown in Figure 21 with illustrated dimensions. We tried to have the same dimensions for the three devices, but the priority was for threshold voltage so we produced dimensions close to each other but not exactly the same.

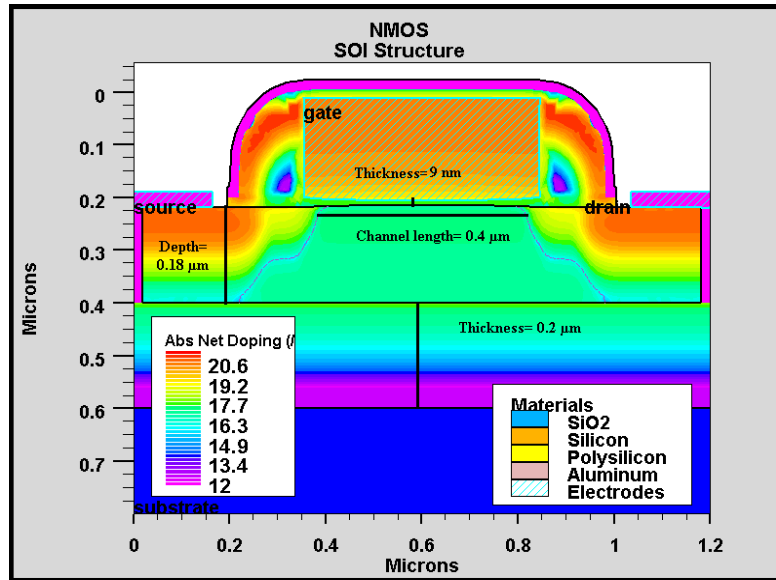

Figure 21: SOI structure

Drain current versus gate voltage for the N-channel SOI at a drain voltage equal to 1V is shown in Figure 22.

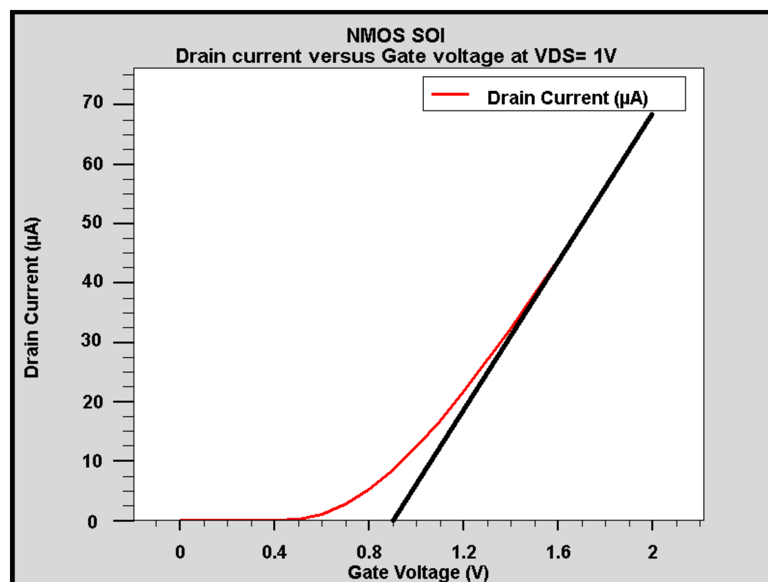

Figure 22: Drain current versus gate voltage for N-channel SOI MOSFET at VDS=1V

Drain current versus drain voltage for the N-channel SOI MOSFET at different gate voltages is shown in Figure 23.

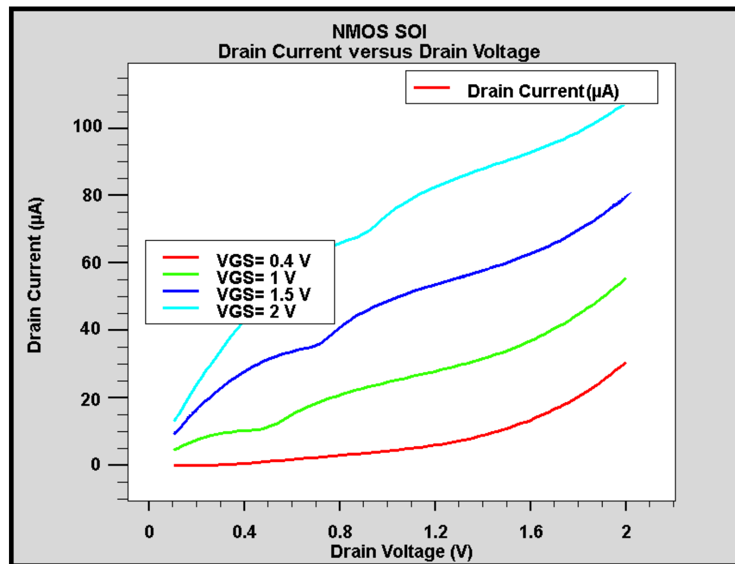

Figure 23: Drain current versus drain voltage for N-channel SOI MOSFET

Figure 23 clearly shows the kink effect. Power dissipation in the SOI is more than the Bulk since we get more DC current at the same V_{DS} as compared to the other two devices. This is due to kink and body voltage variations in the device. Hence the steady state power dissipation in the individual SOI appears to be high.

Leakage current versus drain voltage curve at small gate voltage is shown in Figure 24.

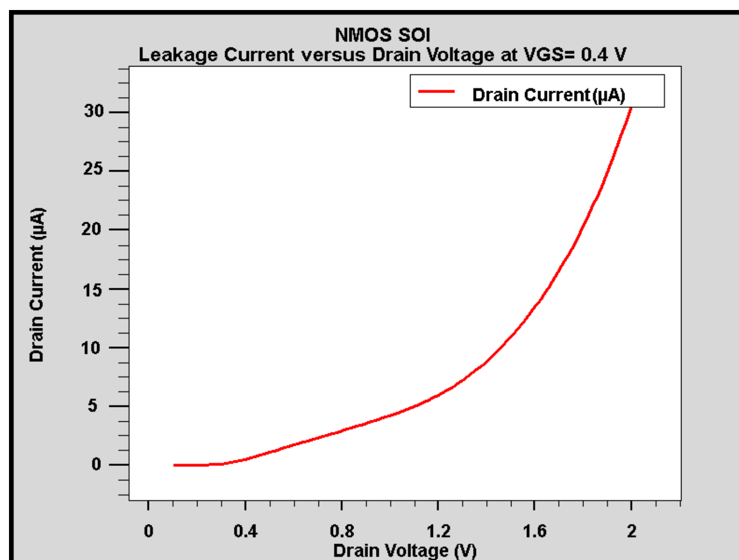

Figure 24: Leakage current versus drain voltage for N-channel SOI MOSFET at VGS=0.4V

As a comparison between Bulk and SOI, leakage current of the Bulk is approximately 6.75 nA at V_{DS} equal to 2 V as shown in Figure 20. But leakage current of the SOI is approximately 30 µA at V_{DS} equal to 2 V as shown in Figure 24. This is a huge difference between Bulk and SOI. So the SELBOX MOSFET is built to have the advantage of reduced power dissipation without the kink effect.

The structure of the SELBOX MOSFET is shown in Figure 25 with illustrated dimensions.

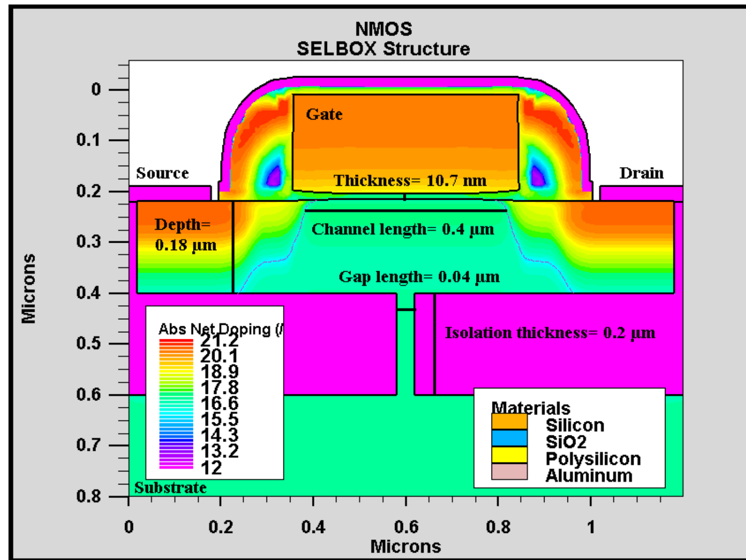

Figure 25: N- channel SELBOX structure

Drain current versus gate voltage for an N-channel SELBOX at drain voltage equal to 1V is shown in Figure 26.

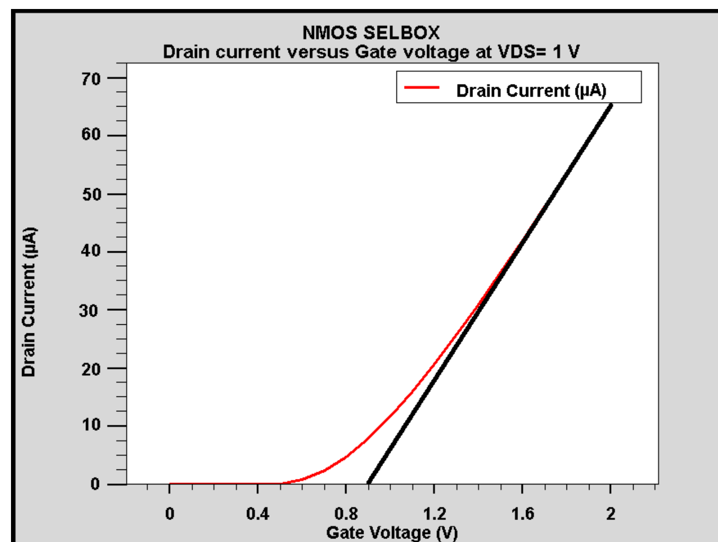

Figure 26: Drain current versus gate voltage for N-channel SELBOX MOSFET at VDS=1V

Drain current versus drain voltage for an N-channel SELBOX MOSFET at different gate voltages is shown in Figure 27. As shown, the kink affect disappeared in this structure and maximum current is reduced compared with SOI device.

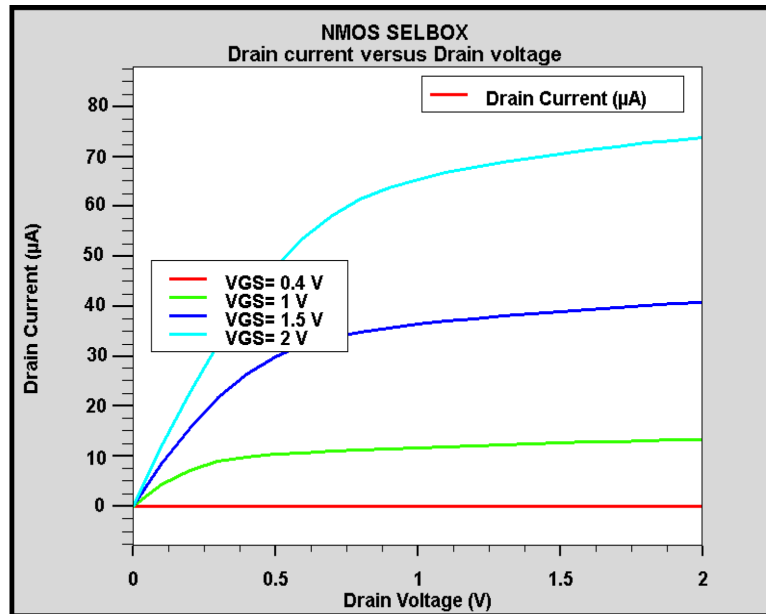

Figure 27: Drain current versus drain voltage for N-channel SELBOX MOSFET

Leakage current versus drain voltage curve at small gate voltage for the N-channel SELBOX is shown in Figure 28.

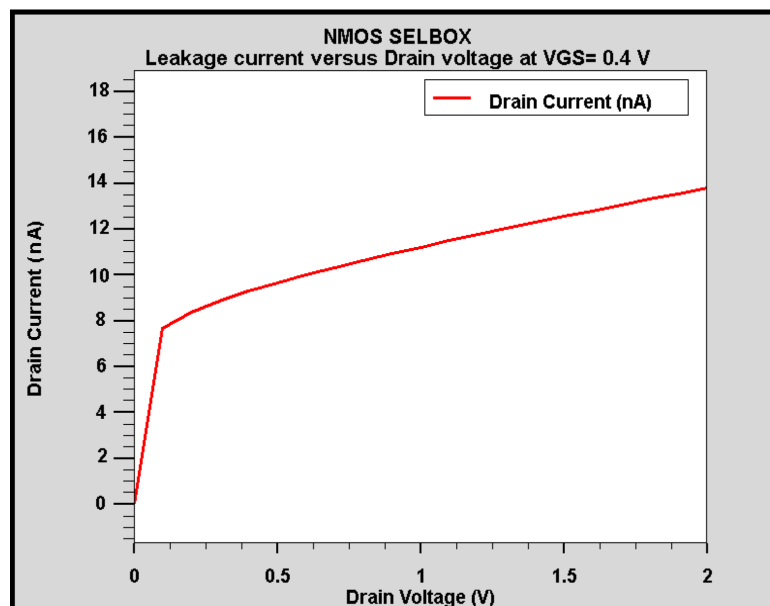

Figure 28: Leakage current versus drain voltage for N-channel SELBOX MOSFET at VGS=0.4V

5.2 P-channel MOSFET

In this section, P-channel single devices were fabricated and tested through simulation with the same threshold voltage of the N-channel devices.

The simulated Bulk MOSFET structure with illustrated dimensions is shown in Figure 29.

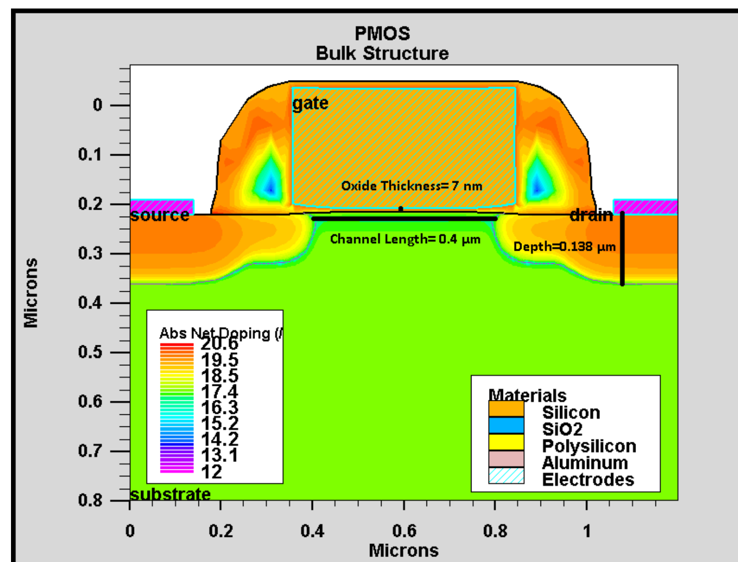

Figure 29: P-channel Bulk structure

Figure 30 shows absolute drain current versus absolute gate voltage for a P-channel Bulk MOSFET at drain voltage equal to (-1V).

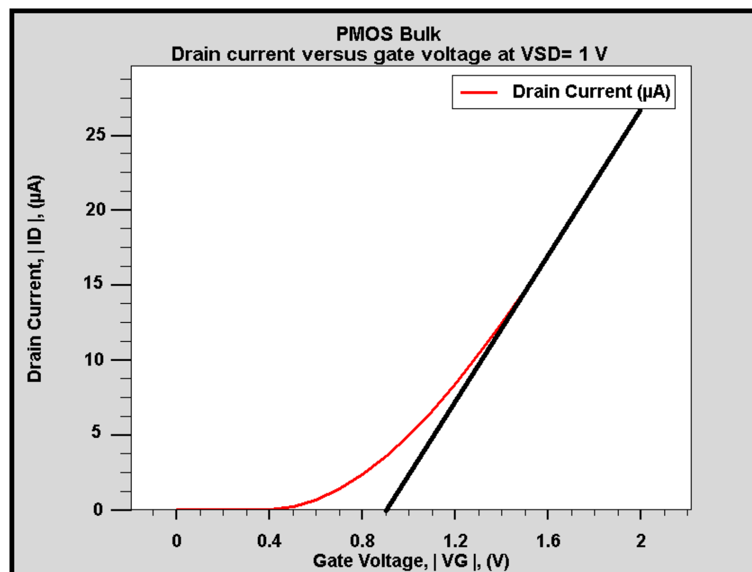

Figure 30: Drain current versus gate voltage for P-channel Bulk MOSFET at VSD=1V

As shown in Figure 30, the absolute value of the threshold voltage is close to 0.9V. That will help us compare between the devices.

Figure 31 shows absolute drain current versus absolute drain voltage for a P-channel Bulk MOSFET at different gate voltages.

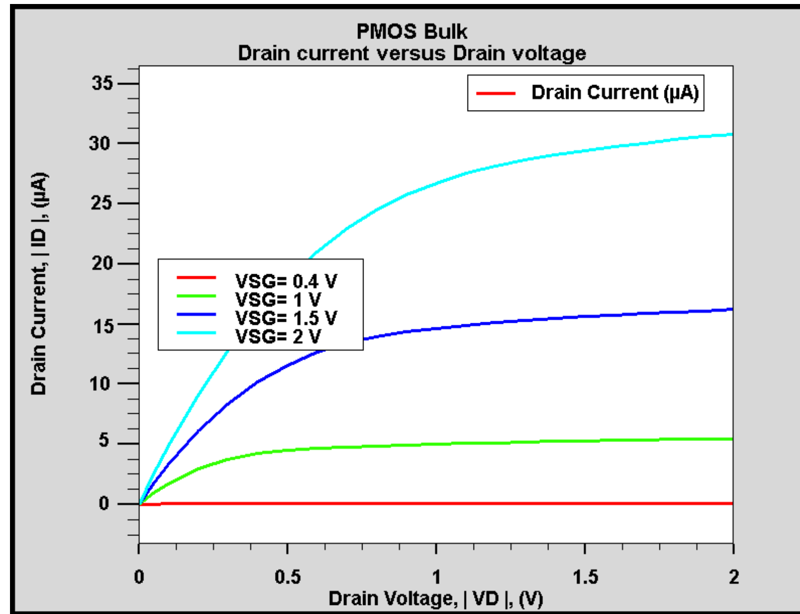

Figure 31: Drain current versus drain voltage for P-channel Bulk MOSFET.

The absolute leakage current versus absolute drain voltage curve at small gate voltage for P-channel Bulk is shown in Figure 32.

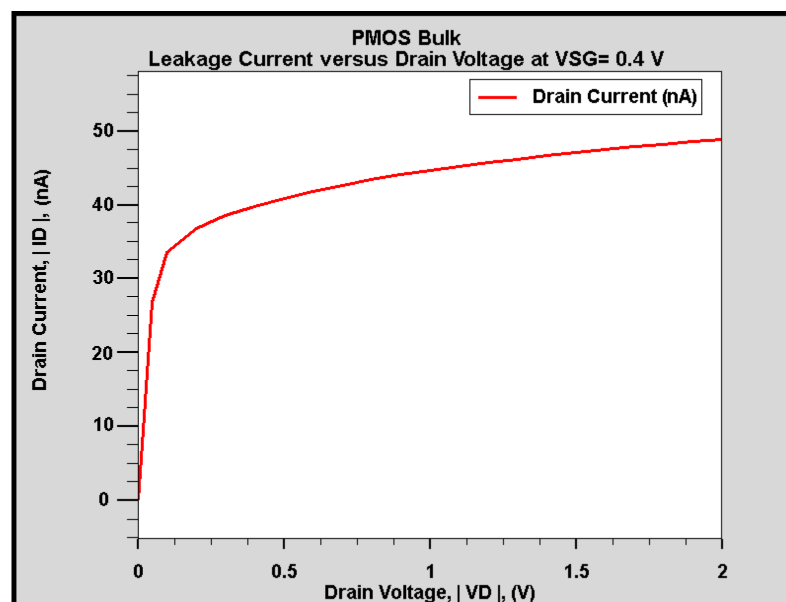

Figure 32: Leakage current versus drain voltage for P-channel Bulk MOSFET at VSG= 0.4V

The simulated SOI PMOS structure with illustrated dimensions is shown in Figure 33.

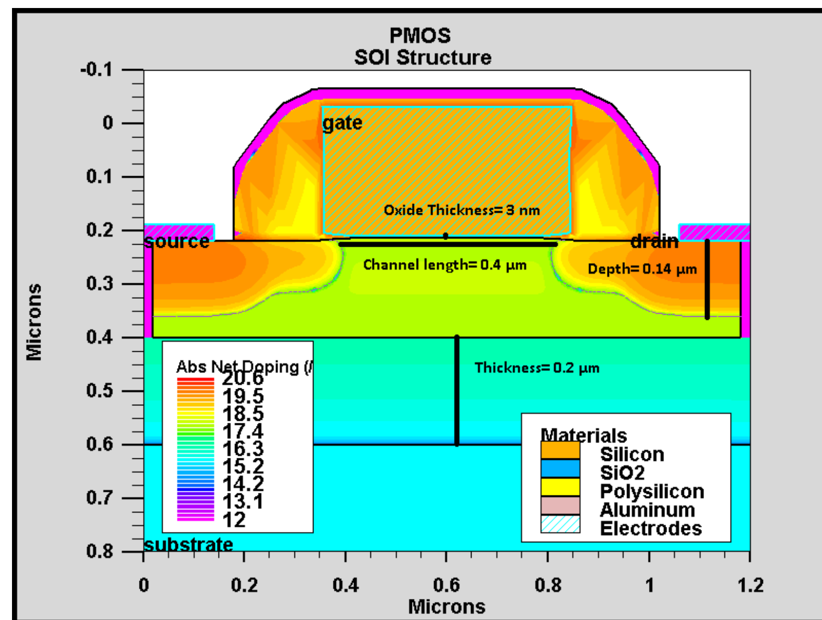

Figure 33: PMOS SOI structure

Figure 34 shows absolute drain current versus absolute gate voltage for a P-channel SOI MOSFET at drain voltage equal to (-1V).

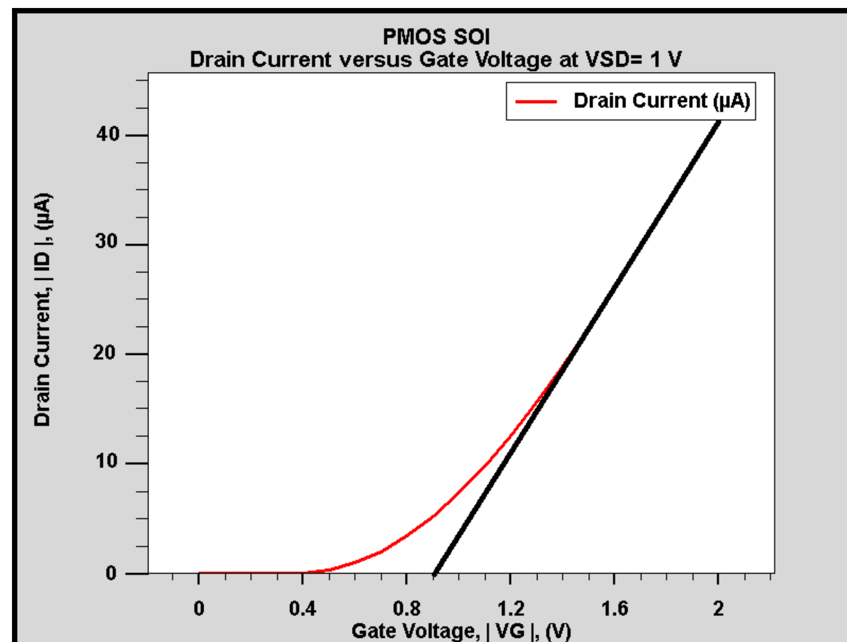

Figure 34: Drain current versus gate voltage for P-channel SOI MOSFET at VSD=1V

Figure 35 shows absolute drain current versus absolute drain voltage for a P-channel SOI MOSFET at different gate voltages.

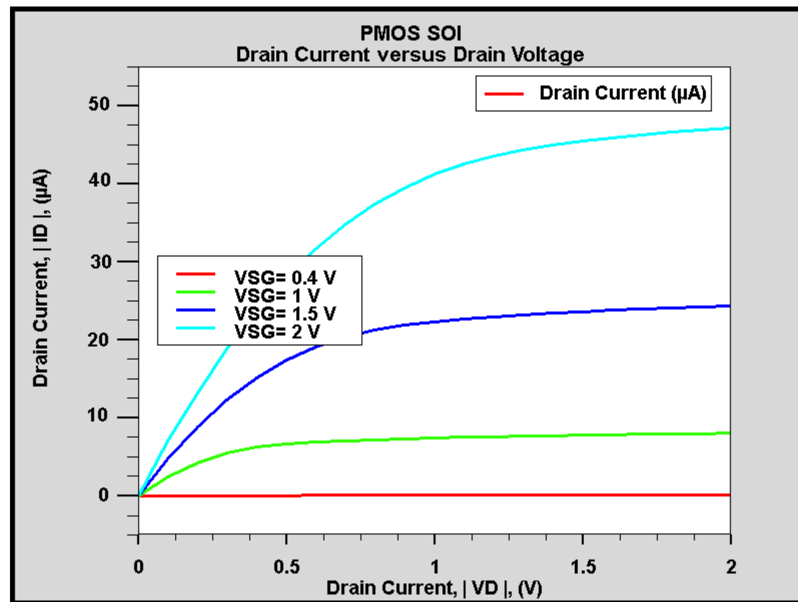

Figure 35: Drain current versus drain voltage for P-channel SOI MOSFET

As we can see in Figure 35, there is no kink effect because the kink affect appears just in the N-channel SOI devices, but the current still high.

The absolute leakage current versus absolute drain voltage curve at small gate voltage for the P-channel SOI is shown in Figure 36.

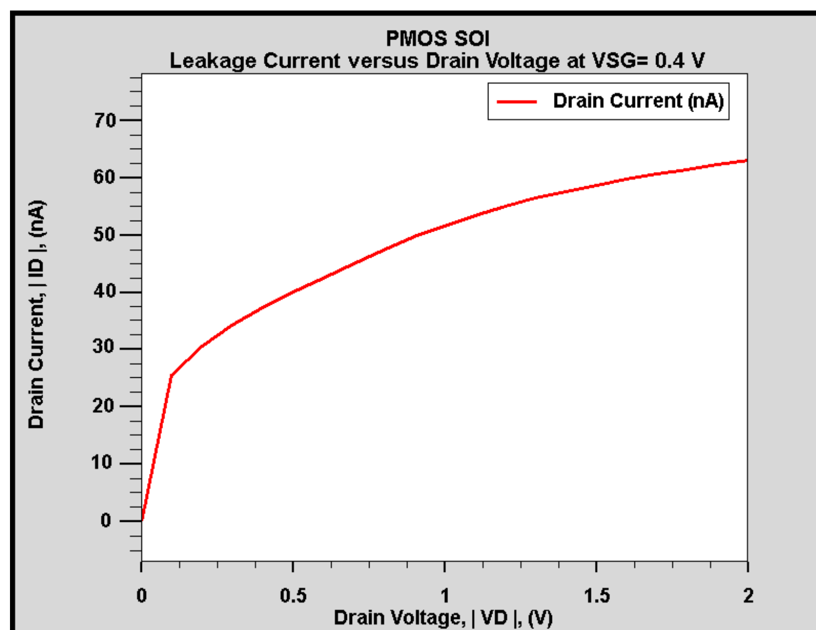

Figure 36: Leakage current versus drain voltage for P-channel SOI MOSFET at VSG=0.4V

This absolute leakage current curve for the P-channel MOSFET is due to body potential changes. As mentioned before, there is no kink effect, which is why the curve takes a different shape than the N-channel MOSFET I-V curve.

The simulated SELBOX MOSFET structure with illustrated dimensions is shown in Figure 37.

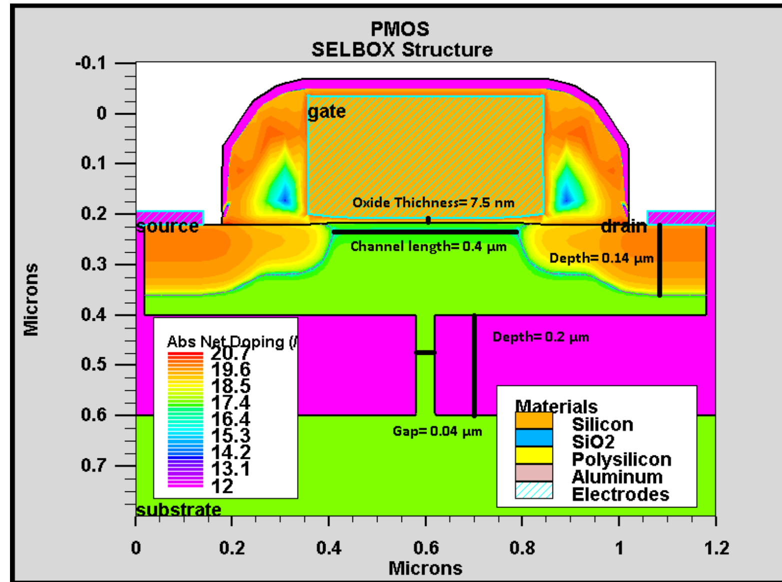

Figure 37: PMOS SELBOX structure

Figure 38 shows absolute drain current versus absolute gate voltage for a P-channel SELBOX MOSFET at drain voltage equal to (-1V).

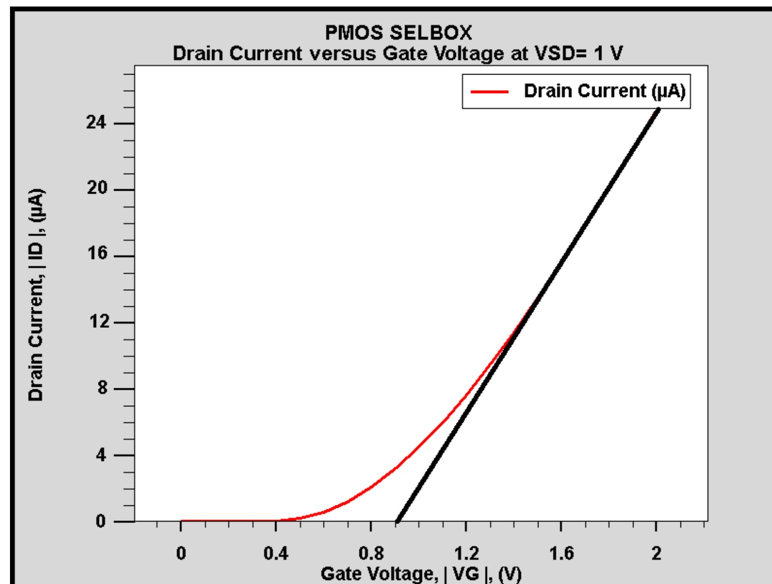

Figure 38: Drain current versus gate voltage for P-channel SELBOX MOSFET at VSD=1V

Figure 39 shows absolute drain current versus absolute drain voltage for a P-channel SELBOX MOSFET at different gate voltages.

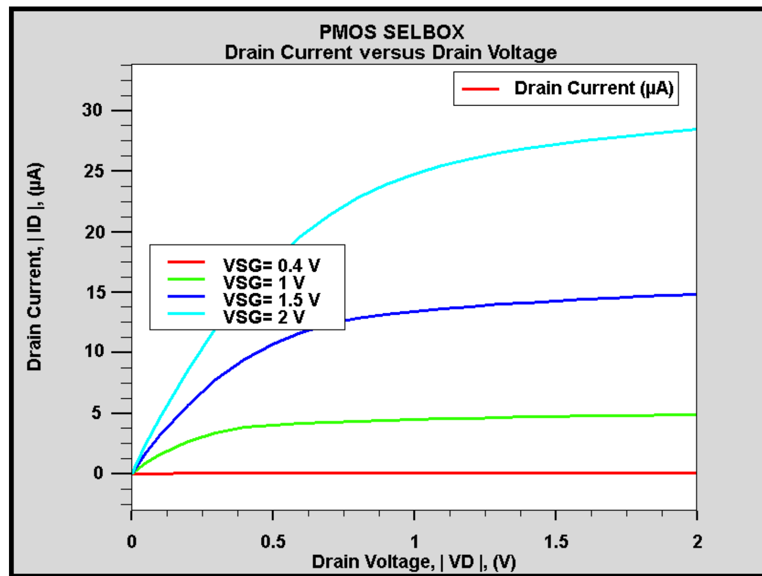

Figure 39: Drain current versus drain voltage for P-channel SELBOX MOSFET

The absolute leakage current versus the absolute drain voltage curve at small gate voltage for the P-channel SELBOX is shown in Figure 40.

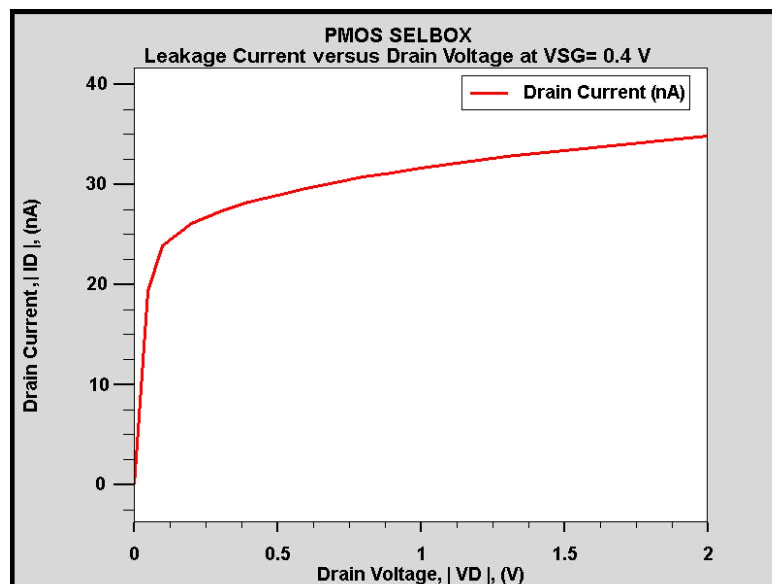

Figure 40: Leakage current versus drain voltage for P-channel SELBOX MOSFET at VSG=0.4V

The next section will illustrate the comparison between the different devices in power dissipation to show the advantage of SELBOX in reducing power dissipation without any kink effect.

5.3 Static power dissipation

5.3.1 NMOS devices.

Power dissipation graphs have been drawn for the three devices for NMOS at four different values for V_{GS}.

At V_{GS}= 0.4V, the static power dissipation curve of the SOI diverged sharply from the Bulk and SELBOX curves as shown in Figure 41.

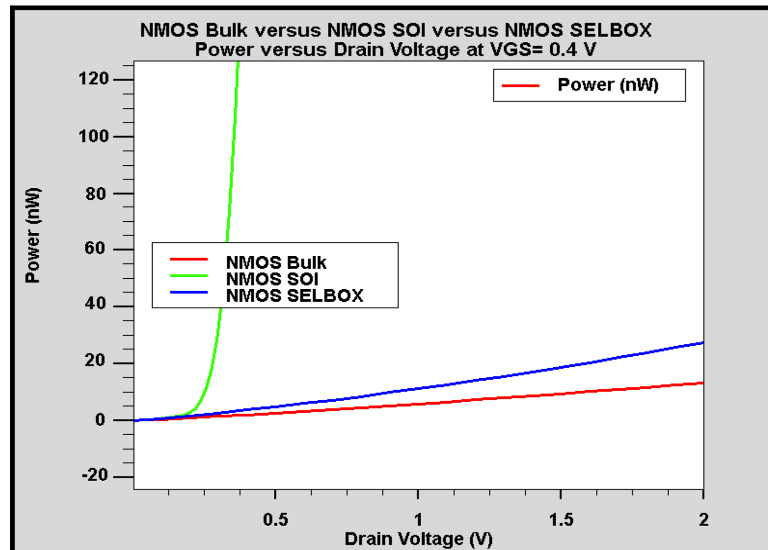

Figure 41: Power dissipation of Bulk, SOI, and SELBOX for NMOS at VGS=0.4V

At V_{GS}= 1V, the static power dissipation curve of the SOI becomes closer to the SELBOX and Bulk curves as shown in Figure 42.

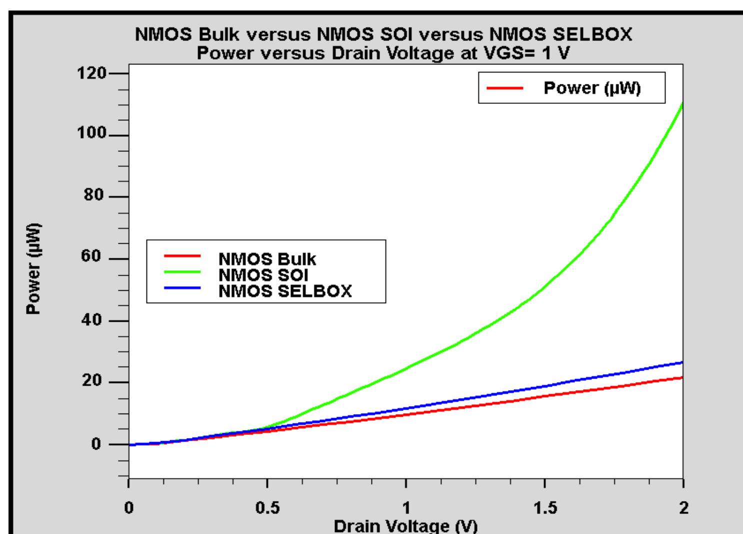

Figure 42: Power dissipation of Bulk, SOI, and SELBOX for NMOS at VGS=1V

At V_{GS}= 1.5V, the static power dissipation curve of the SOI becomes closer to the SELBOX and Bulk curves more than V_{GS}= 1V as shown in Figure 43.

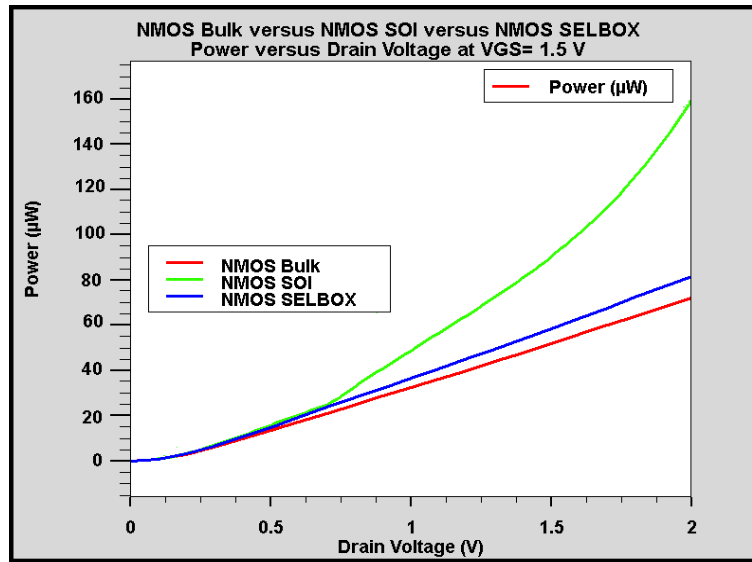

Figure 43: Power dissipation of Bulk, SOI, and SELBOX for NMOS at VGS=1.5V

At V_{GS}= 2V, the static power dissipation curve of the SOI becomes closer to the Bulk and SELBOX curves but still there is an observed difference in between as shown in Figure 44.

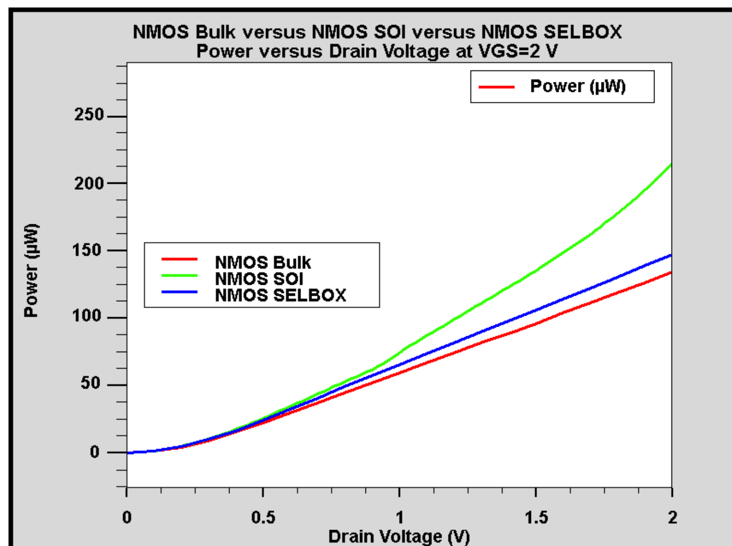

Figure 44: Power dissipation of Bulk, SOI, and SELBOX for NMOS at VGS=2V

In the previous four graphs, SELBOX is in the middle and close to Bulk's curve. This shows that SELBOX has the advantages of SOI while eliminating its disadvantages.

5.3.2 PMOS devices.

Power dissipation graphs have been drawn for the three devices for PMOS at four different values for V_{SG}.

At V_{SG}= 0.4V, the static power dissipation curve of the SELBOX is lower than the Bulk and the SOI as shown in Figure 45.

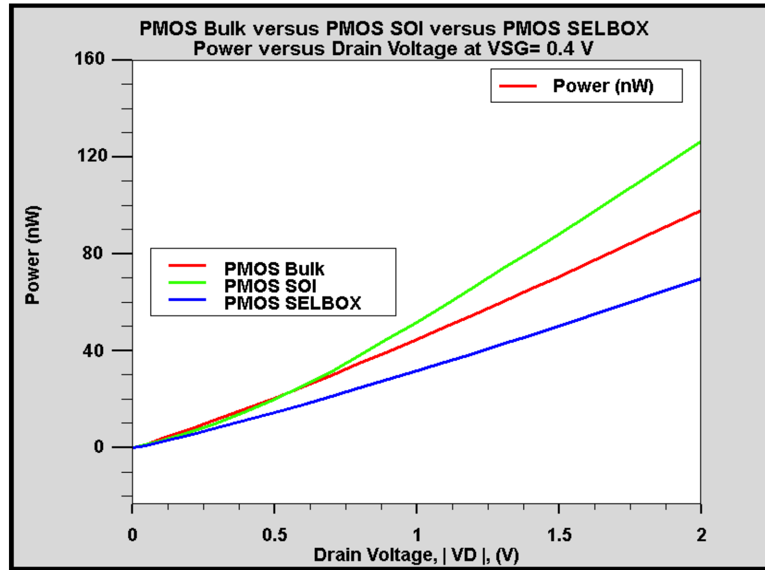

Figure 45: Power dissipation of Bulk, SOI, and SELBOX for PMOS at VSG= 0.4V

At V_{SG}= 1V, the static power dissipation curve of the SELBOX is still lower than the Bulk and the SOI but it became closer to the Bulk curve as shown in Figure 46.

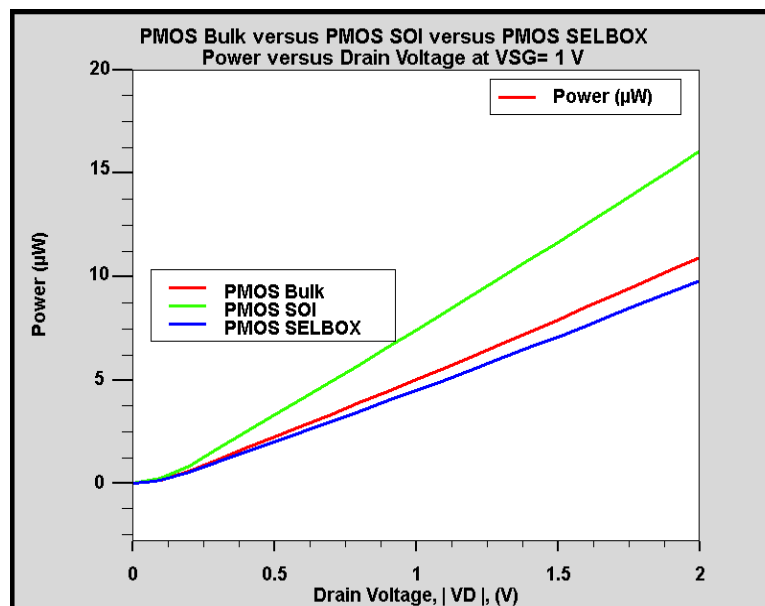

Figure 46: Power dissipation of Bulk, SOI, and SELBOX for PMOS at VSG= 1V

At V_{SG}= 1.5V, the static power dissipation curve of SELBOX is still the lowest but it is becoming closer to the Bulk curve as source-gate voltage increases. The SOI curve is still far away from others as shown in Figure 47.

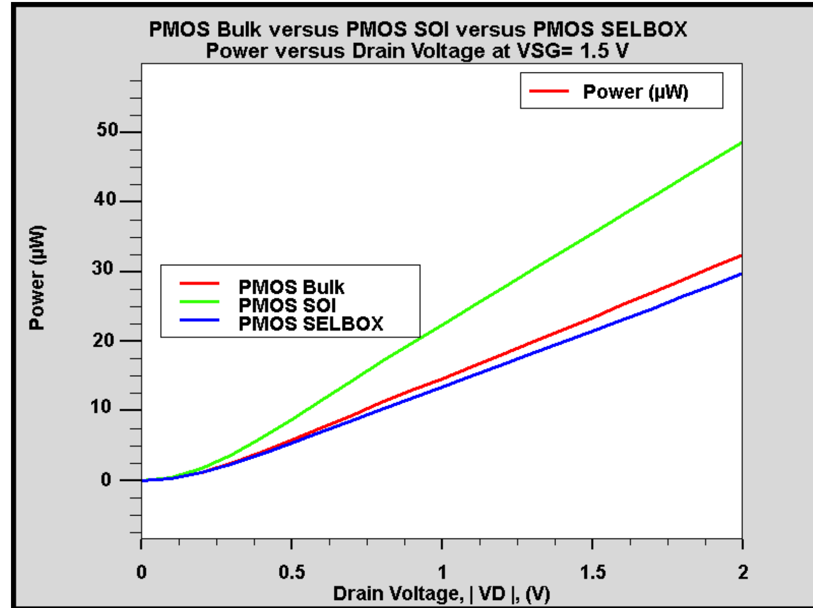

Figure 47: Power dissipation of Bulk, SOI, and SELBOX for PMOS at VSG= 1.5V

At V_{SG}= 2V, the static power dissipation curve of the PMOS SELBOX is very close to the Bulk but it is still the lowest as shown in Figure 48.

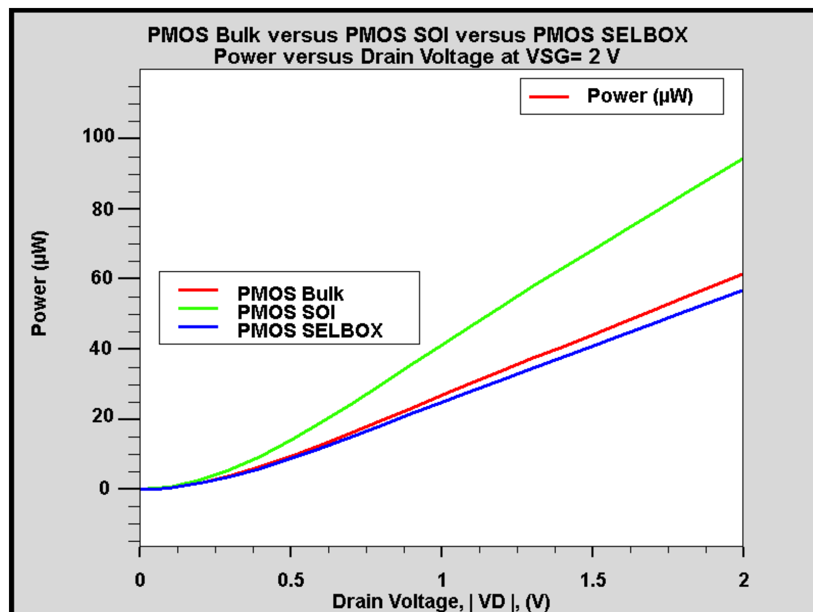

Figure 48: Power dissipation of Bulk, SOI, and SELBOX for PMOS at VSG= 2V

SELBOX as a single device works very well in reducing static power dissipation and in eliminating the kink effect with saving the advantages of SOI. The next chapter will illustrate the simulation of the devices as CMOS.

Chapter 6: Power Dissipation of CMOS Devices

In this chapter, an explanation of all the steps of CMOS device processing and the obtained results are presented and compared. Simulations were performed using the Silvaco software, starting from the CMOS as Bulk to the CMOS as SELBOX. The procedure can be summarized as follows:

4. Simulate the three CMOS devices: Bulk, SOI, and SELBOX.
5. Obtain the I-V characteristics for all devices:
    - Drain current versus gate voltage for NMOS and PMOS.
6. Show dissipated power versus input voltage.
7. Compare static power dissipation of the three devices in four stages:
    - Input voltage less than threshold voltage (0.6 volts).
    - Input voltage less than $V_{DD}/2$ volts.
    - Input voltage greater than $V_{DD}/2$ volts.
    - Input voltage greater than (V_{DD}- V_{TH}) volts.

The simulated devices were fabricated in such a way to reduce power dissipation by controlling the doping level for each, the channel length, the oxidation thickness, and the gap length of SELBOX.

The structures were simulated and tested under a specific threshold voltage of around 0.6 V for Bulk, SOI and SELBOX. In this chapter we demonstrate that the SELBOX as a CMOS device has the advantages of the other two devices in some characteristics such as low power dissipation, no kink effect, and no self-heating effect.

The technology which is used in this test is 90 nm in order to compare it with the state of the art devices [70] [71].

6.1 CMOS as Bulk

Each CMOS transistor was tested separately by making the other transistor OFF through simulation just to make sure that the transistors were working properly.

Then the test was carried out for the Bulk CMOS as one device to get the characteristics and compare them with the other two devices, SOI and SELBOX.

First, Bulk CMOS was fabricated through simulation with channel length equals to 90 nm. The structure of Bulk CMOS is shown in Figure 49.

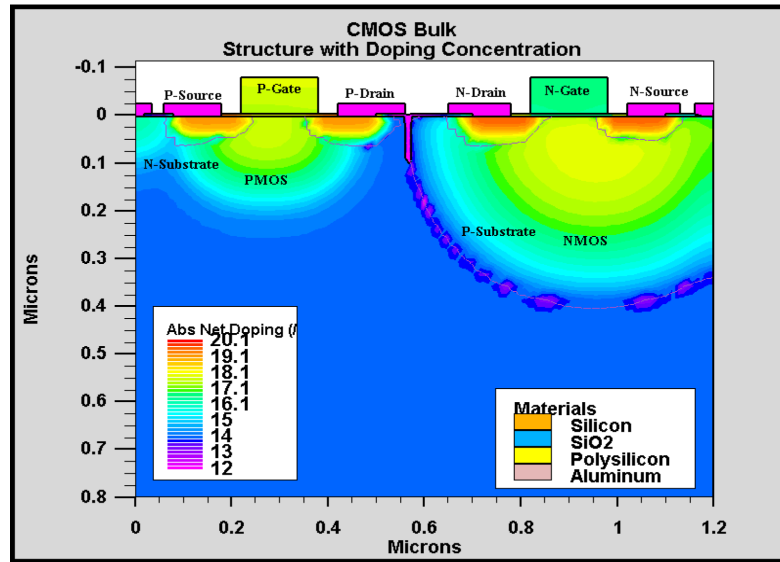

Figure 49: Bulk CMOS structure

As depicted in Figure 49, there is a small isolation between the two transistors just to have a similar structure to SOI and SELBOX as we will see later in this chapter.

The test was conducted for the transistors separately to make sure about the characteristics of each. For the NMOS test, we shorted the PMOS by connecting all electrodes to the ground. The N-Source and P-Substrate were also connected to the ground. Then we applied 1 volt on the N-Drain, and different DC voltages were applied on the N-Gate. The outcome result is shown in Figure 50.

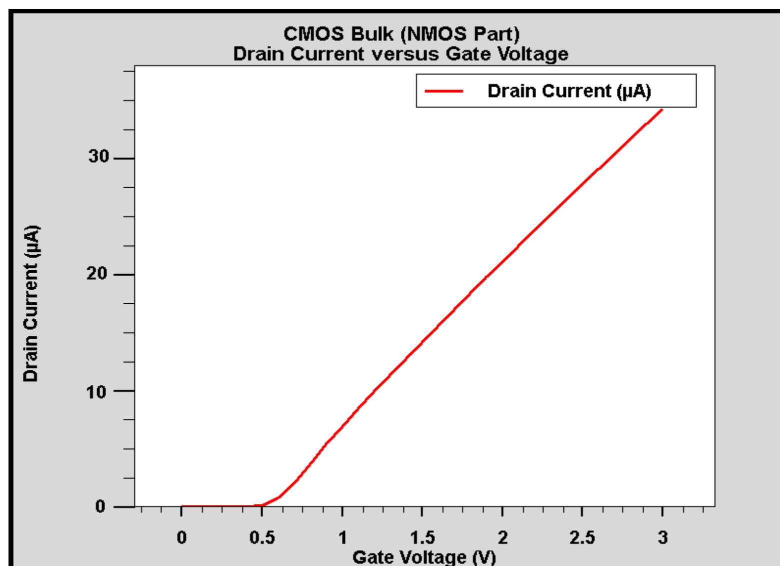

Figure 50: Drain current versus gate voltage for NMOS part

As shown in Figure 50, the theoretical threshold voltage is around 0.6 volts. We were trying to get the same threshold voltage for all transistors in this thesis.

After that, the test was done for the PMOS transistor alone by shorting the NMOS. The short circuit was achieved by connecting all electrodes to the ground. The P-Source and N-Substrate were also connected to the ground. Then we applied -1 volt on the P-Drain, and different DC voltages were applied on the P-Gate. The outcome result is shown in Figure 51.

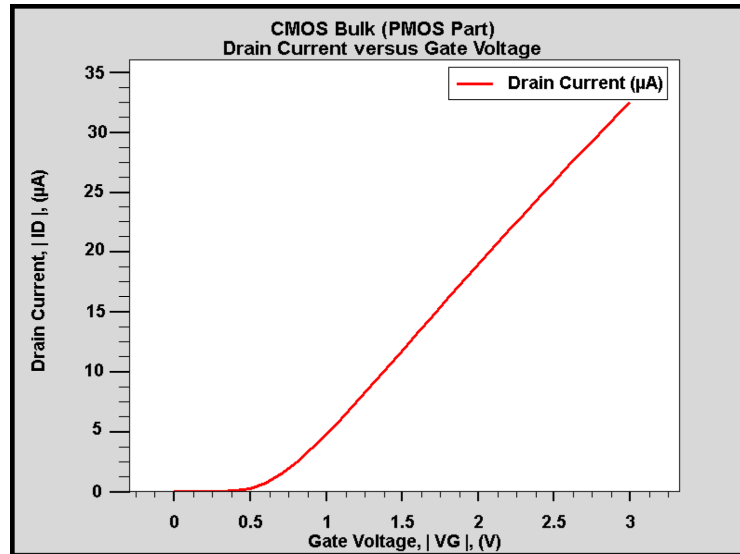

Figure 51: Drain current versus gate voltage for PMOS Part

As depicted in Figure 51, threshold voltage is around 0.6 and drain current is slightly less than the NMOS drain current.

After getting the results of the transistors as single devices, a CMOS device was built by connecting the two transistors together using Mixed-Mode simulation; the Mixed-Mode module of Atlas enables circuit simulation using physically-based models. The drains and the gates were connected to each other and the source of each transistor was connected to its own substrate. A fixed 3-volt was connected to the P-channel source, a changing DC voltage (0 to 3 volts) was connected to the gate, and the N-channel source was connected to the ground.

The following graph shows power versus input voltage. Power is calculated by using the following equation:

$$P = I_{DD} * V_{DD} \text{ (mW)} \quad (8)$$

where P is the power in mW, I_{DD} is the current which flows into the source of the PMOS in A, and V_{DD} is the source voltage in V.

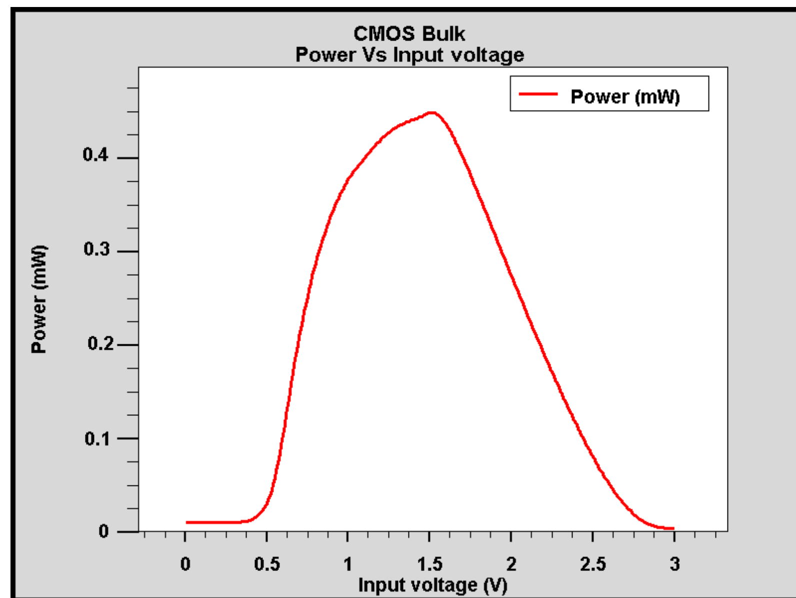

Figure 52: Power versus input voltage

It is noticed from Figure 52 that power reaches its maximum around V_{GS}= 1.5 volts and it reaches its minimum at lower and higher V_{GS} values but it is not reaching zero mW.

Modeling

Figure 52 can be divided into 5 regions as shown in Figure 53.

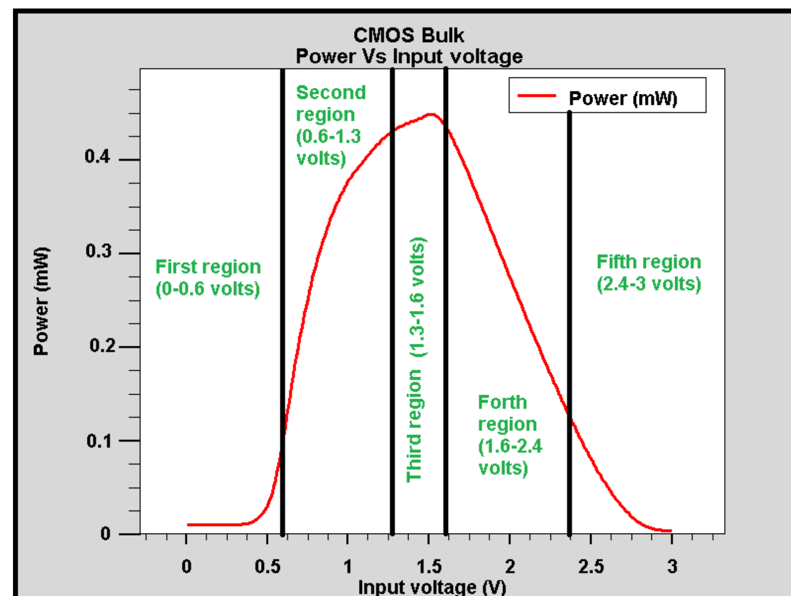

Figure 53: Regions of operation

In the simulated Bulk CMOS, the width of the gate equal to the channel length so $\frac{W}{L}$ ratio is considered as 1. Lambda λ is assumed to be $0.22V^{-1}$ for NMOS and $0.29V^{-1}$ for PMOS. The source voltage V_{DD} is fixed as 3 volts.

First region

This region is known as the subthreshold region, where NMOS is OFF while PMOS is in triode status. The equation used in this stage is [73]:

PMOS drain current

$$I_{DP\ triode} = \mu_p\ C_{ox}\frac{W}{L}\left(V_{DD} - V_{Input} - |V_{TH}| - \frac{(V_{DD}-V_D)}{2}\right) * (V_{DD} - V_D) \qquad (9)$$

Using equations (5) and (8); $C_{ox} = 0.056\ F/m^2$ and $\mu_p =\ 59.36\ \text{cm}^2/\text{V.s}$, V_{DD}= 3 volts and $|V_{TH}|$ = 0.6 volts. In the first stage; the output voltage is equal to the source voltage, V_{Input} is 0 volts and for accuracy we can consider that output voltage V_D is 2.999999 volts. The power is calculated by using equation (9). In this stage, three points were tested which are shown in Table 9

Table 9: Result of the first region

V_{Input} (V)	Modeled $Power\ (mW)$	Simulated $Power\ (mW)$
0.01	2.38E-06	2.70E-06
0.1	2.29E-06	3.00E-06
0.2	2.19E-04	3.00E-04

Second region

In this region both transistors are ON, the PMOS still in the triode status while the NMOS is in saturation. Both currents are equal in magnitude. To calculate the current through the transistors we used the following equations [73]:

$$I_{DP\ triode} =\ I_{DN\ saturation} \qquad (10)$$

$$\mu_p\, C_{ox} \frac{W}{L}\left(V_{DD} - V_{Input} - |V_{TH}| - \frac{(V_{DD} - V_D)}{2}\right)(V_{DD} - V_D) = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left(V_{Input} - V_{TH}\right)^2 (1 + \lambda V_D)$$

where

$$I_{DN\ saturation} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left(V_{Input} - V_{TH}\right)^2 (1 + \lambda V_D) \quad (11)$$

Using equations (5) and (8); $C_{ox} = 0.056\ F/m^2$ and $\mu_n = 89.20\ \mathrm{cm^2/V.s}$.

In the beginning, the output voltage was calculated, and then the result was used to calculate the current at specified input voltage within the region. The results of the calculated PMOS power of different input voltages are shown in Table 10.

Table 10: Results of the second region

V_{Input} (V)	Modeled $Power\ (mW)$	Simulated $Power\ (mW)$
0.7	0.153	0.207
1	0.338	0.377
1.3	0.490	0.433

Third region

In this region, both transistors are in saturation with the same current flow through them. To calculate the current, the following equation was used [73]:

$$I_{DP\ saturation} = I_{DN\ saturation} \quad (12)$$

$$\frac{1}{2}\mu_p C_{ox} \frac{W}{L}\left(V_{DD} - V_{Input} - |V_{TH}|\right)^2 (1 + \lambda_p (V_{DD} - V_D)) = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left(V_{Input} - V_{TH}\right)^2 (1 + \lambda_n V_D)$$

In the beginning, output voltage was calculated, and then the result used to calculate the current at specified input voltage within the region. The result of the calculated PMOS power of input voltages equal to 1.5 volts is shown in Table 11.

Table 11: Results of the third region

V_{Input} (V)	Modeled $Power\ (mW)$	Simulated $Power\ (mW)$
1.5	0.490	0.450

Fourth region

In this region, NMOS will be in triode state while PMOS will stay in the saturation state. To calculate the flowing current, the following equation was used [73]:

$$I_{DN\ triode} = I_{DP\ saturation} \tag{13}$$

$$\mu_n\, C_{ox}\frac{W}{L}\left(V_{Input} - |V_{TH}| - \frac{V_D}{2}\right)V_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{DD} - V_{Input} - V_{TH}\right)^2\left(1 + \lambda_p(V_{DD} - V_D)\right)$$

The results of the calculated PMOS power of different input voltages are shown in Table 12.

Table 12: Results of the fourth region

V_{Input} (V)	Modeled $Power\ (mW)$	Simulated $Power\ (mW)$
1.7	0.315	0.405
2	0.218	0.282
2.2	0.190	0.252

Fifth region

This region is known as the second subthreshold region, where PMOS is OFF while NMOS is in triode status. The equation used in this stage was [73]:

NMOS drain current

$$I_{DN\ triode} = \mu_n\, C_{ox}\frac{W}{L}\left(V_{Input} - V_{TH} - \frac{V_D}{2}\right) * V_D \tag{14}$$

V_{DD}= 3 V and V_{TH} = 0.6 V. In this stage, output voltage is equal to zero; for accuracy we can consider that output voltage V_D is 0.00001 V. In this stage, three points were tested which are shown in Table 13.

Table 13: Results of the fifth region

V_{Input} (V)	Modeled $Power\ (mW)$	Simulated $Power\ (mW)$
2.5	0.0796	0.105
2.7	3.96E-03	5.40E-03
3	4.40E-05	3.90E-05

Figure 54 shows the comparison between the simulated and modeled power. It shows that there is a small difference between the simulated and modeled results. This difference is due to the assumed lambda, and just a few points were tested to make sure about the model. If lambda was accurate and the points were many, we will get results approximately equal to the simulated results.

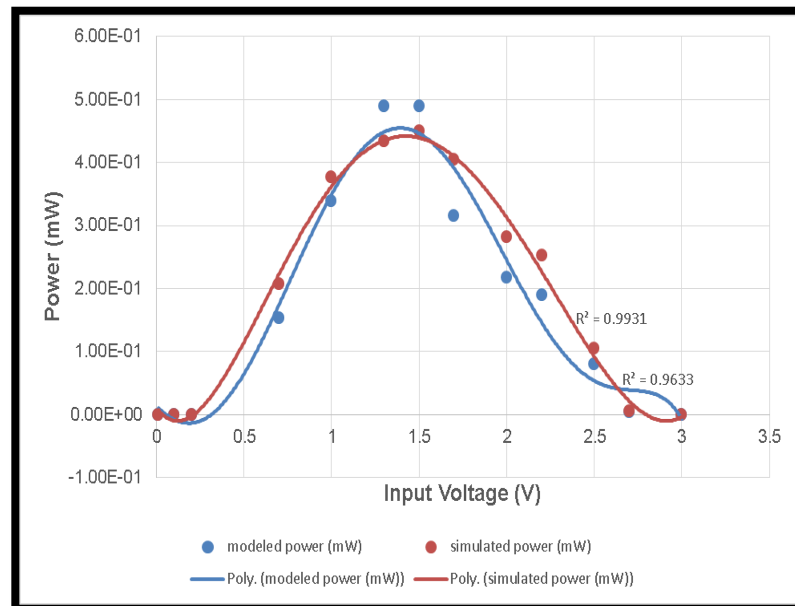

Figure 54: Comparison between the simulated and modeled powers.

6.2 CMOS SOI

In this part, we used the CMOS Bulk structure but with an added isolation layer in the substrate as shown in Figure 55.

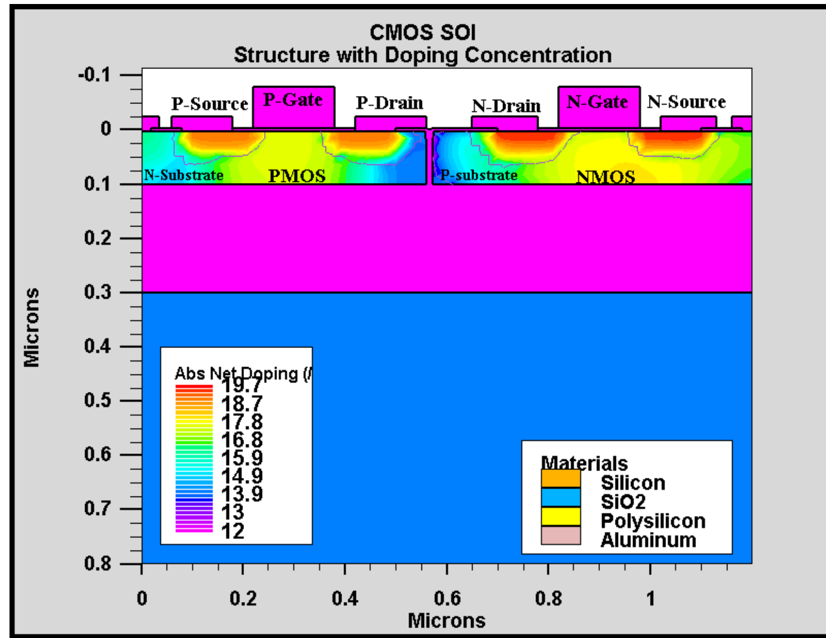

Figure 55: CMOS SOI structure

As we can see in Figure 55, the upper part of the device was isolated completely from the lower part. So the operation took place just in the upper layer which has a thickness of 0.1 μm.

The same procedure of testing the CMOS Bulk was repeated in this part. First, the test was for each transistor separately. Figure 56 shows the result of testing the NMOS transistor alone. Figure 57 shows the result of testing the PMOS transistor alone.

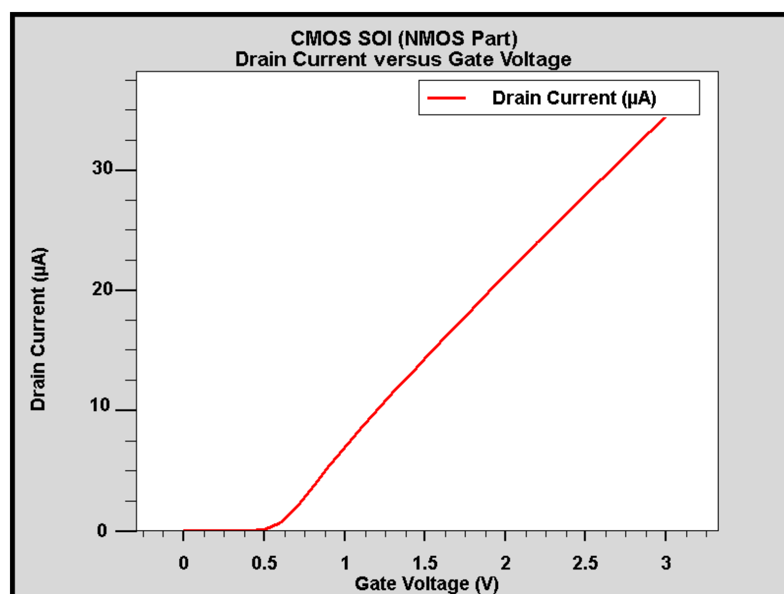

Figure 56: Drain current versus gate voltage NMOS SOI

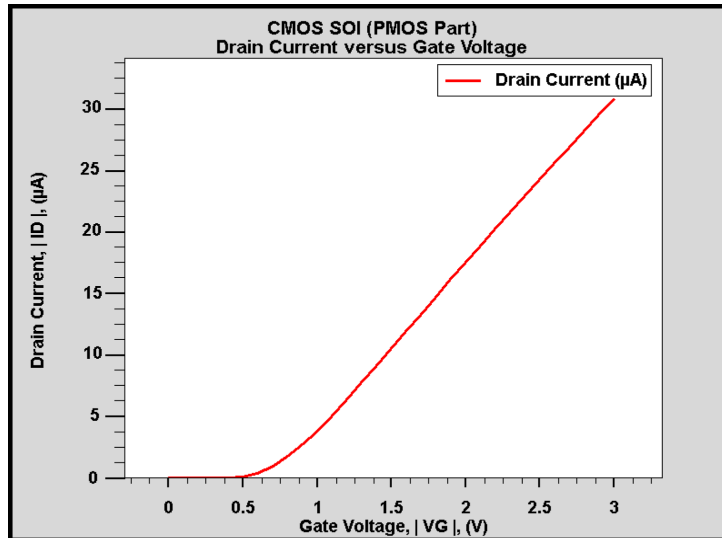

Figure 57: Drain current versus gate voltage for PMOS SOI

Then, both transistors were connected together by using Mixed-Mode simulation and the test steps of the CMOS Bulk were repeated with the same conditions.

Figure 58 shows the behavior of power versus input voltage of CMOS SOI. It is shown that power starts from zero and ends at approximately zero watts. Also it shows that maximum power is around 0.4 mW.

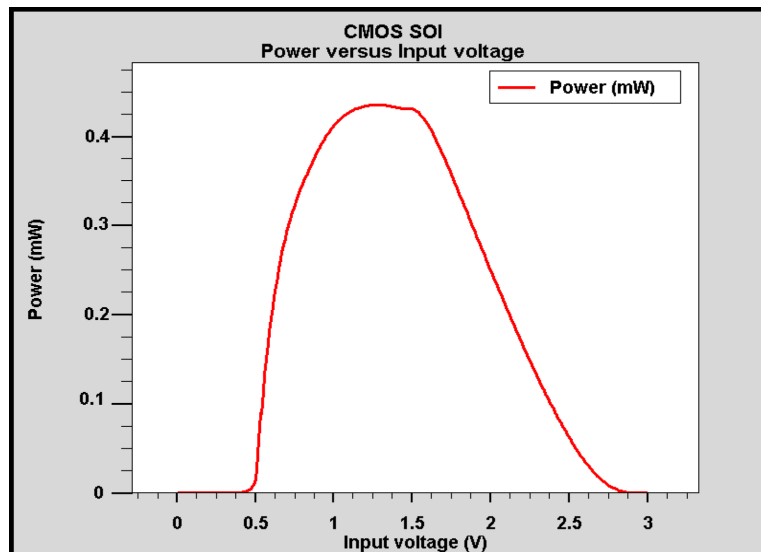

Figure 58: Power versus input voltage

6.3 CMOS SELBOX

In this part we used the CMOS SOI structure but with two gaps in the isolation layer in the substrate, one gap under each gate with length equal to 9 nm as shown in Figure 59.

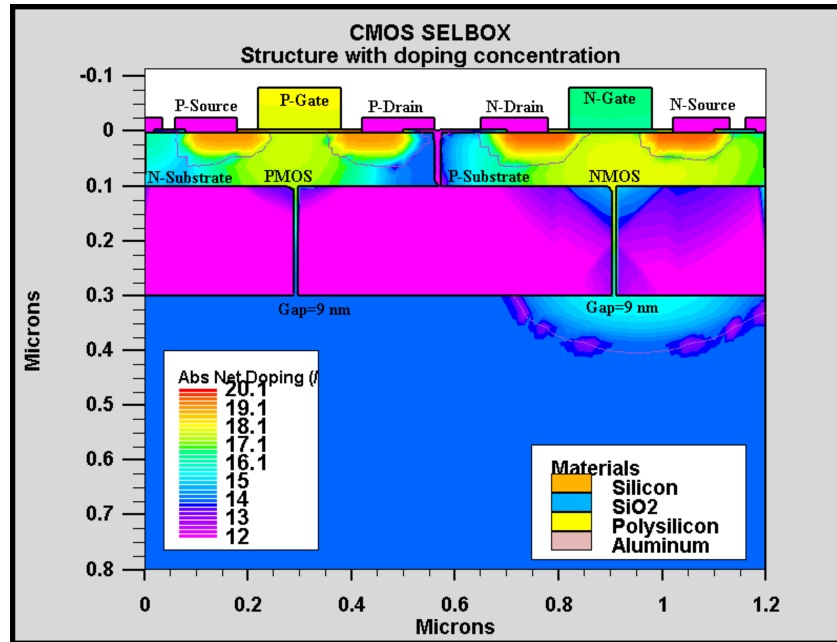

Figure 59: CMOS SELBOX structure

As we can see in Figure 59, the gap under the N-gate gave the opportunity for the P-well to spread under the isolator and also the self-heating effect was reduced.

The same procedure of testing the previous devices was repeated in this part. First, the test was done for each transistor separately. Figure 60 shows the result of testing the NMOS transistor alone. Figure 61 shows the result of testing the PMOS transistor alone.

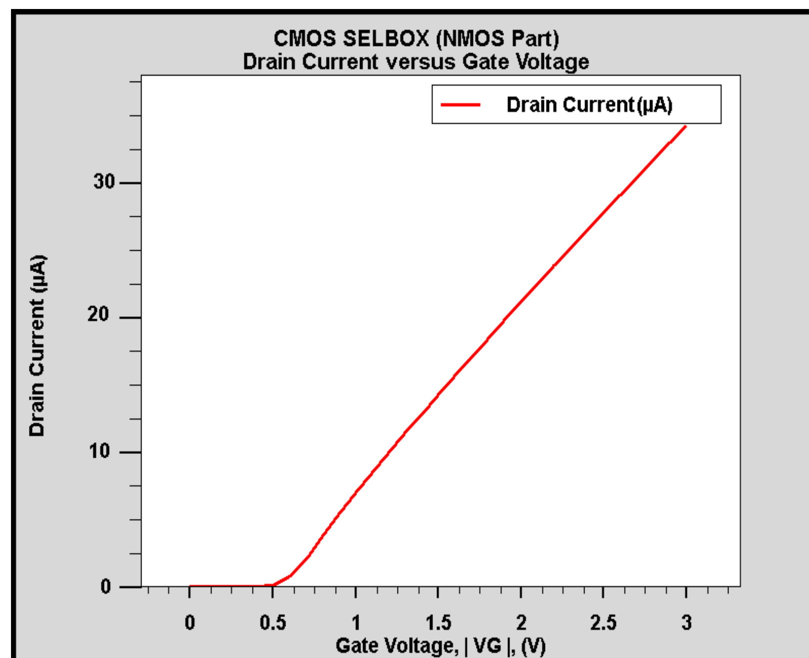

Figure 60: Drain current versus gate voltage for NMOS SELBOX

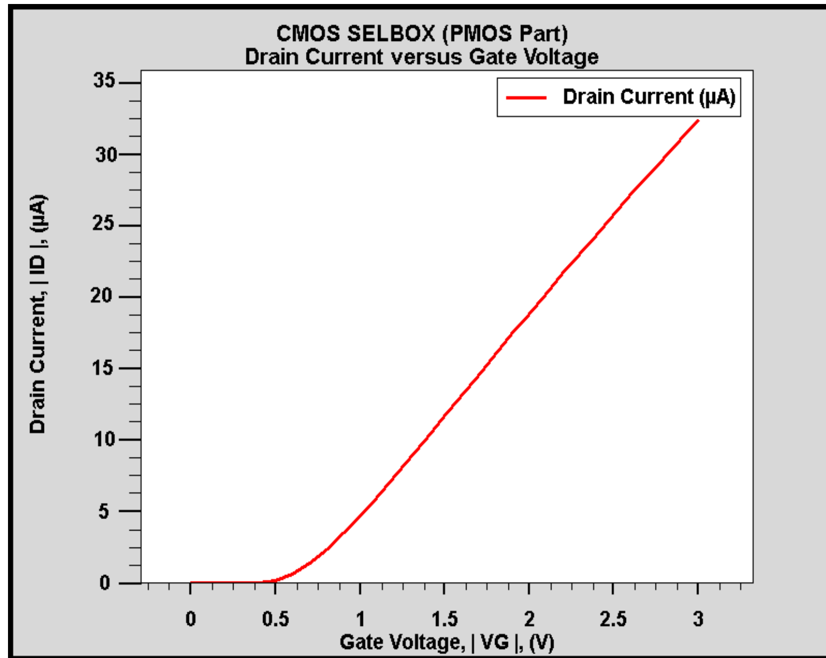

Figure 61: Drain current versus gate voltage for PMOS SELBOX

In Figures 60 and 61, the behaviors of SELBOX transistors as individual devices are the same as Bulk and SOI transistors. Observed differences will be found in the devices as a CMOS. This will be illustrated later in this chapter.

Figure 62 shows the behavior of power versus input voltage of the CMOS SELBOX device.

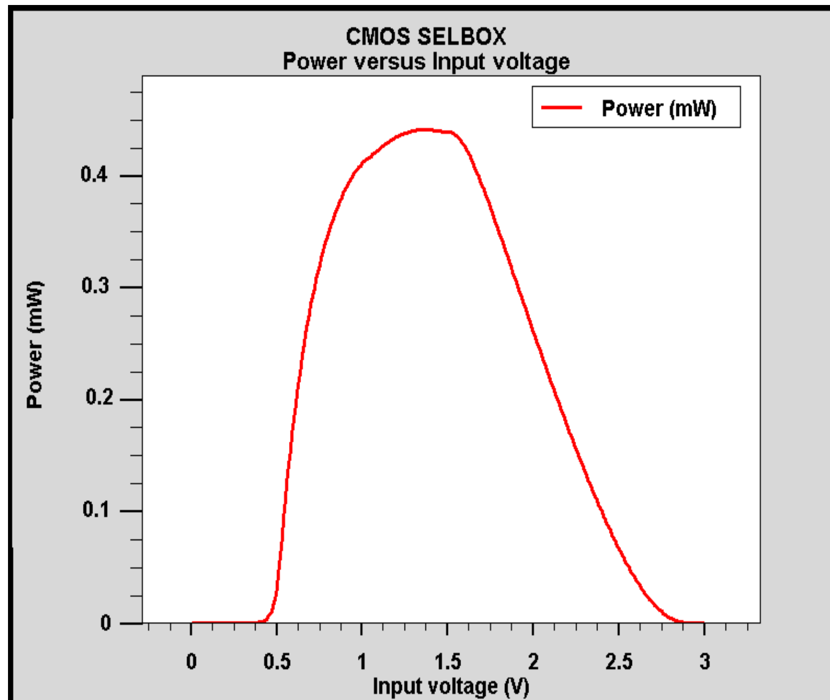

Figure 62: Power versus input voltage for CMOS SELBOX

6.4 Comparison

In this section the comparison between the three CMOS devices will be illustrated briefly. Power versus input voltage will be explained in four stages:

1. Input voltage less than threshold voltage (0.6 volts).
2. Input voltage less than $V_{DD}/2$ volts.
3. Input voltage greater than $V_{DD}/2$ volts.
4. Input voltage greater than (V_{DD}- V_{TH}).

6.4.1 First stage: Input voltage less than threshold voltage (0.6 V).

This stage is the subthreshold region where input voltage is between zero and threshold voltage. Figure 63 shows the behavior of power for the three devices under the same conditions in log scale.

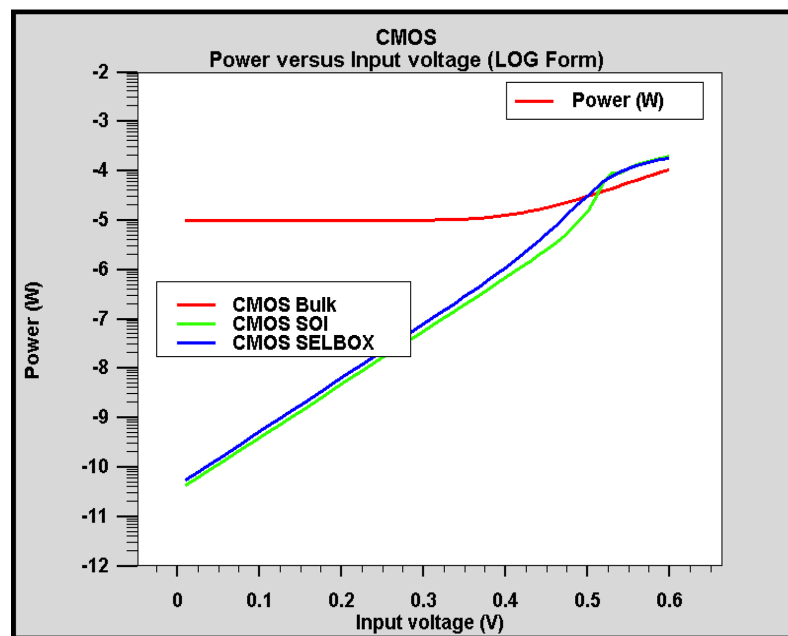

Figure 63: Power versus input voltage in the subthreshold region (LOG Form)

It is shown in Figure 63 that the power curves of SOI and SELBOX are much lower than Bulk. At 0.475 volts, SOI and SELBOX exceed Bulk's curve slightly.

6.4.2 Second stage: Input voltage less than VDD/2.

In this stage, input voltage is between zero and ($V_{DD}/2$) volts where V_{DD}=3 volts. The Figure 64 shows the behavior of power for the three devices in log scale. When input voltage reaches approximately 0.5 volts, SOI and SELBOX become greater than

Bulk until 1.2 volts. After that SOI returns back as the lowest and SELBOX goes under Bulk. In all cases, SELBOX is in the middle and close to SOI.

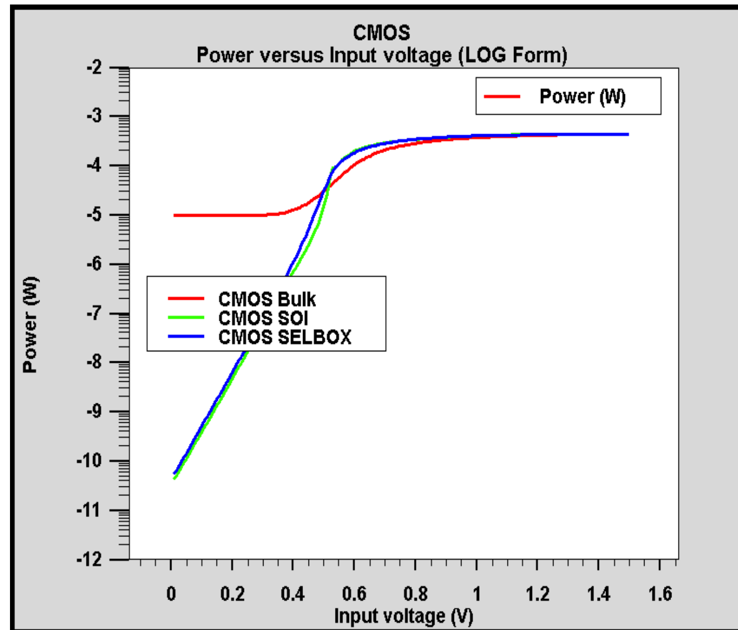

Figure 64: Power versus input voltage less than 1.5V (LOG Form)

6.4.3 Third stage: Input voltage greater than VDD/2.

In this stage, input voltage is between (V_{DD}/2) and V_{DD}. Figure 65 shows the behavior of power for the three devices in log scale.

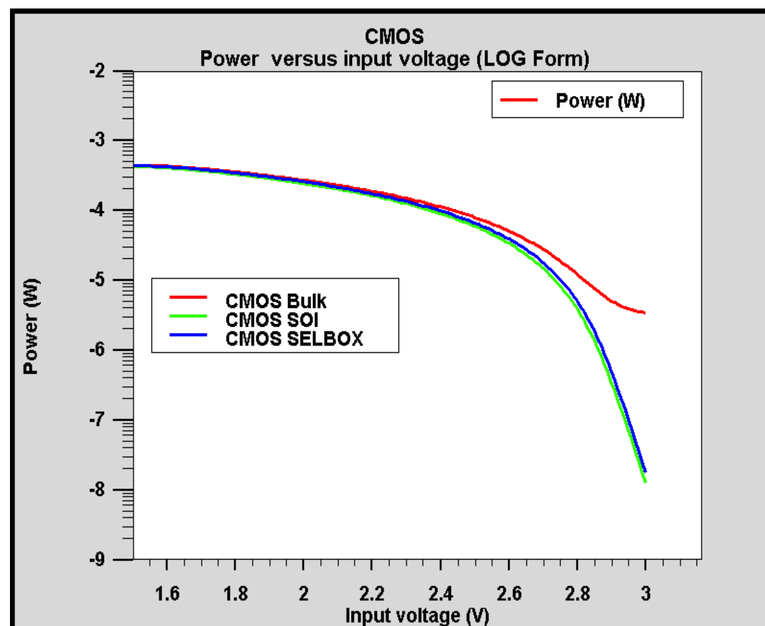

Figure 65: Power versus input voltage greater than 1.5V (LOG Form)

As shown in Figure 65, Bulk's curve is slightly higher than the other curves until we reach the second OFF stage for the CMOS where input voltage is greater than

V_{DD}-V_{TH}. After that Bulk's power is much greater than the others and SELBOX is always close to SOI.

This greater power dissipation is due to well leakage in Bulk which was illustrated previously in Chapter 2. This leakage keeps the CMOS Bulk's power dissipation higher than SOI and SELBOX. But well leakage is eliminated in SOI and SELBOX.

6.4.4 Forth stage: Input voltage greater than (VDD- VTH).

In the fourth stage, input voltage is greater than (V_{DD}-V_{TH}) 2.4 volts. Figure 66 shows the behavior of power for the three devices in log scale.

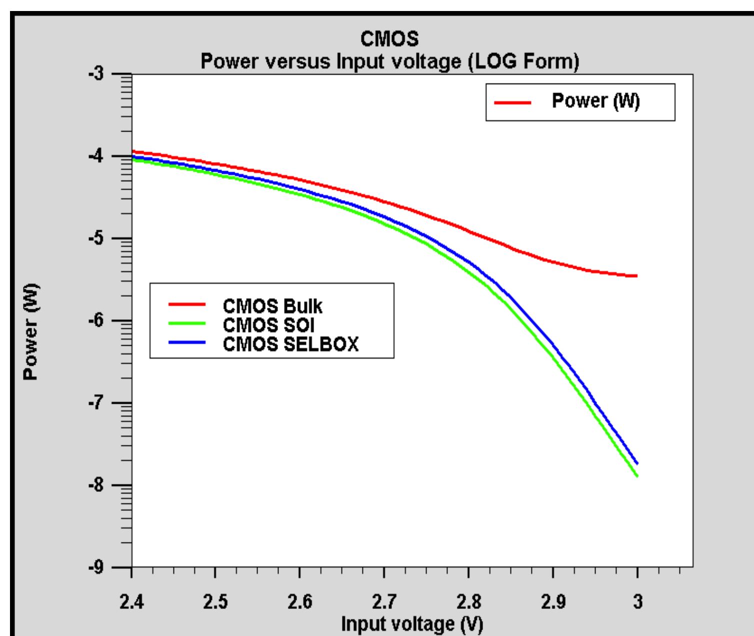

Figure 66: The Power versus input voltage greater than 2.4V (LOG Form)

It is very clear in Figure 66 that SOI and SELBOX have very close behavior in the OFF state and Bulk has greater power dissipation than the others.

We can conclude that SELBOX has the advantages of Bulk and SOI in terms of killing the kink effect, keeping away the self-heating effect, fast processing, and low power dissipation.

Chapter 7: Conclusion

7.2 Conclusion

In this thesis, a newly developed MOSFET was fabricated by simulation to produce low power dissipation device with high speed in operation, without the kink effect, and with low self-heating. This device was called a Selective Buried Oxide MOSFET (SELBOX). Single devices were fabricated and tested in three different structures using two channel types: Bulk, SOI, and SELBOX as N-channel and P-channel devices. Comparisons between the three devices of the same channel type were done for I-V and power characteristics. SELBOX proved that it can eliminate the kink effect and reduce power dissipation while keeping high speed in operation. Simulations of the three different structures of CMOS devices were conducted. SELBOX as CMOS device succeeded in reducing power dissipation and working as the SOI without the kink effect and with low self-heating.

In NMOS, static power dissipation for Bulk is less than that for SOI because of nonlinearity in the drain current-voltage characteristics of SOI, which is known as the kink effect due to the changes in body voltage of the device. For SELBOX, power dissipation is close to Bulk due to the eliminated kink effect.

In PMOS, drain current-voltage characteristics show that power dissipation will be very small compared to NMOS due to high resistivity. Also, leakage current has different behavior due to the body effect. Static power dissipation of SELBOX is the lowest. With increasing gate voltage, SELBOX power dissipation comes closer to Bulk.

In CMOS, static power dissipation of Bulk is higher than others due to well leakage. SELBOX has lower self-heating than SOI due to the gap in the isolation layer. The new device succeeded in both single and CMOS, in keeping the advantages of Bulk and SOI while eliminating their drawbacks.

Each device has its strengths and weaknesses; the new device’s weakness is the long fabrication process which needs more procedures than SOI.

7.3 Future work

In this thesis, the static power dissipation of SELBOX has been tested. But to have a full description about power characteristics of SELBOX, the dynamic power dissipation has to be tested and compared with other devices. Dynamic power dissipation happens due to the charging and discharging of the load capacitance.

The radiation effect is also an important factor and it has to be eliminated. CMOS resistivity to Total Ionizing Dose (TID) is due to the radiation induced charge tapping into the oxide layers or the gate. Depending on the function, nature, and position of the oxide, ionizing radiation may build electron-hole pairs in the isolation layer with subsequent trapping of holes at the interface between the silicon and oxide. In the gate oxide, an electric field is produced by hole tapping. This field may cause conductive channels to open between n+ diffusions. Threshold, voltage, mobility, and noise are affected by the resultant leakage current which flows between the drain and the source of the transistor or between the adjacent n+ regions (including the N-wall) [64]. It is believed that SELBOX can reduce this effect but this assumption must be tested and proved.

References

[1] J. Srinivasan, "An Overview of Static Power Dissipation," 2007. [Online]. Available: http://citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.24.4173. [Accessed 10 June 2015].

[2] [Online]. Available: http://low-powerdesign.com/article_microchip_rao.htm. [Accessed 20 June 2015].

[3] V. De and S. Borkar, "Technology and Design Challenges for Low Power and High Performance [microprocessors]," *Proceedings. of the International Symposium on Low Power Electronics and Design, 1999.* San Diego, CA, USA, 17 August 1999.

[4] M. Johnson, D. Somasekhar, L.Y. Chiou and K. Roy, "Leakage Control with Efficient use of Transistor Stacks in Single Threshold CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 10, no. 1, pp. 1 - 5, August 2002.

[5] M. Johnson, D. Somasekhar and K. Roy, "Models and Algorithms for Bounds on Leakage in CMOS circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 18, no. 6, pp. 714 - 725, August 2002.

[6] N. Saxena and S. Soni, "Leakage Current Reduction in CMOS Circuits using Stacking Effect," *International Journal of Application or Innovation in Engineering & Management (IJAIEM),* vol. 2, no. 11, pp. 213-216, November 2013.

[7] J. T. Kao and A. P. Chandrakasan, "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," *IEEE Journal of Solid-State Circuits,* vol. 35, no. 7, pp. 1009 - 1018, July 2000.

[8] R. Udaiyakumar and K. Sankaranarayanan, "Dual Threshold Transistor Stacking (DTTS) - A Novel Technique for Static Power Reduction in Nanoscale CMOS Circuits," *European Journal of Scientific Research,* vol. 72, no. 2, pp. 184-194, February 2012.

[9] M. Horiguchi, T. Sakata and B. Kiyoo Itoh, "Switched-Source-Impedance CMOS Circuit for Low Standby Subthreshold Current Giga-Scale LSI's," *IEEE Journal of Solid-State Circuits,* vol. 28, no. 11, pp. 1131 - 1135, November 1993.

[10] S. H. Kim and V. Mooney, "Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design," *2006 IFIP International Conference on Very Large Scale Integration,* Nice, 16-18 October 2006.

[11] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu and J. Yamada, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," *IEEE Journal of Solid-State Circuits,* vol. 30, no. 8, pp. 847 - 854, August 2002.

[12] M. Powell, S. H. Yang, B. Falsafi, K. Roy and T. Vijaykumar, "Gated-Vdd: a Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories," *Proceedings of the 2000 International Symposium on Low Power Electronics and Design,* 2000.

[13] H. Y. Lin, C. S. Lin, L. Y. Chiou and B. D. Liu, "Leakage Current Reduction in CMOS Logic Circuits," *Proceedings of the 2004 IEEE Asia-Pacific Conference on Circuits and Systems, 2004.*, Tainan, 6-9 December 2004.

[14] A. Abdollahi, F. Fallah and M. Pedram, "Leakage Current Reduction in CMOS VLSI Circuits by Input Vector Control," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 12, no. 2, pp. 140 - 154, February 2004.

[15] L. Yuan and G. Qu, "A Combined Gate Replacement and Input Vector Control Approach for Leakage Current Reduction," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 14, no. 2, pp. 173 - 182, February 2006.

[16] S. Katrue and D. Kudithipudi, "GALEOR: Leakage Reduction for CMOS Circuits," *15th IEEE International Conference on Electronics, Circuits and Systems, 2008. ICECS 2008.* St. Julien's, August 31 2008-September 3 2008.

[17] R. Gonzalez, B. Gordon and M. Horowitz, "Supply and Threshold Voltage Scaling

for Low Power CMOS," *IEEE Journal of Solid-State Circuits,* vol. 32, no. 8, pp. 1210 - 1216, August 1997.

[18] A. Chandrakasan, S. Sheng and R. Brodersen, "Low-Power CMOS Digital Design," *IEEE Journal of Solid-State Circuits,* vol. 27, no. 4, pp. 473 - 484, April 1992.

[19] V. Peluso, M. Steyaert and W. Sansen, *Design of Low-Voltage Low-Power CMOS Delta-Sigma A/D Converters,* Netherlands: Kluwer Academic Publishers, 1999, pp. 174.

[20] S. Thompson *et al.* "An Enhanced 130 nm Generation Logic Technology Featuring 60 nm Transistors Optimized for High Performance and Low Power at 0.7 - 1.4 V," *Technical Digest. International Meeting in Electron Devices, 2001. IEDM '01.*, Washington DC, USA, 2001.

[21] S. Thompson *et al.* "A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, low k ILD, and 1 /spl mu/m/sup 2/ SRAM Cell," *International Meeting* in *Electron Devices, 2002. IEDM '02.* San Francisco, CA, USA, 8-11 December 2002.

[22] P. Girard, C. Ladrault, S. Pravossoudovitch and D. Severac, "Technique for Reducing Power Consumption in CMOS Circuits," *Electronics Letters,* vol. 33, no. 6, pp. 485-486, June1997.

[23] P. Girard, C. Landrault, S. Pravossoudovitch and D. Severac, "A Gate Resizing Technique for High Reduction in Power Consumption," *Proceedings of the 1997 International Symposium on Low Power Electronics and Design, 1997.,* Monterey, CA, USA, 18-20 August 1997.

[24] S. P. Mohanty, R. Velagapudi, V. Mukherjee and H. Li, "Reduction of Direct Tunneling Power Dissipation During Behavioral Synthesis of Nanometer CMOS Circuits," *Proceedings of the IEEE Computer Society Annual Symposium* on *VLSI, 2005.* Texas, 11-12 May 2005.

[25] Association and S. Industry, "Semiconductor Industry Association," 2002. [Online].

Available: http://public.itrs.net. [Accessed 14 December 2014].

[26] F. Hamzaoglu and M. Stan, "Circuit-Level Techniques to Control Gate Leakage for Sub-100 nm CMOS," *Proceedings of the 2002 International Symposium on Low Power Electronics and Design, 2002. ISLPED '02.*, New York,USA, August 2002.

[27] A. Sultania, D. Sylvester and S. Sapatnekar, "Tradeoffs Between Gate Oxide Leakage and Delay for Dual T/Sub OX/ Circuits," *Proceedings of the Conference on Design Automation 2004. 41st*, San Diego, CA, USA, 7-11 July 2004.

[28] R. Lorenzo and S. Chaudhary, "Low Leakage and Minimum Energy Consumption in CMOS Logic Circuits," *2015 International Conference on Electronic Design, Computer Networks & Automated Verification (EDCAV),* Shillong, 29-30 January 2015.

[29] H. Mendez, "Fully Depleted SOI Designed for Low Power," *SOI Industry Consortium*, Land Creek Cove, Austin, USA, 2010.

[30] Ruchika, T. Sharma and K. Sharma, "Double Gate MOSFET Circuit Design," *Conference on Recent Advances and Innovations in Engineering (ICRAIE), 2014*, Jaipur, 9-11 May 2014.

[31] A. K. Shrivastava and S. Akashe, "Comparative Analysis of Low Power 10T and 14T Full Adder using Double Gate MOSFET at 45nm Technology," *International Journal of Computer Applications ,* vol. 75, no. 3, pp. 48-52, August 2013.

[32] J. Lee, H. Kim, J. Oh, J. Yang, W. Lee, J. Kim, M. Oh and Y. Koh, "A new SOI MOSFET for Low Power Applications," *Proceedings of the1998 IEEE International SOI Conference,* Stuart, FL, USA, 5-8 October 1998.

[33] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. Ko and C. Hu, "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," *IEEE Transactions on Electron Devices,* vol. 44, no. 3, pp. 414 - 422, August 2002.

[34] L. P. Yuan, C. C. Teng and S. M. Kang, "Statistical Estimation of Average Power Dissipation in CMOS VLSI Circuits Using Nonparametric Techniques," *1996*

International Symposium on Low Power Electronics and Design, Monterey, CA, 12-14 August 1996.

[35] A. S. Gaur and J. Budakoti, "Energy Efficient Advanced Low Power CMOS Design to Reduce Power Consumption in Deep Submicron Technologies in CMOS Circuit for VLSI Design," *International Journal of Advanced Research in Computer and Communication Engineering (IJARCCE),* vol. 3, no. 6, pp. 9, June 2014.

[36] J. Pelloie, "Using SOI to Achieve Low-Power Consumption in Digital," *Proceedings of the 2005 IEEE International Conference on SOI,* France, 3-6 Oct. 2005.

[37] S. Lin and J. KUO, *Low -Voltage SOI CMOS VLSI Devices and Circuits*, New York, USA: John Wiley & Sons, 1st edition, 2001.

[38] N. Madathumpadical, H. AlNashash, B. Mazhari and D. Pal, "Studies and Minimization of Kink Effect in SOI MOSFET Devices with SELBOX Structure," *2008 International Conference on Microelectronics, ICM 2008.* Sharjah, 14-17 December 2008.

[39] Y. Dong, M. Chen, J. Chen, X. Wang, X. Wang, P. He, X. Lin, L. Tian and Z. Li, "Patterned Buried Oxide Layers Under a Single MOSFET to Improve the Device Performance," *Semiconductor Science and Technology,* vol. 19, no. 3, pp. 25-29, March 2004.

[40] T. Agarwal, "Understanding CMOS Fabrication Technology," *EDGEFX.in Kits and Solutions, 2014.* [Online]. Available: http://www.edgefx.in/understanding-cmos-fabrication-technology/. [Accessed 8 November 2015].

[41] N. Madathumpadical, H. Al-Nashash, D. Pal and M. Chandra, "Thermal Model of MOSFET with SELBOX Structure," *Journal of Computational Electronics,* vol. 12, no. 4, pp. 803-811, December 2013.

[42] M. Knight and N. Glass, "Are Computer Chips on the Verge of a Quantum Leap?," *CNN.com, September 2013.* [Online]. Available: http://edition.cnn.com/2013/09/02/tech/innovation/are-computer-chips-verge-

quantum/. [Accessed 30 August 2015].

[43] H. Hagedoorn, "Intel Desktop Roadmap 2015 to 2H 2016 Shows Broadwell-E," *Guru3D.com, 16 July 2015*. [Online]. Available: http://wccftech.com/intel-14nm-skylake-processors-feature-pcie-4-ddr4-memory-sata-express/. [Accessed 30 August 2015].

[44] B. J. Van Zeghbroeck, "The MOSFET - Introduction," 2011. [Online]. Available: http://ecee.colorado.edu/~bart/book/mosfet.htm. [Accessed 16 June 2015].

[45] M. M. Atalla, E. Tannenbaum and E. J. Scheibner, "Stabilization of Silicon Surfaces by Thermally Grown Oxides," *Bell System Technical Journal,* vol. 38, no. 3, p. 749–783, May 1959.

[46] S. Natarajan, "Transistors: Past, Present, Future, and Future-er," *Device Research Conference (DRC), 2010*, South Bend, IN, 21-23 June 2010.

[47] A. Ortiz-Conde, F. J. García-Sánchez and J. Liou, "Extracting the Threshold Voltage from the Subthreshold to Strong Inversion Transition Region of MOSFETs," *Acta Científica Venezolana,* vol. 52, no. 3, pp. 176-187, March 1999.

[48] A. Ortiz-Conde, F. García Sánchez, J. Liou, A. Cerdeira, M. Estrada and Y. Yue, "A Review of Recent MOSFET Threshold Voltage Extraction Methods," *Microelectronics Reliability,* vol. 42, no. 4, pp. 583-596, April 2002.

[49] T. Ytterdal, Y. Cheng and T. A. Fjeldly, *MOSFET Device Physics and Operation, in Device Modelling for Analog and RF CMOS Circuit Design*, Chichester,UK: John Wiley & Sons, Ltd, 2003.

[50] M. Zabeli, N. Caka, M. Limani and Q. Kabashi, "The Impact of MOSFET's Physical Parameters on its Threshold Voltage," *Proceedings of the 6th WSEAS International Conference on Microelectronics, Nanoelectronics, Optoelectronics*, Istanbul, Turkey, 27-29 May 2007.

[51] V. Quenette *et al.*, "Electrical Characterization and Compact Modeling of MOSFET Body Effect," *9th International Conference of Ultimate Integration of Silicon, 2008.*

ULIS 2008., Udine, 12-14 March 2008.

[52] G. Dolny, S. Sapp, A. Elbanhaway and C. Wheatley, "The Influence of Body Effect and Threshold Voltage Reduction on Trench MOSFET Body Diode Characteristics," *Proceedings of the16th International Symposium on Power Semiconductor Devices and ICs, 2004. ISPSD '04.* USA, 24-27 May 2004.

[53] K. Green and J. Fossum, "A Simple Two-Dimensional Model for Subthreshold Channel-Length Modulation in Short-Channel MOSFETs," *IEEE Transactions on Electron Devices,* vol. 40, no. 8, pp. 1560 - 1563, August 2002.

[54] B. Deepaksubramanyan and A. Nunez, "Analysis of Subthreshold Leakage Reduction in CMOS Digital Circuits," *50th Midwest Symposium on Circuits and Systems, MWSCAS 2007.* , Montreal, Que., 5-8 August 2007.

[55] G. Consentino and G. Ardita, "A Simplified and Approximate Power MOSFET Intrinsic Capacitance Simulation: Theoretical Studies, Measures and Comparisons," *IEEE International Symposium on Industrial Electronics, ISIE 2008.* Cambridge, 30 June- 2 July 2008.

[56] M. Pelella *et al.*, "Advantages and Challenges of High Performance CMOS on SOI," *2001 IEEE International Conference on SOI,* , Durango, CO, USA, 1-4 October 2001.

[57] R. Huang *et al.*, "Novel Localized-SOI MOSFET's Combining the Advantages of SOI and Bulk Substrates for Highly-Scaled Devices," *2005 IEEE Conference on Electron Devices and Solid-State Circuits,* China, 19-21 December 2005.

[58] T. Hiramoto, A. Kumar, T. Mizutani, J. Nishimura and T. Saraya, "Statistical Advantages of Intrinsic Channel Fully Depleted SOI MOSFETs Over Bulk MOSFETs," *2011 IEEE Custom Integrated Circuits Conference (CICC),* , San Jose, CA, 19-21 September 2011.

[59] M. Yoshimi *et al.*, "Advantages of Low Voltage Applications and Issues to be Solved in SOI Technology [DRAMs]," *Proceedings of the 1996 IEEE International*

Conference on SOI, Sanibel Island, FL, 30 September- 3 October 1996.

[60] O. Faynot *et al.*, "Advanced SOI Technologies: Advantages and Drawbacks," *2006 International Workshop on Junction Technology. IWJT '06.* Shanghai, 2006.

[61] W. Jin, S. Fung, W. Liu, P. Chan and C. Hu, "Self-Heating Characterization for SOI MOSFET Based on AC Output Conductance," *1999 International Conference on Electron Devices. IEDM '99. Technical Digest.*, Washington, DC, USA, 5-8 December 1999.

[62] B. Iñ́gueza, J.-P. Raskinb, P. Simonb, D. Flandrec and J. Segurad, "A Review of Leakage Current in SOI CMOS ICs: Impact on Parametric Testing Techniques," *Solid-State Electronics,* vol. 47, no. 11, pp. 1959–1967, November 2003.

[63] Z. X. Zhang, Q. Lin, M. Zhu and C. L. Lin, "A New Structure of SOI MOSFET for Reducing Self-Heating Effect," *Ceramics International,* vol. 30, no. 7, pp. 1289–1293, July 2004.

[64] J. Samanta, P. Bishnu De, B. Bag and K. Maity Raj, "Comparative Study for Delay & Power Dissipation of CMOS Inverter in UDSM Range," *International Journal of Soft Computing and Engineering (IJSCE),* vol. 1, no. 6, pp. 6, January 2012.

[65] Narendra, G. Siva., Chandrakasan and P. Anantha, *Leakage in Nanometer CMOS Technologies*, New York, USA: Springer, 2006.

[66] A. Chandrakasan, S. Sheng and R. Brodersen, "Low-Power CMOS Digital Design," *IEEE Journal on Solid-State Circuits,* vol. 27, no. 4, pp. 473 - 484, April 1992.

[67] A. Wiltgen, K. Escobar, A. Reis and R. Ribas, "Power Consumption Analysis in Static CMOS Gates," *26th Symposium on Integrated Circuits and Systems Design (SBCCI).* Curitiba, 2-6 September 2013.

[68] B. J. Van Zeghbroeck, "Principles of Semiconductore Devices," 2011. [Online]. Available: http://ecee.colorado.edu/~bart/book/. [Accessed 10 December 2015].

[69] L. Akers and J. Sanchez, "Threshold Voltage Models of Short, Narrow, and Small Geometry MOSFET's: A review," *Solid-State Electronics,* vol. 25, no. 7, pp. 621-

641, July1982.

[70] J. Liou, A. Ortiz-Conde and F. Sanchez, "Extraction of the Threshold Voltage of MOSFETs: an overview," *Proceedings of the 1997 IEEE Conference on Electron Devices.* Hong Kong, 30 August 1997.

[71] T. Devoivre *et al.*, "Validated 90nm CMOS Technology Platform with Low-k Copper Interconnects for Advanced System-on-Chip (SoC)," *Proceedings of the 2002 IEEE International Workshop on Memory Technology, Design and Testing. (MTDT 2002).* France, 2002.

[72] E. N. Shauly, "CMOS Leakage and Power Reduction in Transistors and Circuits: Process and Layout Considerations," *Journal of Low Power Electronics and Applications ,* vol. 2, no. 1, pp. 1-29, January 2012 .

[73] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, UK: John Wiley & Sons, November 2011.

Vita

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