DESIGN OF A POWER AMPLIFICATION SYSTEM

FOR S-BAND SATELLITE APPLICATIONS

by

Ahmad Ibrahim R. Dalbah

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Declaration of Authorship

I declare that this thesis is my own work and, to the best of my knowledge and belief, it does not contain material published or written by a third party, except where permission has been obtained and/or appropriately cited through full and accurate referencing.

Signed Ahmad Ibrahim R. Dalbah

Date: July 20, 2021

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We, the undersigned, approve the Master's Thesis of Ahmad Ibrahim R. Dalbah

Thesis Title: Design of a Power Amplification System for S-Band Satellite Applications

Date of Defense: 11/07/2021

Name, Title and Affiliation	**Signature**
Dr. Oualid Hammi Professor, Department of Electrical Engineering Thesis Advisor	
Dr. Nasser Qaddoumi Professor, Department of Electrical Engineering Thesis Committee Member	
Dr. Assim Sagahyroon Professor, Department of Computer Science and Engineering Thesis Committee Member	
Dr. Nasser Qaddoumi Head Department of Electrical Engineering	
Dr. Lotfi Romdhane Associate Dean for Graduate Affairs and Research College of Engineering	
Dr. Sameer Al-Asheh Interim Dean College of Engineering	
Dr. Mohamed El-Tarhuni Vice Provost of Research and Graduate Studies Office of Graduate Studies	

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Abstract

The satellite industry is in more demand than ever for more efficient satellites as they are getting smaller, and with it, the on-board power resources are also getting more limited. The high-power amplification section of the satellite consumes most of the power supplied to the system and is usually the least efficient subsystem of the satellite. Therefore, more efficient power amplification systems are vital for the upcoming small-satellites applications. To address this issue, a high-efficiency power amplification system with acceptable linearity performance is proposed. This system is designed to work in the S-band, specifically around the 3.5 GHz center frequency, with a targeted high efficiency in the range of 60% to 70% at a 6 dB output power backoff. The system is composed of two high efficiency amplifiers operating in the Doherty configuration which results in the high back-off efficiency. Simulations of the system were carried out using Advanced Design System (ADS) software with a large signal model of CGH40010F from Cree-Wolfspeed, which resulted in 62% to 75% of Power Added Efficiency (PAE) at peak output power of 43 dBm. The amplifier's layout was then generated and tuned. The prototyped amplifier achieved an efficiency of 35% at 6 dB back-off and a maximum efficiency of 52% at peak power. It also meets out-of-band spectrum emission requirements for a satellite transmitter. Finally, the amplifier was linearized using digital predistortion (DPD) to ensure meeting the requirements of high order modulation schemes.

Keywords: Radio frequency; Power amplifiers; Digital predistortion; Doherty power amplifier; S-band; satellite.

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Chapter 1. Introduction

Satellite communications have drastically changed the way people live their lives. The menial communications evolved from a simple face-to-face conversations and mail to the invention of the telegraph and telephones, and that in turn evolved in cellular telephones that can perform incredible achievements that were unthinkable of a century ago, and satellites play an important role in this evolution. From high-speed internet connectivity, to the broadcasting of hundreds of TV channels worldwide, satellites have become an essential part of the modern civilization that is indispensable. Even with the evolution of fiber optic cables and ocean links, satellites are still used as a more convenient and reliable way of relaying information and broadcasting [1].

The simplest and first form of satellites is what is known as the geostationary (GEO) satellite system. The first satellite to be launched by the Soviet Union, the Sputnik, and the subsequent satellites that provided telephone links such as the Early Bird were all geostationary. In fact, this was made possible by the development of powerful launch vehicles in the 60's that enabled the positioning of a 500 Kg satellite with a capacity of 500 telephone circuits, which marked the first hint at worldwide telecommunications that is essential for today's civilization. In fact, by the year of 2016, 1459 active satellites were in orbit, and over 500 of them were geostationary serving almost every part of the Earth [1]. In addition to GEO satellites, low earth orbit (LEO) satellites are popular. LEO satellites can be used for earth imaging and low-delay data transfer and telecommunications. However, they have more complicated handoff procedures due to them not being stationary relative to the earth like GEO satellites. The distribution of satellite applications is comprised of 49% of all satellites serving as communications means, with majority of them being digital TV broadcasting (DBS-TV) applications [1]. The main reason for the popularity of services such as satellite DBS in the fiber optics era is cost. To illustrate this, a satellite can broadcast simultaneously to millions of receivers in large areas that require an earth terminal, which is comprised of a dish antenna, and a low noise block (LNB) unit. On the other hand, fiber optics broadcasting would require laying the cable to every receiver which is unrealistic in some places. Therefore, the cost of satellite broadcasting is usually lower than alternative broadcasting methods.

1.1. Motivation

Satellites have come a long way from their early days. Indeed, the first satellite INTELSAT I (formerly Early Bird) used 25 MHz of bandwidth at 6 GHz and 4 GHz (C-band). However, it quickly became apparent that more bands and better electronics are needed to expand onto more services and capacity, leading to Ku-band (14/11 GHz), and then Ka-band (30/20 GHz) motivated by the expansion of digital traffic.

Further complications are present in the dimensions of modern satellites. Indeed, small satellites have become commonplace, such as CubeSats. CubeSats are 0.1 meter cubes with a maximum weight of 1 Kg as indicated by the 1U form. This rush to smaller satellites adds to the complications of transceivers design, especially in the form of power amplifier (PA) as they consume the most power. Therefore, PA efficiency is very important when dealing with the limited supply of power in CubeSats [1] [2]. This thesis is mainly focused on the design and analysis of the power amplification system of a CubeSat system operating in the S-band which falls in the 2 GHz to 4 GHz range.

One of the main challenges in the design of a PA for satellite applications is the choice between Travelling Wave Tube Amplifiers (TWTA) or Solid-State Power Amplifier (SSPA). However, the recent advances of transistor technology, especially Gallium Nitride (GaN) technology have made SSPA more attractive for small-sized missions, especially for the low-power and small-size satellites such as CubeSats [2]. Another challenge in the design of a PA is that memory effects are more pronounced in SSPAs than TWTAs. Therefore, proper linearization techniques have to be developed and applied to the specific application at hand to compensate for gain and phase impairments. Although SSPA and GaN technologies are mature, they are still not very popular for satellite applications, which presents a motivation and a challenge that will be tackled in this thesis.

1.2. Problem Statement

The design of a power amplification system for S-band satellites is the main problem that this thesis tackles. The proposed work involves the design of a high efficiency single-ended amplifier for S-band satellite applications, specifically at 3.5 GHz. Furthermore, a Doherty PA system was implemented based on the designed single-ended PA, with the aim of increasing the back-off efficiency, while meeting the linearity as recommended by the ITU for satellite applications in the S-band and 3GPP

standard for specific modulation schemes, and output power requirements. Specifically, the amplifier is expected to output 20W of power while meeting the linearity requirements and having a drain efficiency of 60 % to 70%.

This work expands and improves on a previous work [3] by considering the design for satellite applications and proposal of enhancement to the architecture by constant uneven power drive and adaptive power drive techniques and simulating the proposed enhancements. The work also aims to verify the operation of the hybrid look-up table model as a linearizer for the designed amplifier and benchmark its performances against that of established models.

Chapter 2. Literature Review

2.1. Power Amplifier Classes

Power amplifiers fall under different classes depending on their operation where different classes correspond to different efficiency and linearity parameters. Efficiency in this discussion is defined in equation (**1**).

$$\boldsymbol{\eta = P_{OUT}/P_{DC}} \quad (1)$$

Where P_{OUT} is the RF power delivered to the load, P_{DC} is the power delivered from the DC supply. Power Added Efficiency (PAE) is defined in equation (**2**).

$$\boldsymbol{PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}}} \quad (2)$$

Where P_{IN} is the RF power delivered to the system's input.

2.1.1. Class A power amplifiers. It is conventional to assume any linear amplifier is operating in class A. However, it is not always true that every class A amplifier is linear, nor any other class is nonlinear. Indeed, the careful choice of bias point and beforehand knowledge of the input signal's characteristics is critical for class A operation, as will be discussed.

Figure 2.1 shows the bias conditions for class A operation. The gate bias is such that the quiescent current is in the middle of its allowable rage. When the input signal is applied to the gate of the transistor, it can have a full swing from $V_{G,\,BIAS} - V_{MIN}$ to $V_{G,\,BIAS} + V_{MAX}$ where all voltages are normalized by the saturation voltage such that 1 corresponds to the maximum voltage, and 0 to the minimum (cut-off) voltage. Therefore, class A operation leads to linear operation with a conduction angle of 2π.

2.1.2. Class AB and class B power amplifiers. Although class A amplifiers benefit from linear operation that satisfies the strictest linearity requirements, they are usually avoided due to their low efficiency. Indeed, the bias point being such that the DC voltage at the drain is half the maximum voltage (voltage at which current saturation is achieved) to allow for the maximum voltage swing (maximum conduction angle of 2π) comes with a constant current consumption, that is, if no signal is present at the input, the DC current consumed is $I_{D,MAX}/2$, which is significant, and causes the

efficiency of class A amplifiers to not exceed 50%. Therefore, it would follow that reducing the conduction angle by reducing the bias point, and therefore reducing DC power consumption, would improve efficiency [4].

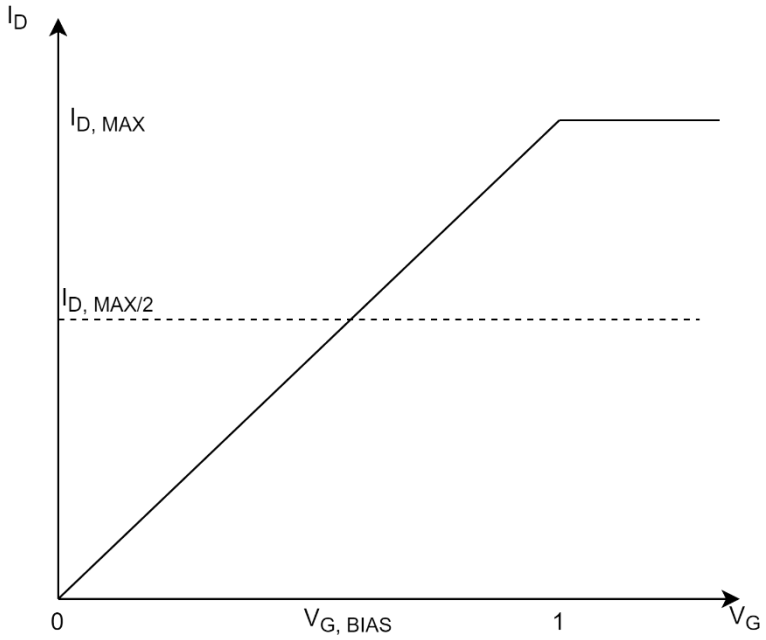

Figure 2.1: Class A operation

Class B and class AB amplifiers are simple solutions to the efficiency problem, without too much trade-off in linearity. In fact, class AB amplifiers are the most widely used in literature and industry for audio and RF applications due to their excellent performance, and they make the basis for more advanced classes.

The bias point for class AB drain current is between 0 and 0.5 (conduction angle of π to 2π), where 0.5 being the class A case and 0 being the class B case. A typical mid class AB bias point would be around 0.3 which results in theoretical peak efficiency of 68% [4].

The reduced conduction angle creates a clipped current output, which translates to added distortion which can be calculated analytically using the Fourier series expansion method. However, it is more common to either simulate the output in software or test it with real components. The distortions of class AB, although still high, are a compromise between distortion-less class A and the distortion-ridden class B.

Class B bias point is at 0 drain current which results in significant distortions. However, this distorted operation results in a maximum theoretical efficiency of 78.5% which is desirable in many applications where power is limited, such as handsets [4].

2.1.3. Class C power amplifiers. In general, class C amplifiers are biased to be anywhere below cutoff. This translates to a conduction angle of less than a π, which means that the signal has to exceed a certain positive value before the transistor starts conducting.

Consider a typical class C bias point of -0.6. The efficiency achieved is 87%. It is worth noting that it is difficult to obtain a class C operation due to the very nature of the bias point causing the signal to be very well in the reverse region of the transistor. Moreover, depending on the physical parameters of the transistor, namely the breakdown voltage, it can cause permanent damage to the system. Furthermore, even if the transistor has an excellent breakdown voltage, another concern is the leakage current, which can lower the efficiency considerably [4]. Fortunately, recent advances in the GaN-based transistors having much higher breakdown voltages, have improved the operations in high efficiency classes such as class C [5].

2.2. Power Amplifier Systems

The main goal of different power amplifier systems is to maintain high efficiency at a practical power range. In traditional amplifier classes discussed previously, efficiency reported is a peak efficiency usually at the saturation power of the transistor. However, most modern signals have an amplitude modulation component, which introduces a dynamic range requirement for the amplifier. What this translates into in terms of efficiency, is that despite having a peak efficiency at the peak power, typically very low efficiency is obtained at the average power of the input signal. Therefore, different power amplifier architectures were reported in the literature in order to solve this issue.

2.2.1. Envelope tracking power amplifiers. Envelope tracking systems make use of the fact that varying the drain supply of the transistor will change its power characteristics, mainly saturation point. Therefore, it would follow that having a modulated drain voltage that tracks the envelope of the input signal would maintain high efficiency at an extended dynamic range. The block diagram of a basic envelope

tracking system is shown in Figure 2.2. The RF input is coupled, and its envelope sent to the supply modulator, which will modulate the DC bias of the RF amplifier. A delay line is added to compensate for the delay of the supply modulation part. Generally, the input signal's envelope is not directly input into the bias, but rather it goes through a shaping function that will result in the desired drain voltage to be applied to the amplifier in order to reduce its power consumption. In fact, envelope shaping functions mitigate some issues in this approach, for example, when the drain supply voltage is less than the knee voltage of the transistor, the nonlinear characteristics of the PA will be very strong. To solve this issue, shaping functions usually have a minimum value of just above this knee voltage or pinch-off voltage value to ensure never dipping below the knee voltage [6].

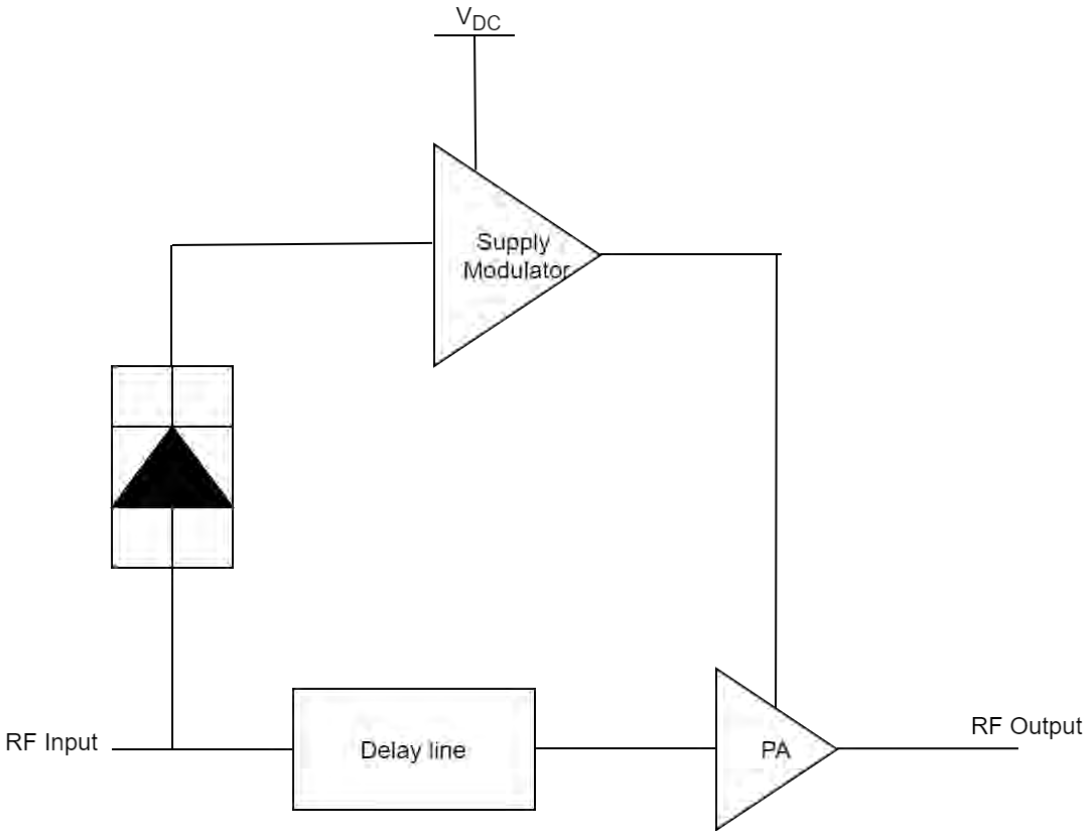

Figure 2.2: Envelope tracking block diagram [6]

In Figure 2.3, different shaping functions are depicted. The no shaping case is when the envelope is followed faithfully without alterations, but this results in, as discussed previously, poor linearity. Furthermore, shaping function #1 simply clips the

voltage below the knee, and then follows the no shaping case. However, this abrupt break causes bandwidth requirements' increase on the supply modulator, and it does not produce good linearity. Moving on to shaping function #2, it introduces an offset to shift the curve above the knee voltage, which does not increase bandwidth requirements. This approach produces very good linearity, and a minor dip in efficiency compared to function #1. Shaping function #3 is a mix of the first two, but optimized for efficiency, and therefore is a compromise between the linearity and efficiency.

2.2.2. Doherty power amplifiers. The Doherty power amplifier is capable of delivering the most strict requirements for satellite and base stations in terms of efficiency. Indeed, Doherty power amplifiers are the industry standard for base stations because of their mature technology and high reliability. Furthermore, its design is not riddled with restrictions as the envelop tracking, and Doherty systems are more suitable for high dynamic range signals [7]- [13].

The overall design of the Doherty amplifier is shown in Figure 2.4. The input signal is split evenly between the carrier and peaking amplifiers through a hybrid coupler, which provides a 90 degrees phase shift in signal being fed to the peaking amplifier. Then, the output signals of the two amplifiers are combined through a quarter wavelength impedance transformer, which in the typical case of 50 Ω systems, transforms the 25 Ω to 100 Ω in the low power region, and doesn't have any effect over the 50 Ω shown to the carrier amplifier in the high-power region. This behavior is known as load modulation. The 35 Ω line transforms the 25 Ω impedance at the summing branch of the two amplifiers to 50 Ω.

The Doherty design relies heavily on the concept of load modulation, which is the modulation or change of load impedance in conjunction with the change of input power. Consider Figure 2.5, where the impedance of the voltage-controlled voltage source is modulated by the current source by equation (**3**).

$$\boldsymbol{Z_1 = V_1/I_1 = V_1/(I_R - I_2)} \qquad (3)$$

Varying the current I_2 from zero to $I_2 = V_1/R$ will modulate impedance from R to ∞. This is an important result, as it will allow us to modulate the load impedance to track the optimum performance of the amplifier [7].

This translates to the operational diagram of the Doherty amplifier seen in

Figure 2.6. An amplifier can be visualized as a current source, and usually, two amplifiers are used in the Doherty system, a carrier amplifier, and a peaking amplifier.

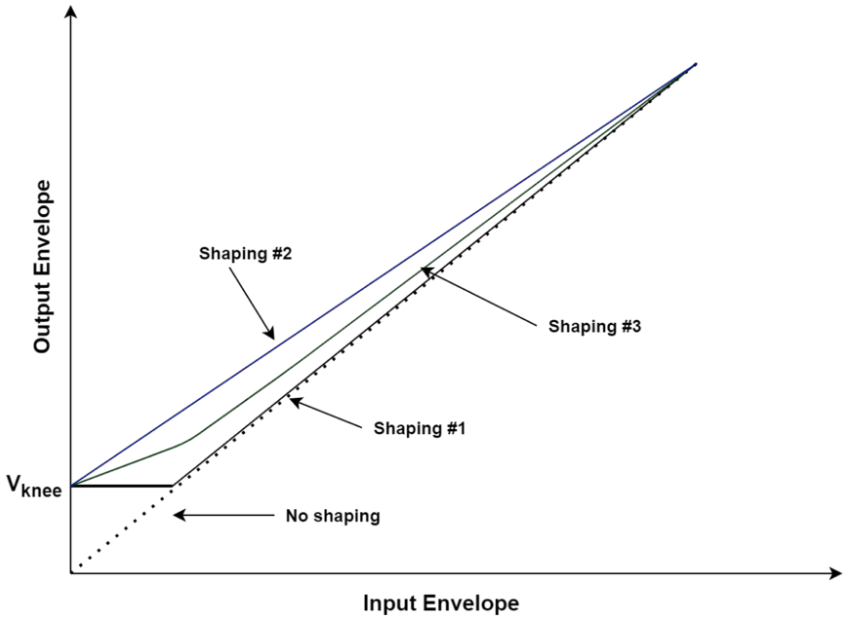

Figure 2.3: Sample shaping functions used envelope tracking [6]

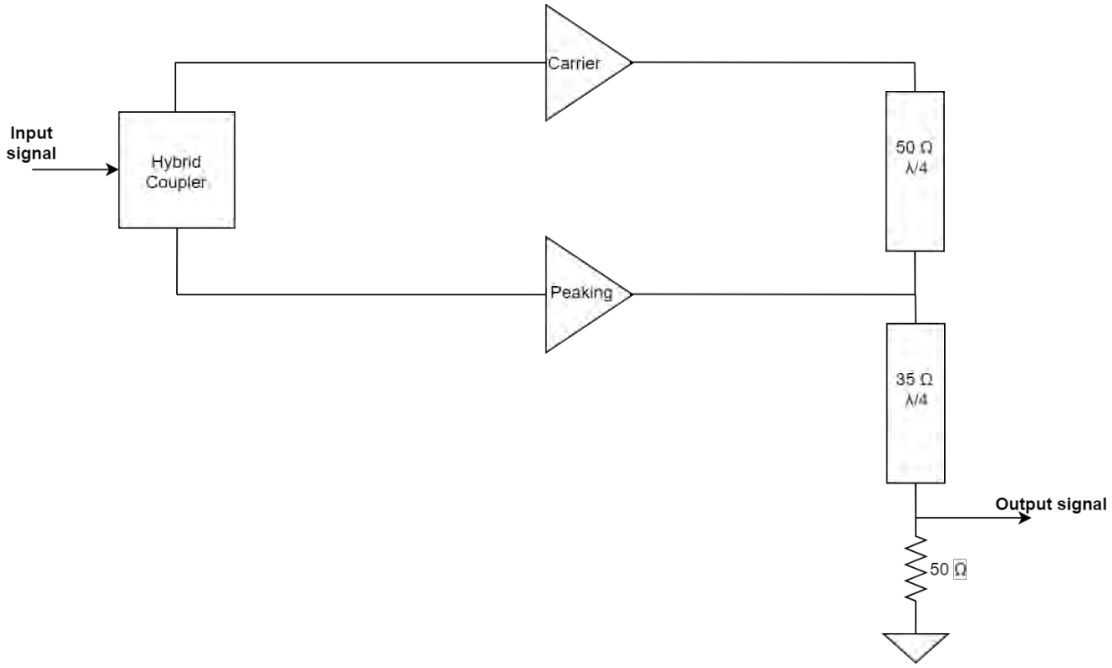

Figure 2.4: Generic block diagram of the Doherty amplifier

The carrier amplifier is connected to the load through a quarter-wavelength transmission line. The impedance seen by the carrier amplifier can be found as reported in (**4**) and (**5**).

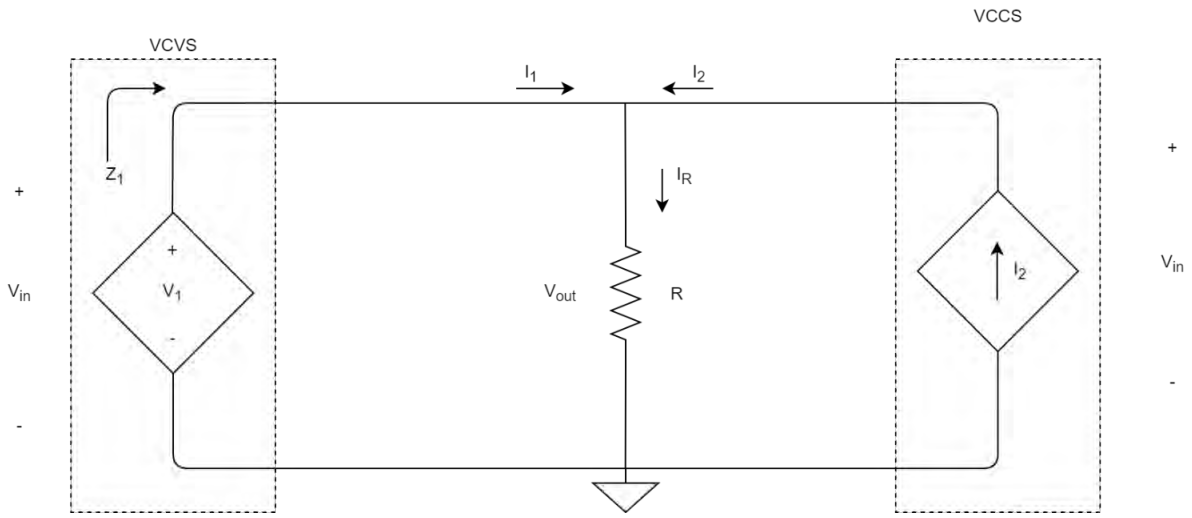

Figure 2.5: Load modulation circuit [7]

$$\boldsymbol{Z_1' = V_0/I_1 = (R_0/2) \cdot [(I_1' + I_2)/I_1']} \qquad (4)$$

$$\boldsymbol{Z_1 = R_0^2/Z_1' = 2R_0/(1+\alpha)} \qquad (5)$$

Where α is I_2/I_1' .

This effectively makes $Z_1 = 2R_0$ when the peaking amplifier is off ($I_2 = 0$), and $Z_1 = R_0$ when $I_2 = I_1 = I_{MAX}$. It is worth noting that usually both amplifiers are designed to handle the same power to satisfy this condition. At the same time, the impedance seen by the peaking amplifier is shown in equation (**6**).

$$\begin{aligned} \boldsymbol{Z_2 = V_0/I_2} &= \boldsymbol{(R_0/2) \cdot [(I_0' + I_2)/I_2]} \\ &= \boldsymbol{(R_0/2) \cdot [(1+\alpha)/\alpha]} \end{aligned} \qquad (6)$$

The load modulation profile for both the peaking and carrier amplifiers can be seen in Figure 2.7.

The goal of this load modulation, and the use of two amplifiers is to enhance the back-off efficiency. Typical amplifiers of any of the conventional classes discussed

previously have a peak efficiency at the maximum voltage and current swings which is specified by the power delivered to a certain load. However, the load modulation of the Doherty system allows for the existence of two peak efficiencies, specifically, the carrier amplifier achieves its peak efficiency typically at half of the output power, while the peaking amplifier achieves its peak efficiency at the maximum output power. This effect is shown in Figure 2.8. In theory, this allows for designing amplifiers with high efficiency at the average operating power, while simultaneously achieving high efficiency at the occasional low probability peak power, effectively satisfying the linearity and efficiency required out of most industrial systems.

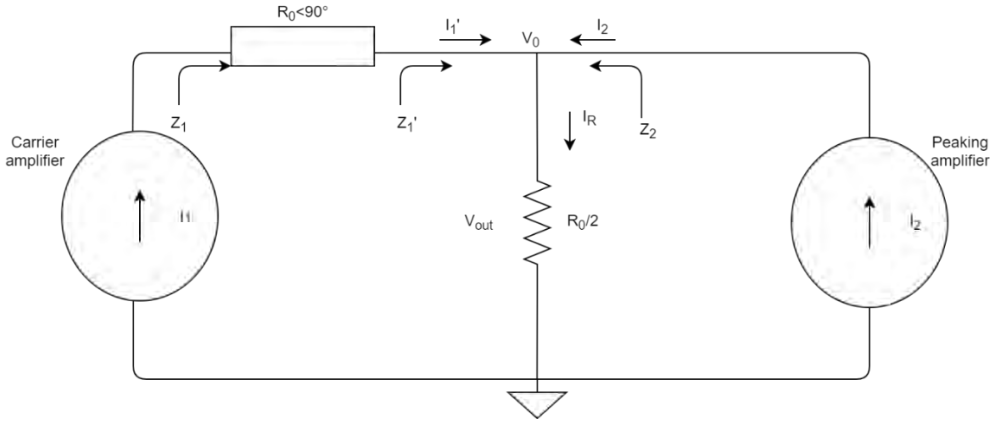

Figure 2.6: Operational diagram of the Doherty amplifier [7]

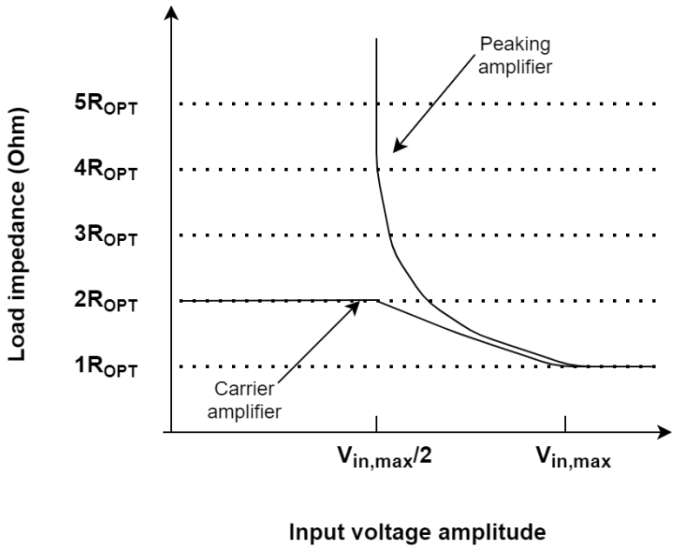

Figure 2.7: Load modulation curves [7]

The first step to be considered when designing a Doherty power amplifier is the bias point of the two amplifiers, the carrier and peaking amplifiers. From the previous section, the Doherty PA requires a certain current profile shown in equations (**7**) and (**8**).

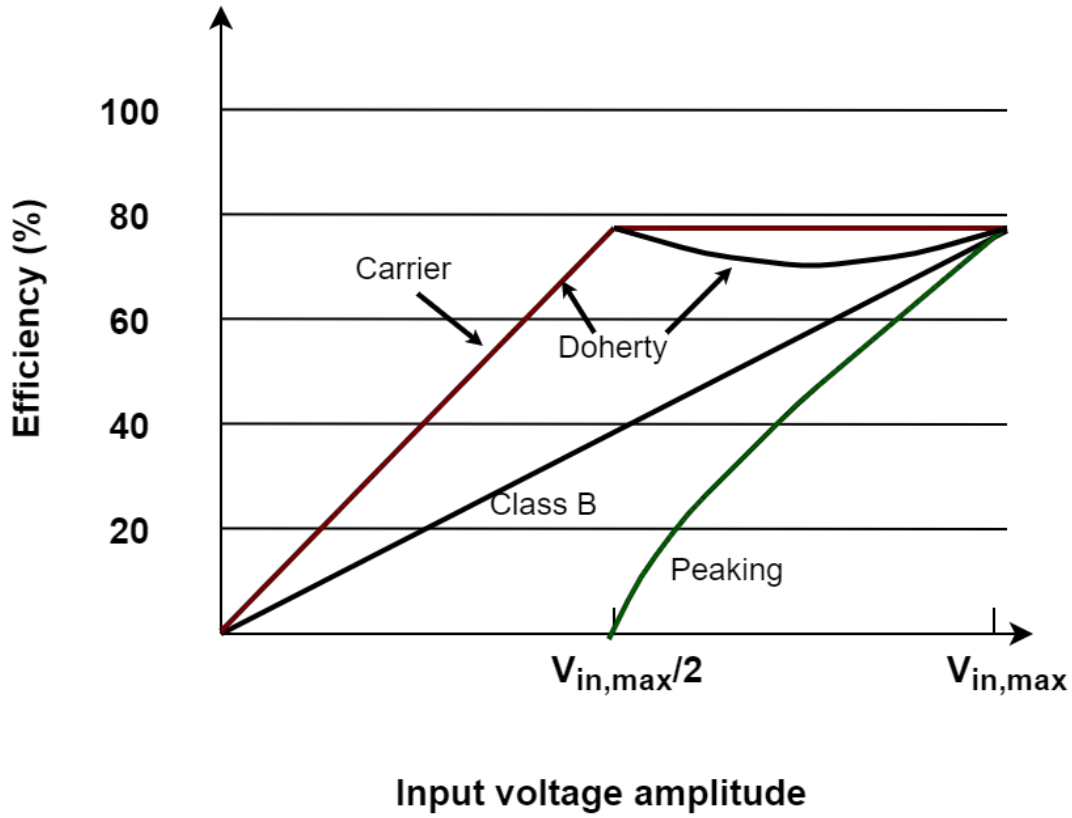

Figure 2.8: Theoretical efficiency curves of a Doherty amplifier [7]

$$I_C = I_{MAX}\left[\frac{V_{IN}}{V_{IN,MAX}}\right], 0 < V_{IN} < V_{IN,MAX} \quad (7)$$

$$I_p = \begin{cases} 0\,, \;\; 0 < V_{IN} < V_{IN,MAX}/2 \\ I_{MAX}\left[\dfrac{V_{IN} - V_{IN,MAX}/2}{V_{IN,MAX}/2}\right], V_{IN,MAX}/2 < V_{IN} < V_{IN,MAX} \end{cases} \quad (8)$$

As shown from equation (7), the carrier amplifier profile can be achieved using a class-B amplifier with a linear current profile. However, the peaking amplifier is the design

challenge faced in this case. In order to satisfy the equation (8), the amplifier must start conducting at exactly $V_{IN,MAX}/2$, and then reach the same current level of the carrier amplifier at saturation, which is a shortcoming in class-C amplifiers, as the lower bias point results in a lower power gain, and lower current that won't match the carrier amplifier's current level. Furthermore, the amplifier will not turn on abruptly as desired from the equation, but rather would follow a soft turn-on profile as shown in Figure 2.9. To alleviate the issue of soft turn-on, the biasing of the peaking amplifier can be adjusted to turn on before the back-off power threshold, leading to efficiency degradation. In fact, the earlier the peaking amplifier is turned on, the more the amplifier becomes a balanced two-way amplifier instead of a Doherty power amplifier, with no efficiency enhancement at the back-off. Therefore, the biasing of the peaking amplifier has to be selected carefully to ensure a good compromise between linearity and efficiency.

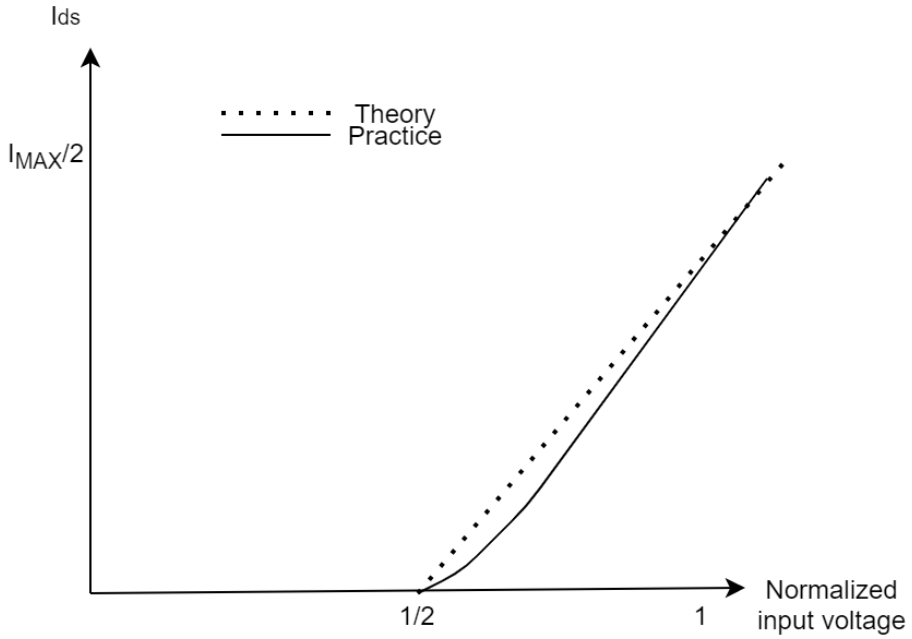

Figure 2.9: Soft-turn on of class-C amplifier

2.2.3. Enhancements to the basic Doherty amplifier. Doherty amplifiers are very popular in the literature due to their performance characteristics, namely their relatively large output power range that can sustain high efficiency compared to traditional

amplifiers, that are suitable for modern communication systems. However, there are different techniques and architectures in the literature that can improve on the theory of the Doherty amplifier.

Before discussing specific enhancements, a common practical design consideration is the inclusion of phase-offset lines at the output of carrier and peaking amplifiers. Although Doherty operation may seem simple, it requires further fine-tuning at every stage. Indeed, offset lines are often required at the output of each amplifier as shown in Figure 2.10. The need for these offset lines comes from the nonidealities of the amplifiers and the difference between the carrier amplifier and peaking amplifier paths that have to be compensated for, such as the phase difference in their outputs. This technique offers an easy way to correct the overall design while simultaneously allowing the use of the same matching network in both amplifiers. Without the phase offset lines, the load modulation behavior is not guaranteed to follow the desired path, especially for the peaking amplifier as it needs to present open circuit in the low power range. The peaking offset lines is tuned to guarantee this behavior is observed.

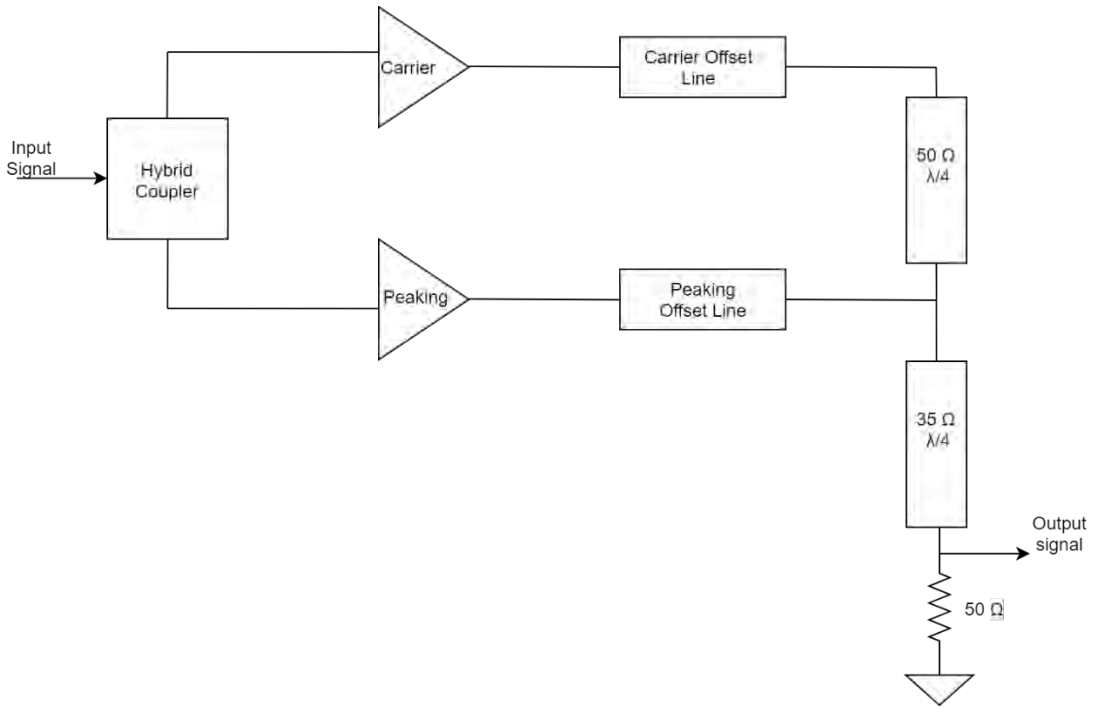

Figure 2.10: Doherty amplifier schematic using offset lines [7]

Another practical consideration is the load value to be shown to the carrier amplifier. Although the traditional Doherty power amplifier should have two peaks of efficiency (one at 6 dB back-off, and one at saturation), the reality of it is different. In order to obtain such results, perfect load modulation conditions have to be met, where the maximum power of the carrier amplifier is delivered at the first saturation of the carrier amplifier which occurs at half the input power of the Doherty amplifier as shown in Figure 2.11 a). In this figure, R_{OPT} refers to the optimal load resistance seen by the carrier amplifier's internal current source in the high-power region and $2R_{OPT}$ refers to the value of the same at the low-power region. Ideally, the carrier amplifier should be saturated at the two impedances due to the load modulation and have ideal efficiency peak at 6-dB back-off power. However, this is made difficult by the knee effect of the transistors which results in a region where the transistor will not conduct as illustrated in Figure 2.11 b). One solution to this is by modulating the carrier amplifier with a larger load than $2R_{OPT}$, therefore reducing the knee voltage effect by making sure the carrier amplifier saturates exactly at the desired back-off power as depicted in Figure 2.11 b) where the current is reduced and voltage is increased to make sure the power at such impedance is exactly the same as the ideal case. What this means in practice is that the first peak efficiency of the Doherty PA can be tuned to different power levels and back-off ranges depending on the need of the application at hand.

2.2.3.1 Uneven drive through a coupler. In order to address the issue of class-C typical current output being lower than desired, the uneven drive of the two amplifiers can be adopted. The traditional Doherty power amplifier requires a coupler to divide the input power equally between the carrier and the peaking amplifiers. However, a technique to overcome the low current issue in the peaking amplifier is simply to supply it with more power, or use an asymmetrical architecture for the Doherty PA with a bigger peaking amplifier to compensate for the lower current output due to class-C biasing. Since using two different transistors is more complex and undesirable in many cases, directing more power to the peaking amplifier than to the carrier amplifier is implemented when needed. This is known as the uneven drive, and an example schematic of it is shown in Figure 2.12. The side effect of this technique is reducing the overall gain of the amplifier since less power is supplied to the carrier amplifier. This in effect leads to a more linear amplifier at the cost of less efficiency at back-off due to the loss of the extra power supplied to the peaking amplifier that will not turn on until

the power input exceeds specified turn-on requirement for the class-C peaking amplifier [12] [14].

2.2.3.2 Adaptive gate bias voltage. Another way of synthesizing the exact desired current profile of the peaking amplifier is to adjust the gate voltage adaptively depending on the envelope of the input signal. This is usually implemented by sampling the RF input into an envelope shaping circuit which will determine the gate voltage of the peaking amplifier at any given time.

For example, to force the peaking amplifier to be off in the lower power region, the gate voltage would be set very deep in class-C. On the other hand, at peak power, the peaking amplifier's gate voltage would be set at the same gate voltage as the carrier amplifier to obtain higher gain and correct load modulation behavior. An implementation of this method is shown in Figure 2.13.

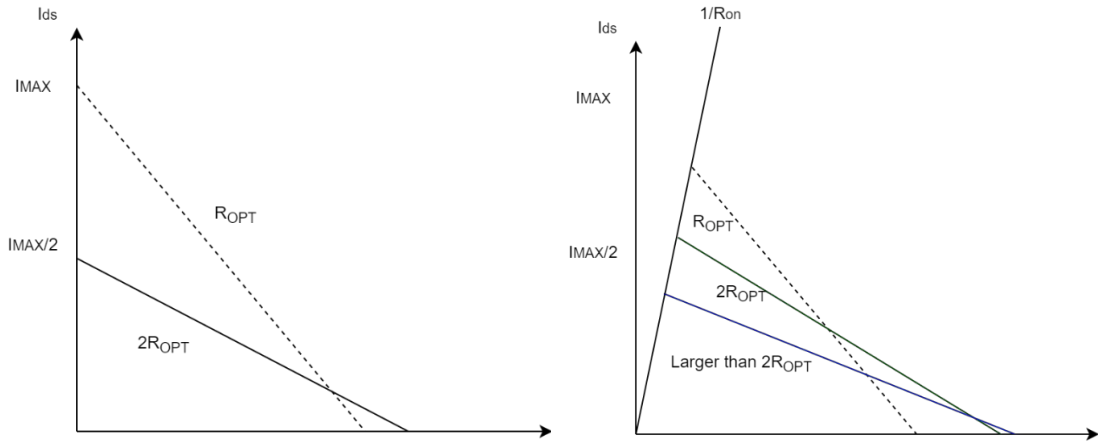

Figure 2.11: Load modulation in Doherty amplifiers. a) Ideal case with zero knee voltage b) practical case with knee voltage [7]

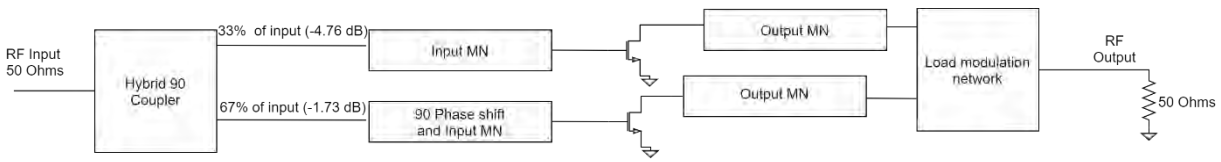

Figure 2.12: Schematic of a Doherty amplifier using uneven power drive

This method effectively eliminates the issue of soft turn-on of the peaking amplifier shown previously in Figure 2.9. However, the downsides to this method are the additional circuit elements and design complexity [12].

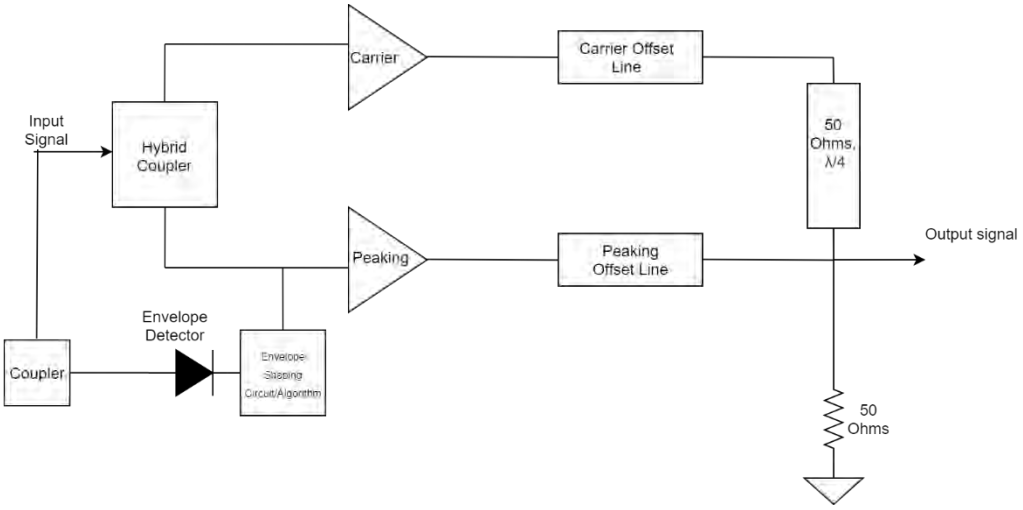

Figure 2.13: Schematic of a Doherty amplifier using adaptive gate bias

2.2.3.3 Adaptive uneven drive. Although the uneven drive architecture is simple to design and alleviates the issue of the peaking amplifier's lower current, it does that at the cost of wasting power in the low-power region. An alternative to adaptive gate voltage and simple uneven drive is a power-dependent input power distribution tailored to the specific PA at hand, where the carrier amplifier is driven more in the low-power region to maximize power transfer and increase efficiency, and the peaking amplifier is driven more in the high-power region to maximize efficiency and compensate for lower current of the class-C peaking amplifier [15] [16]. An example design for such an adaptive power split is shown in Figure 2.14, where the ratio shown is $P_{carrier}/P_{peaking}$.

2.2.3.4 Bandwidth enhancement architecture. The traditional Doherty power amplifier requires the load modulation conditions to be met for optimal operation. However, these conditions can drift with frequency changes, especially if the open-circuit condition for the peaking amplifier is met through an offset line. This results in efficiency and gain degradation, which can be significant. Therefore, a bandwidth enhancing architecture based on a modified load modulation network was proposed in [3], and is shown in Figure 2.15. Figure 2.15 a) shows the traditional design with the

inverter line transforming 100 Ω shown by the carrier amplifier at back-off to 25 Ω to match the load. However, in the proposed architecture, the impedance shown to the carrier is 50 Ω at back-off, and 25 Ω at peak power which is a lower transformation ratio than the conventional Doherty PA. This results in easier design, lower complexity, and higher theoretical bandwidth as it deviates from the ideal conditions. In practice, this also results in higher average efficiency for wideband modulated signals.

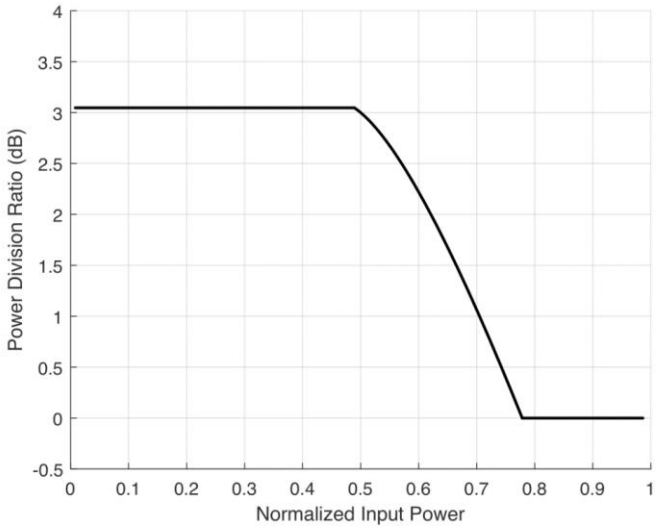

Figure 2.14: Typical adaptive uneven power splitting for enhanced Doherty amplifier performance [15]

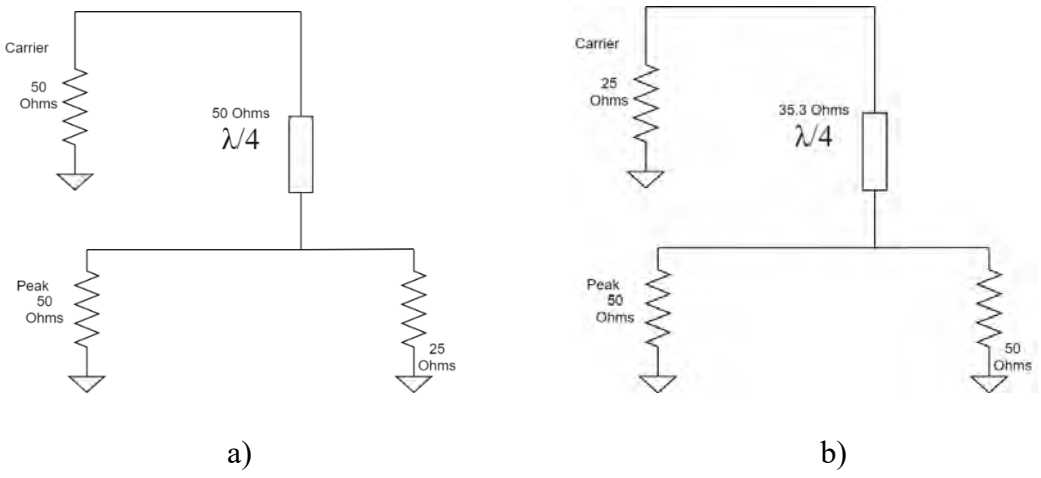

Figure 2.15: Bandwidth enhancement in Doherty amplifiers. a) Traditional Doherty amplifier b) Bandwidth-enhanced Doherty amplifier [3]

2.3. Digital Predistortion (DPD)

In order to obtain a high efficiency linear amplification, most amplifiers are designed with the efficiency requirements, and are later linearized. The goal of a linearizer is to cancel out the undesired frequency components, specifically, the goal often is to reduce carrier to third-intermodulation component ratio (C/IMD3) in multi-tone tests, or Adjacent Channel Leakage Ratio (ACLR) in modulated signals such as Long Term Evolution (LTE). There are many variations to linearizer architectures, but the most well-known ones are feedforward and predistortion. However, feedforward systems are not popular due to their difficulty of implementation as well as their impact on the overall efficiency of the amplification system. The efficiency degradation is mainly due to the need a highly linear amplifier as part of the distortion cancellation loop in the feedforward system.

Digital predistortion is the most popular form of power amplifiers linearization owing to its low complexity and ease of implementation on digital tools and hardware such as field-programmable gate array (FPGA). A predistorter needs to equalize the gain of the amplifier, and therefore, can be thought of as having the expression shown in equation (**9**) in dB.

$$\boldsymbol{G_L(P_{outL}) - G_{L\_SS} = -(G_A(P_{inA}) - G_{A\_SS})} \quad (9)$$

$$\boldsymbol{G_L = x_{out\_DPD}(n) - x_{in\_DPD}(n)} \quad (10)$$

$$\boldsymbol{G_A = x_{out\_PA}(n) - x_{in\_PA}(n)} \quad (11)$$

Where G_L is the DPD gain as defined in (10), G_{L_SS} is the small-signal gain of DPD, G_A is the instantaneous gain of the PA as defined in (11), and G_{A_SS} is the small-signal gain of PA. The small signal gains are used to normalize the gain of DPD and ensure appropriate input power level to the PA [17]. The terms defined in equations (**10**) and (**11**) are visualized in Figure 2.16. Usually, the gain of a device under test (DUT) is characterized by amplitude modulation to amplitude modulation (AM/AM) plot. The AM/AM characteristic is obtained by plotting the magnitude of the instantaneous gain (such as $\boldsymbol{G_A}$ for a DPD) versus the instantaneous input power.

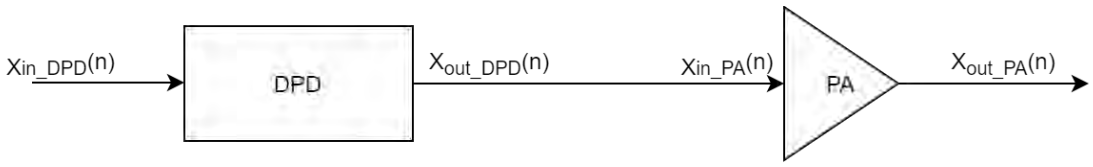

Figure 2.16: Simplified block diagram of a predistortion system

Likewise, the phase distortion of the PA has to be compensated for to ensure a constant phase, equation (**12**) is used for this purpose, in degrees.

$$\boldsymbol{\phi_L(P_{outL}) - \phi_{L\_SS} = -(\phi_A(P_{inA}) - \phi_{A\_SS})} \qquad (12)$$

Where $\boldsymbol{\phi_L}$ is the instantaneous phase shift of the DPD, $\boldsymbol{\phi_{L\_SS}}$ is the small-signal phase shift of the DPD, $\boldsymbol{\phi_A}$ is the PA's instantaneous phase shift and $\boldsymbol{\phi_{A\_SS}}$ is the small-signal phase shift of the PA. Usually, the phase shift of DUT is characterized by amplitude modulation to phase modulation (AM/PM) plot. The AM/PM characteristic is obtained by plotting the phase shift of the instantaneous gain (such as $\boldsymbol{\phi_L}$ for DPD) versus the instantaneous input power.

Graphically, this translates into what is illustrated in Figure 2.17. The PA's characteristics are inverted and then cascaded with the PA to obtain a Linear Power Amplifier (LPA).

Digital predistortion systems implementation vary in shape and form, but any predistortion system that operates at large bandwidth must take into account the memory effects. Memory effects are the dependency of the current sample at the amplifier's output on its current input sample, and on a finite set of previous input samples as well.

2.3.1. Memoryless DPD. The simplest form of DPDs are Look-Up Table (LUT) based DPDs. The goal of a LUT is simply to store the input and output of the DPD in the form of a table, such that, when an input is requested, the LUT determines which cell it falls under and outputs the appropriate DPD gain values. Appropriate interpolation techniques are to be used for values that do not exist in the LUT.

The first variation of LUT models are uniformly indexed LUTs. Typically, AM/AM characteristic is modeled in an LUT and another LUT is made for the AM/PM characteristic. Then, the input's magnitude is quantized and taken as the indexing

element for the LUT as shown in Figure 2.18, and each entry is assumed to be optimal at its bin midrange, with the bin width given in equation (**13**).

$$\boldsymbol{d = (A_{MAX} - A_{MIN})/(N - 1)} \qquad (13)$$

Where A is the discrete quantized signal, and N the number of samples.

However, since the nonlinearity mainly occurs at compression, it was found that indexing the LUT nonuniformly, with most of the cells being packed near compression will lead to better performance than that of the uniform indexing. This calls for the use of a compounding function to distribute the cells appropriately as shown in Figure 2.19.

2.3.2. Memory DPD. Memory DPDs are popular for the improvement in performance they bring when memory effects are present in the amplifier to be linearized. The most popular memory model is the memory polynomial [18] – [21].

The memory polynomial model is obtained by the reduction of unnecessary terms in the Volterra series, specifically by keeping only its diagonal terms. This results in the formulation shown in equation (**14**).

$$\boldsymbol{y_{MP}(n) = \sum_{m=0}^{M} \sum_{k=1}^{K} a_{mk} x(n-m)\,|x(n-m)|^{k-1}} \qquad (14)$$

Where $\boldsymbol{a_{mk}}$ represents the model's coefficients, $\boldsymbol{K}$ is the model's nonlinearity order, and $\boldsymbol{M}$ is the memory depth of the model.

Therefore, the goal is to identify the coefficients a_{mk} which represent the weight of the model at combinations of nonlinearity order and memory depth. The equation can be rewritten as shown in equation (**15**).

$$\boldsymbol{y_{MP}(n) = \varphi_{MP}(n) \cdot A} \qquad (15)$$

Where $\boldsymbol{\varphi_{MP}}$ and $\boldsymbol{A}$ are defined as shown in equation (**17**).

The memory polynomial reported excellent reliability and is often used as a benchmark for other models. However, it still suffers from the difficult extraction process which involves the inversion of the matrices as part of the coefficients identification through the least mean squares (LMS) algorithm. Therefore, many models have been proposed to combat this, and they are often box-oriented models.

The simplest and most popular among these box models are the Hammerstein and Wiener models. They simply work by cascading a linear FIR filter and a memoryless nonlinear model (often an LUT) such as the Wiener model shown in Figure 2.20.

The FIR filter introduces the memory effect into the predistortion system by the basic FIR filter equation (**16**).

$$\boldsymbol{x_W(n) = \sum_{m=0}^{M} a_m \; x_{in}(n-m)} \qquad (16)$$

Where $x_W(n)$ is the filter output, and M is the memory depth of the filter.

The main limitation of the Wiener and Hammerstein models is their inability to model nonlinear memory effects. To address this twin-nonlinear two-box models have been introduced [22]. This model came in three versions as shown in Figure 2.21, where (a) is the forward twin-nonlinear two-box model, in which the LUT is placed before a memory polynomial function. Figure 2.21 (b) is the reverse of that and is called the reverse twin-nonlinear two-box model. Finally, the parallel twin-nonlinear two-box model, the LUT and memory polynomial are parallel to each other.

The basic principle of the Twin-nonlinear two-box models is combining a memoryless model and a low order memory polynomial. The advantage of separating the static nonlinearity and the dynamic nonlinearity is a less complex model by separately controlling the size of the LUT and number of coefficients of the memory polynomial to achieve the desired performance. Furthermore, the identification procedure only adds one extra step, which is de-embedding the data to reach the memory polynomial reference planes and extract the coefficients from there. The de-embedding phase is executed after extracting the LUT from the DUT measured data, which is straightforward LUT mapping. The authors reported that the TNTB model outperforms the conventional memory polynomial with less parameters.

In the case of GaN based amplifiers, it was found that strong memory effects might be exhibited and this can impact the performance of TNTB based predistorters. Hence, an enhanced TNTB model which uses a generalized memory polynomial for implementing the dynamic nonlinear function was proposed in [23].

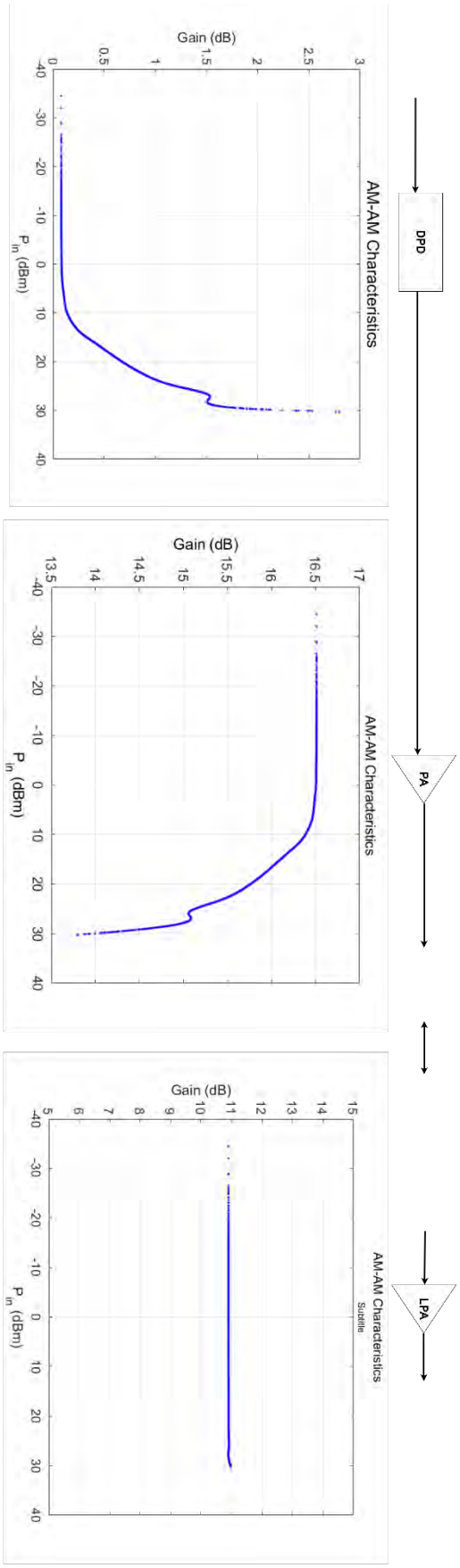

Figure 2.17: Predistortion principle

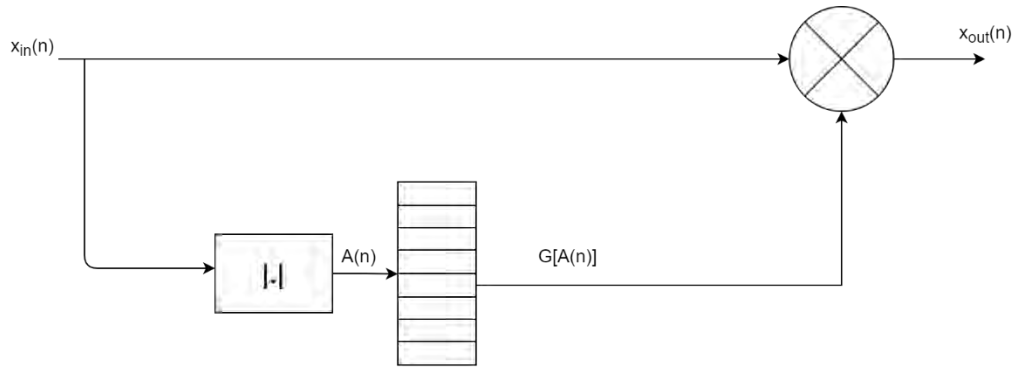

Figure 2.18: Look-up table based DPD system [18]

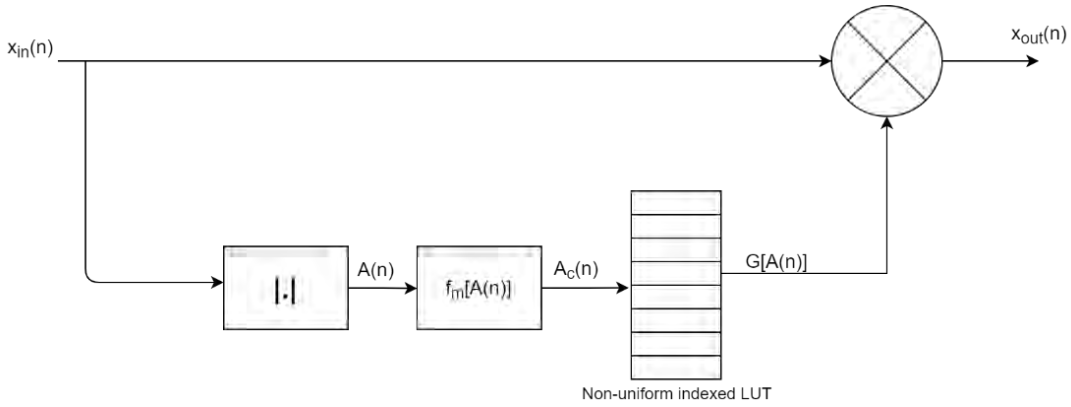

Figure 2.19: Nonuniform LUT DPD system [18]

$$\boldsymbol{\varphi_{MP}(n)} = \begin{bmatrix} \boldsymbol{x(n)} \\ \vdots \\ \boldsymbol{x(n)\cdot|x(n)|^{K-1}} \\ \boldsymbol{x(n-1)} \\ \vdots \\ \boldsymbol{x(n-1)\cdot|x(n-1)|^{K-1}} \\ \vdots \\ \boldsymbol{x(n-m)\cdot|x(n-M)|^{K-1}} \end{bmatrix}^{\boldsymbol{T}} \boldsymbol{, A = [a_{01} \dots a_{0K}\ a_{11}\ \dots\ a_{1K} \dots\ a_{MK}]^T} \quad (17)$$

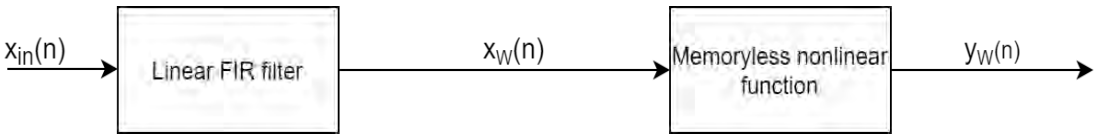

Figure 2.20: Wiener model block diagram

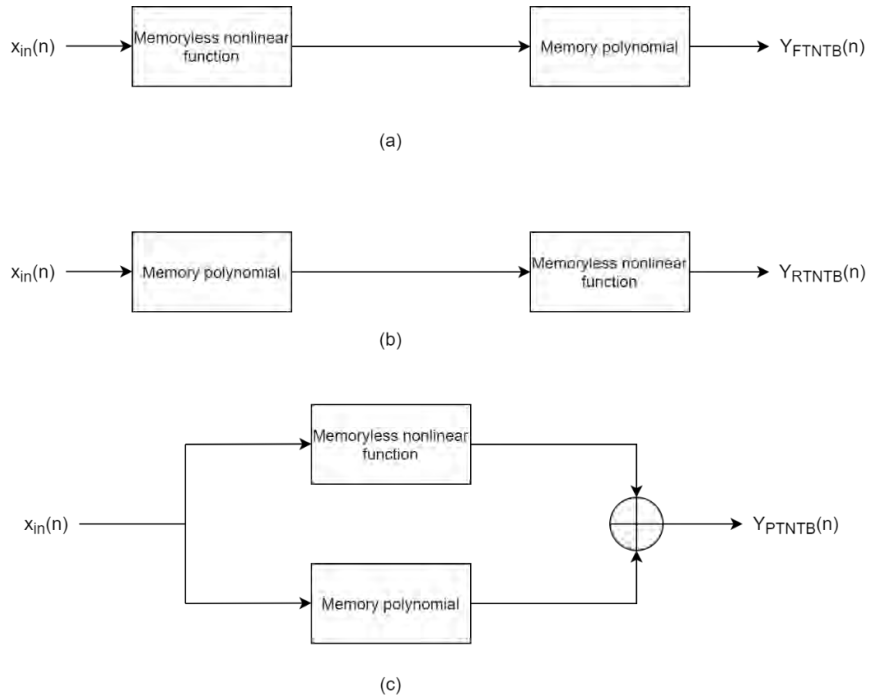

Figure 2.21: Twin-nonlinear Two-box Models a) forward model b) reverse model c) parallel model

Even though models such as the TNTB offer excellent compromise between complexity and performance, some applications can't afford the computational complexity that the memory polynomial and its variants introduce to the system through the identification of their coefficients. Therefore, the Look-up Table (LUT) model was improved on and made into a Nested Look-up Table (NLUT) to introduce memory effects into the basic LUT model [24]. The representation of the nested table model is shown in Figure 2.22, where it is visualized as a 2D table instead of a vector for convenience. The horizontal axis of the table represents the possible power levels of the instantaneous signal |x(n)|, while the vertical axis represents a compound index of the previous samples, in this case, only 2 previous samples were considered (memory depth). The signals are quantized over *K* discreet values. However, the size of the table is huge at $S_{NLUT} = K^{M+1}$, where *M* is the memory depth, which comes to 16,777,216 cells for a typical signal quantized over 256 values and memory depth of 2. In this thesis, the linearization approach will investigate the use of a more compact version of the nested LUT in order to linearize the designed Doherty amplifier.

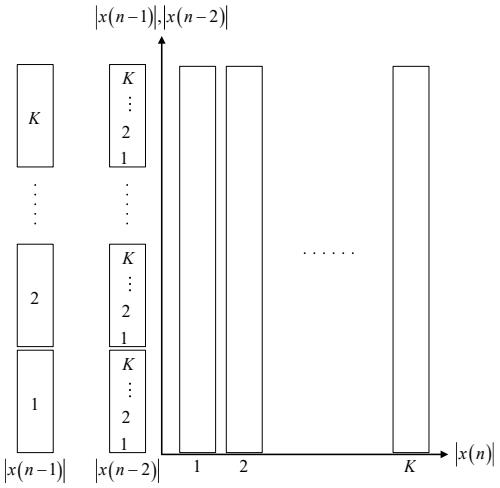

Figure 2.22: 2D representation of the Nested LUT model [24]

2.4. GaN Technology

Gallium Nitride (GaN) has been a popular choice for RF power amplifier designs in the recent years, which is due to its excellent characteristics compared to other technologies. First, GaN as a material, is very hard with very strong atomic bonds that produces a bandgap of 3.4 electron Volt (eV). In comparison to other popular fabrication technologies, gallium arsenide (GaAs) has a bandgap of 1.4 eV and silicon (Si) 1.1 eV only. The significance of bandgap is mainly in its effect on the breakdown voltage. GaN's improved bandgap allows it to endure much higher operating voltages up to five times higher than GaAs. This in effect makes it more suitable for higher efficiency and higher power applications reliably. Furthermore, GaN features high saturation velocity, which allows it to have a higher current density, allowing the use of smaller sized transistors for the same output power as compared to other technologies (ten times higher power density than GaAs). Also, the thermal properties of GaN is an improvement over older technologies, which allows the use of smaller heatsinks for cooling down the operating transistor. Another notable improvement GaN brings is increased bandwidth since it has lower capacitance that affects the frequency response of the transistor [5]. Overall, this makes GaN based transistors very attractive in satellite applications where fluctuations in environment (e.g. temperature) is expected and longevity is desired.

2.5. Literature Review Summary

Power amplifiers fall in different classes depending on their operation point. Class A amplifiers are very linear when carefully designed and can satisfy the most strict of linearity requirements. However, they are inefficient compared to other classes, having a maximum theoretical efficiency of 50%. Class B amplifiers sacrifice some linearity to improve efficiency, with a maximum theoretical efficiency of 78.5%, while class AB amplifiers are the compromise between class A and class B, enjoying both high linearity and high efficiency with a typical class AB amplifier having a theoretical efficiency of 68%. In fact, class AB are the most widely used in the industry for audio and RF applications. Finally, class C amplifiers are biased below the cutoff of the transistor, which introduces nonlinearities to the output signal, making class C amplifiers typically nonlinear, but a typical class C amplifier enjoys a theoretical efficiency of 87%.

Power amplifier systems are used to maintain high efficiency over a practical power range, since the typical amplifier classes efficiencies reported previously are only for peak efficiencies when the amplifier is saturated. To solve this issue, power amplifier systems are used in the industry and the literature. Envelope tracking power amplifiers shape the DC bias of the transistor according to the input signal's envelope to maximize the efficiency over the largest power range possible. Doherty power amplifiers on the other hand, use two amplifiers with the input signal split between them, then the output signal is combined through a load modulation network. Doherty systems are often designed with a class AB as the main or carrier amplifier, and a class C amplifier as the peaking or auxiliary amplifier. Therefore, Doherty systems often enjoy high linearity of class AB and the high efficiency of class C. Furthermore, the Doherty systems are the most widely used in the industry for base stations due to their advantages. To improve on the basic Doherty system design, offset lines are often introduced after the carrier and peaking amplifiers output path to fine tune the load modulation behavior. Another consideration to the basic design is the impedance inverter's characteristic, as it affects the power range of the system depending on the transistor's knee voltage. To enhance the basic Doherty operation, uneven drive of the two amplifiers was discussed, where instead of driving both amplifiers equally, they are driven unevenly to enhance either linearity or efficiency. Another way of enhancing

the Doherty operation is the adaptive gate bias voltage, where the gate of the peaking amplifier's transistor is biased adaptively depending on the input signal's envelope to synthesize an ideal current profile for the Doherty system. Furthermore, an adaptive uneven drive method was discussed which adaptively changes the split of the input signal to the carrier and peaking amplifier depending on the input signal's envelope, to improve both linearity and efficiency. Finally, a bandwidth enhancement architecture was discussed, which relies on changing the impedance inverter transformation ratio to a smaller ratio to avoid issues such as frequency drift of the inverter due to the larger transformation ratio, therefore maintaining a better match over a wider frequency range.

Usually, power amplifiers are optimized for efficiency, and are later linearized. The most widely used way of linearization is DPD due to its low complexity and ease of implementation. A predistorter equalizes the gain and phase shift of the amplifier to produce a near ideal response at the output of the DPD and amplifier cascade system. Memoryless DPDs, such as LUT, are the simplest form of linearization and are used for any amplifiers that do not exhibit memory effects. Memory DPD are used when the amplifier exhibits strong memory effects and are more computationally expensive. The memory polynomial is very popular in the industry and is used as a benchmark for other models, but suffers from computational cost as its identification process involves inverting huge matrices. Simpler models discussed include two-box models which combine FIR filters acting as a memory component, and a memoryless model. Finally, the NLUT model has the advantage of simplicity, easy identification, and competitive performance, but suffers from memory consumption.

In this thesis, a Doherty power amplification system will be designed with a class AB and a class C as basis for the system. The Doherty power amplifier architecture was chosen for its simplicity and compactness, as it does not require additional circuitry which might not be possible for satellite systems to support. The amplifiers will be designed using GaN transistors to maximize efficiency and reliability. Finally, the Doherty system will be linearized using different models and discuss the results.

Chapter 3. Design of S-band Amplification Systems

In this chapter, the process of designing S-band amplification systems will be detailed. Specifically, the chapter will start with the design and verification of a single-ended high efficiency PA operating around 3.5 GHz using the CGH40010F transistor from Cree-Wolfspeed. Furthermore, the chapter will detail the design and verification of a Doherty PA using the designed single-ended PA as a basis. Doherty-specific enhancement techniques will be studied and detailed.

3.1. Design of Single-ended PA

3.1.1. Bias level. The transistor's model used is a large signal model from Cree-Wolfspeed, with model number CGH40010F which is suitable for the project as it is rated at the S-band, and its operating output power is 10W. The transistor is designed to operate at a drain voltage of 28V, with the gate voltage level varied upon the need. In this project's case, a single-ended amplifier is expected to provide reasonable linearity and efficiency, hence the transistor is expected to be biased at class AB condition. For a class AB operation, 200 mA was chosen as a reasonable starting point for the quiescent drain current. To achieve this, the gate-to-source voltage Vgs was set to -2.7V.

3.1.2. Load-pull and source-pull. Load-pull and source-pull are important measurements for any power amplifier designs. Indeed, they are used to obtain the optimal operating parameters to get a specific efficiency requirement, output power requirement, or a combination of both. Generally, a basic load-pull setup involves a device under test (DUT), and a calibrated tuned output load, such that the load impedance will be tuned and varied, and key performance parameters (mainly power and efficiency) are obtained for each variation. Also, the input can be tuned such that the power gain of the DUT is boosted, which makes source-pull measurements also important in PA design. Other parameters that can be controlled include the input available power, and bias level of the transistor. Generally, the results of load-pull measurements are displayed as contours of constant power or efficiency, where any impedance on the contour will result in that power or efficiency, and the impedances within the contour will result in stricter requirements such as higher power, or higher efficiency.

ADS provides a load-pull measurement setup as seen in Figure 3.1. The available power, bias levels, and source impedance are parameters that can be fixed, while the load impedance is varied. The region that is covered by the output tuner is specified by how many points are taken into account in impedance variations, and the range over which the impedances are allowed to vary. Generally, the range of impedances to be varied is initially wide, and then narrowed down to the area where the optimum power or efficiency are obtained.

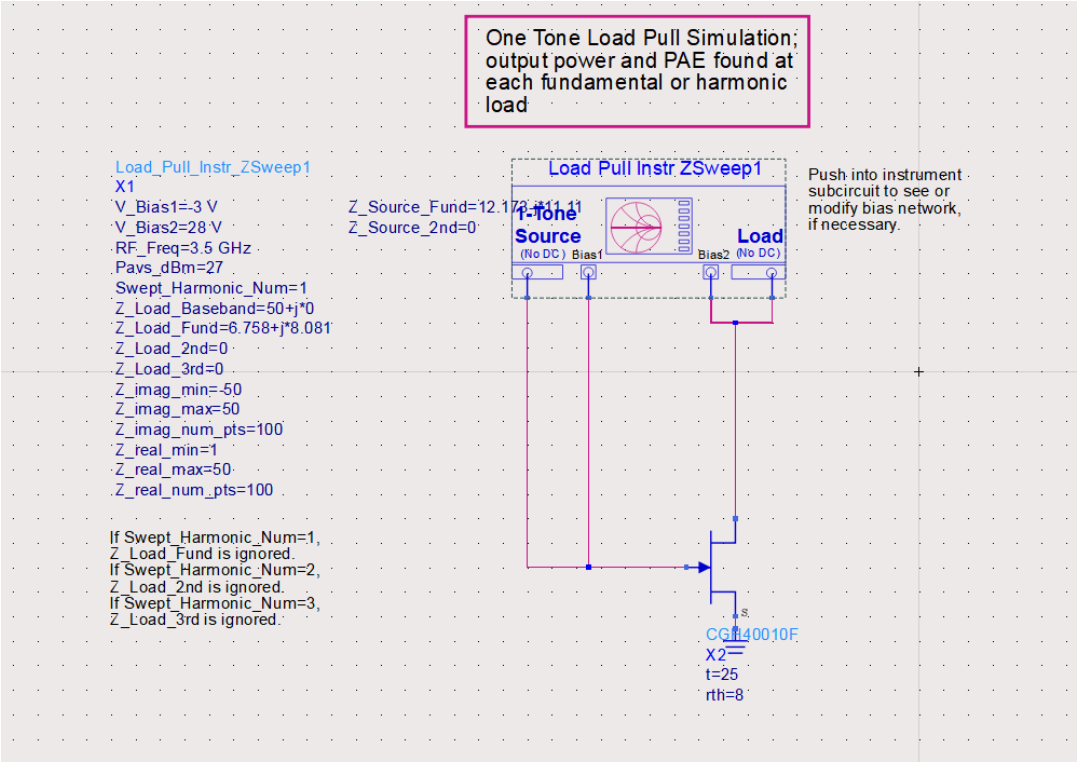

Figure 3.1: ADS Load-pull setup

After the simulation is finished, the contours are plotted on a Smith Chart. In the case of ADS load-pull guide, both power and efficiency are measured as seen in Figure 3.2, and the results are expected of this transistor which is 40 dBm (10 watts) and 79.776% PAE. The process of obtaining the optimum load impedance and source impedance is iterative, and it ends when both source-pull and load-pull results match and no further improvement can be made. The results of this process are summarized in Table 3.1. It is important to note that these results are obtained under ideal conditions

since the simulation uses ideal components to feed the transistor, which real transmission lines and capacitors will not be able to match.

Table 3.1: Load-pull and source-pull results

Power output level (dBm)	Optimum load reflection coefficient	Optimum source reflection coefficient	PAE (%)
40	0.7321∠158.7	0.9138∠154.9	79.8%

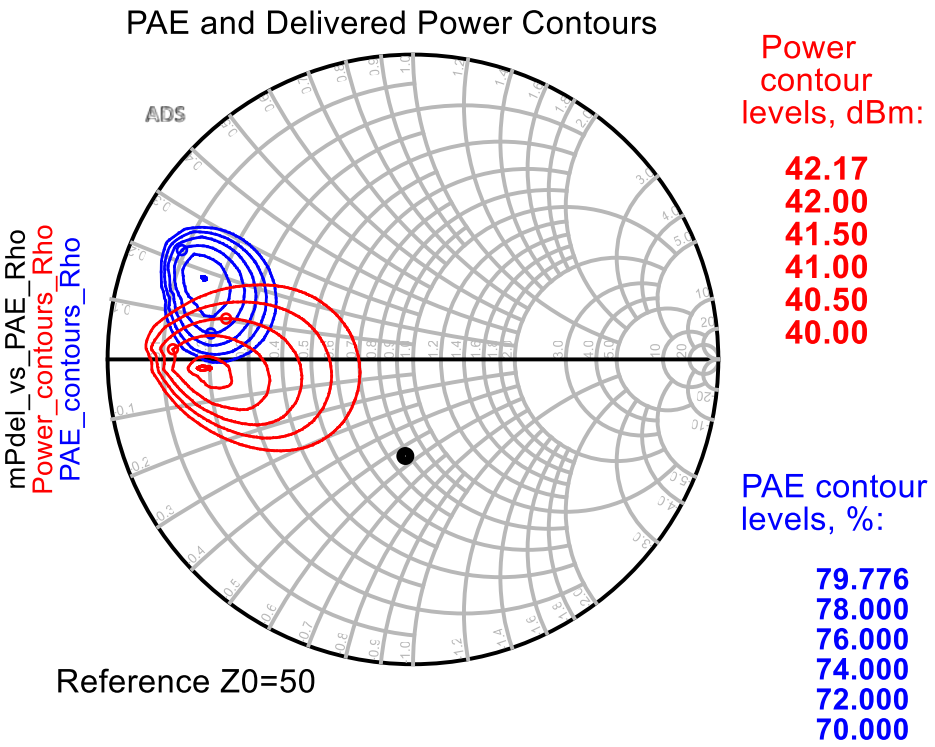

Figure 3.2: Load-pull simulation results for the single ended PA

3.1.3. Stability analysis and stabilization. Before the design of the matching networks, the stability of the transistor must be considered as it heavily affects the design of the matching networks. ADS offers an S-parameters probe pair to be used at the gate and drain of the transistor to measure the stability indices. According to the template, both indices should be less than 1 for the transistor to be stable. Figure 3.3

shows the transistor's stability indices before stabilizing for both the gate and drain ports of the transistor. For unconditional stability, both indices have to be less than 1. According to these results, the transistor is potentially unstable and can oscillate at frequencies below 1 GHz. To stabilize the transistor, the stabilization network shown in Figure 3.4 was connected to the gate of the transistor. The network consists of a resistor to cancel the negative resistance causing oscillation, and a capacitor in parallel to enhance the response of the transistor at low frequencies. The values were chosen based on trial and error until the transistor is completely stabilized. The network is usually connected to the gate of the transistor to minimize its effect on RF performance, specifically the gain of the amplifier. The resulting stability indices reported in Figure 3.5 demonstrate the ability of the stabilization network in making the transistor unconditionally stable over the entire frequency range.

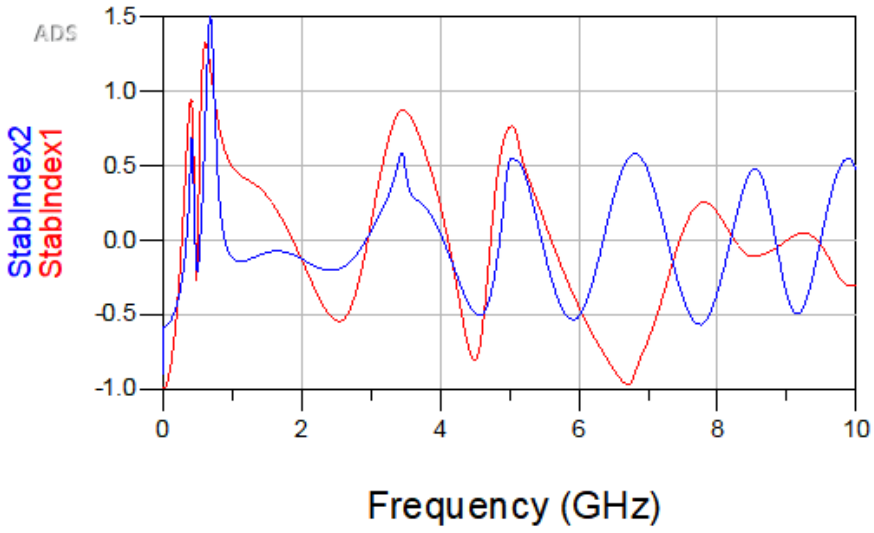

Figure 3.3: Stability indices of the transistor before stabilization

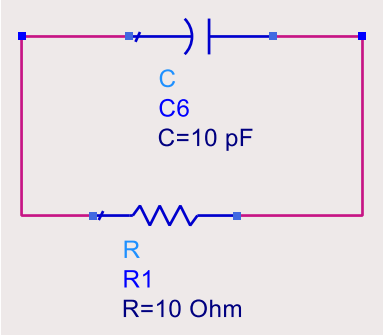

Figure 3.4: Stabilization network used

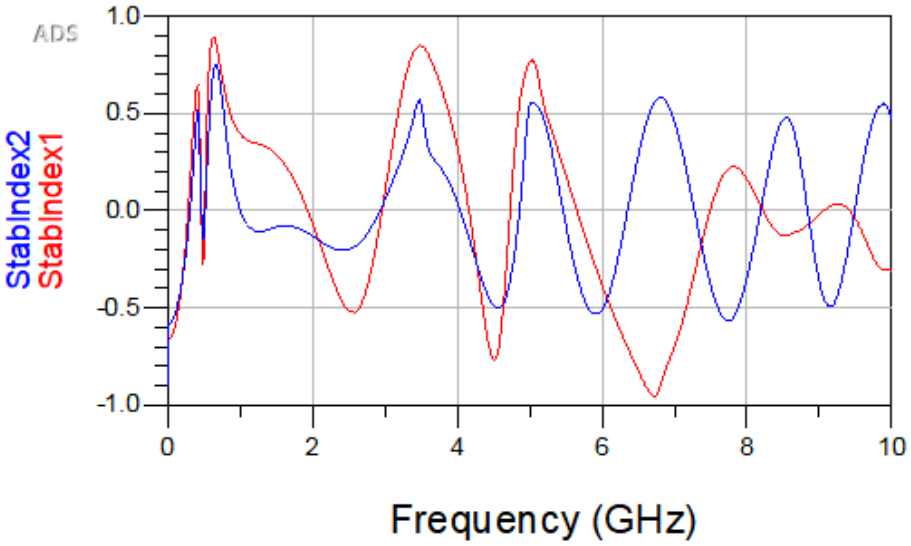

Figure 3.5: Stability indices of the transistor after stabilization

3.1.4. Matching networks design. A common architecture for matching networks would be an L matching network at the source as shown in Figure 3.6, and multiple L networks at the drain, which depend on the degrees of freedom necessary. An example of that is shown in [25] and can be seen in Figure 3.7. This architecture was used to allow easy fine tuning and multiple degrees of freedom to ensure exact matching. The variables $L1, L2, L3, L4, L5, L6,$ and $L7$ refer to the length of the transmission lines in mils, while the width of the transmission lines is fixed to the equivalent of that needed for a 50 Ω characteristic impedance. This width corresponds to 74 mils for the RO3003 substrate used. The parameters of this substrate are reported in Table 3.2.

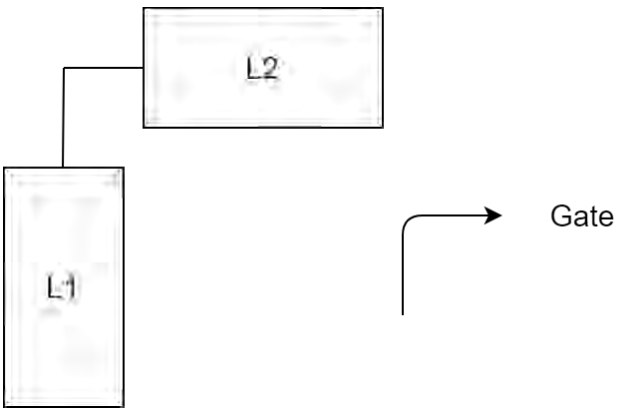

Figure 3.6: Input matching network

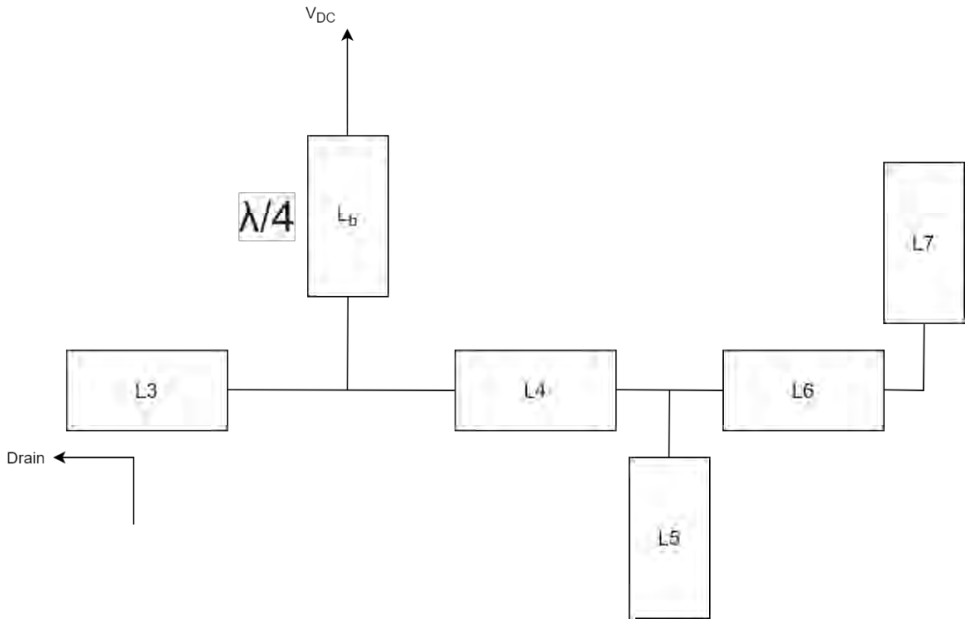

Figure 3.7: Output matching network architecture

Table 3.2: Substrate parameters

Substrate model	Rogers RO3003
Dielectric constant (ε_r)	3.00
Dissipation factor	0.001
Substrate thickness	30 mils (0.75 mm)
Copper cladding	17 µm

In order to check the impedance presented to the transistor and therefore tune the matching network accordingly, an S-parameters probe is used which measures the reflection coefficient in both directions and then converts them into impedances. The corresponding schematic is shown in Figure 3.8.

The next step is to design the matching network that corresponds to the optimum impedances. This can be done either by manually varying the physical dimensions of the transmission lines or using the optimization controller with certain goals such as showing certain impedance at a certain location. As for the input matching network, a simple L network was chosen for simplicity and compactness. The final circuit is shown in depicted in Figure 3.9 and Figure 3.10 in ADS, and the lengths of the transmission

lines are reported in Table 3.3. Furthermore, the schematics include a number of practical considerations for layout design, which are as follows:

- DC blocking capacitors at the input and output of the amplifier, with values of 1 µF.
- Gaps for soldering the lumped components.
- A taper for each bias line to transform the line from a small line to a bigger one to ease soldering any needed bigger capacitors and DC power supply connectors.
- Bypass capacitors positioned after the quarter wavelength line to short the RF signal to ground to protect the DC supply.
- A taper line on the gate of the transistor and a taper on the drain of the transistors matching the dimensions of the gate and drain leads of the transistors.

The bias feed to the transistor was designed in such a way that the line shows an open circuit to the RF path in order to keep the RF signal flowing exclusively to the transistor and out of the transistor without the RF signal leaking to the DC path. Furthermore, a bypass capacitor was used to show a short circuit at the fundamental frequency to protect the power supply from any ripple or noise caused by the RF signal. Figure 3.11 and Figure 3.12 show the simulation setup used to optimize the bias network. Figure 3.13 and Figure 3.14 show the performance of the bias network, and bypass capacitor. In Figure 3.11 and Figure 3.13, S_{22} refers to the reflection coefficient shown to the bypass capacitor path, while, in Figure 3.12 and Figure 3.14, S_{11} refers to the reflection coefficient of the quarter wavelength line as shown in the figure. It can be seen from these figures that the desired conditions have been met and this bias line design can be used in the amplifier.

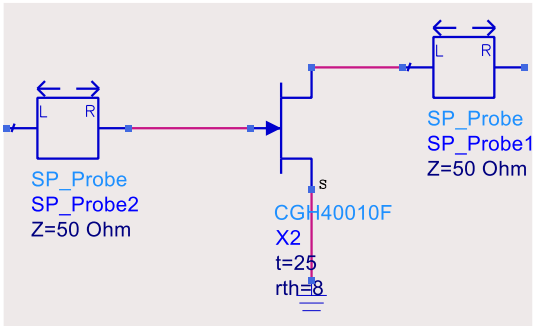

Figure 3.8: S-parameters probe in ADS

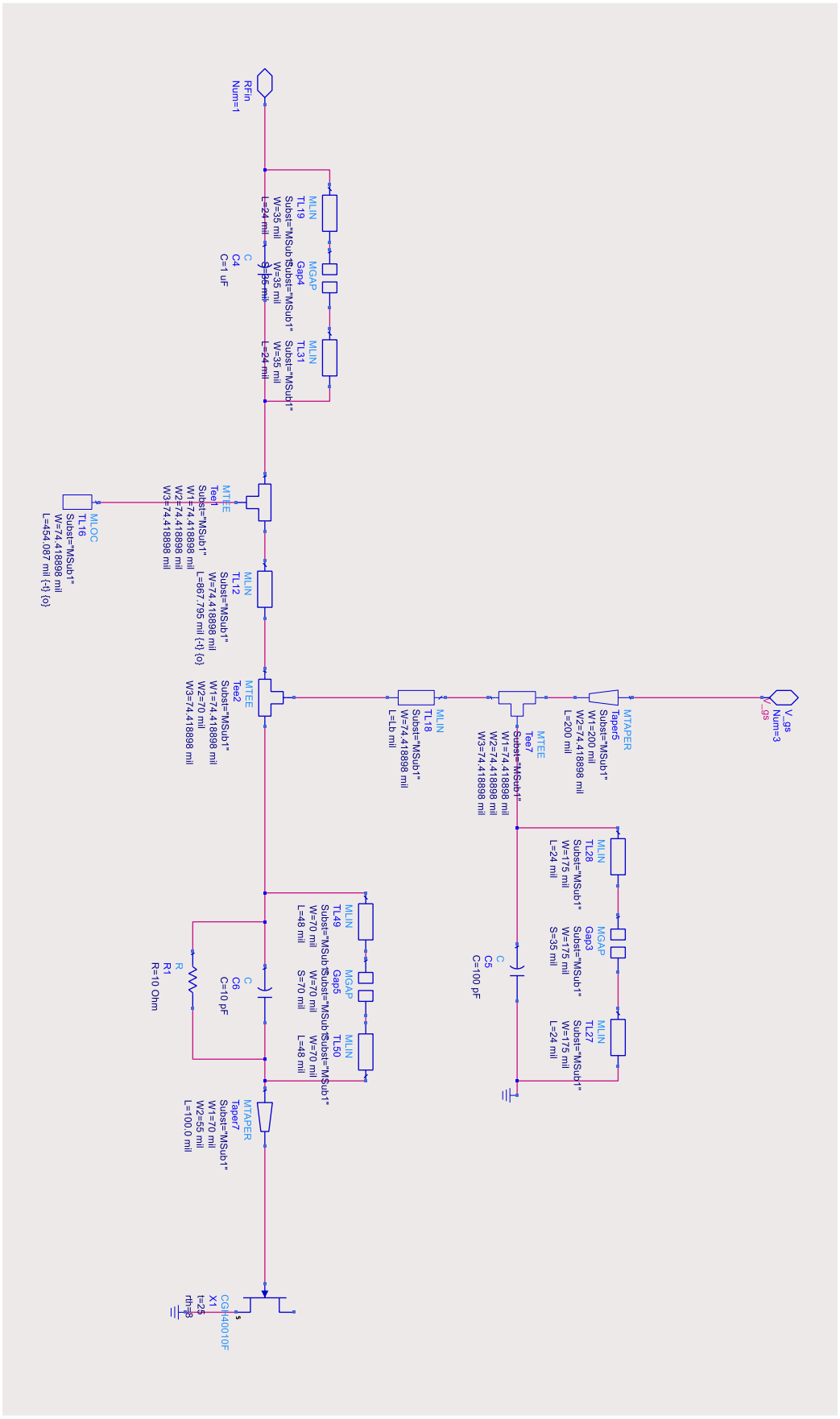

Figure 3.9: Final schematic of single-ended PA's input matching network in ADS

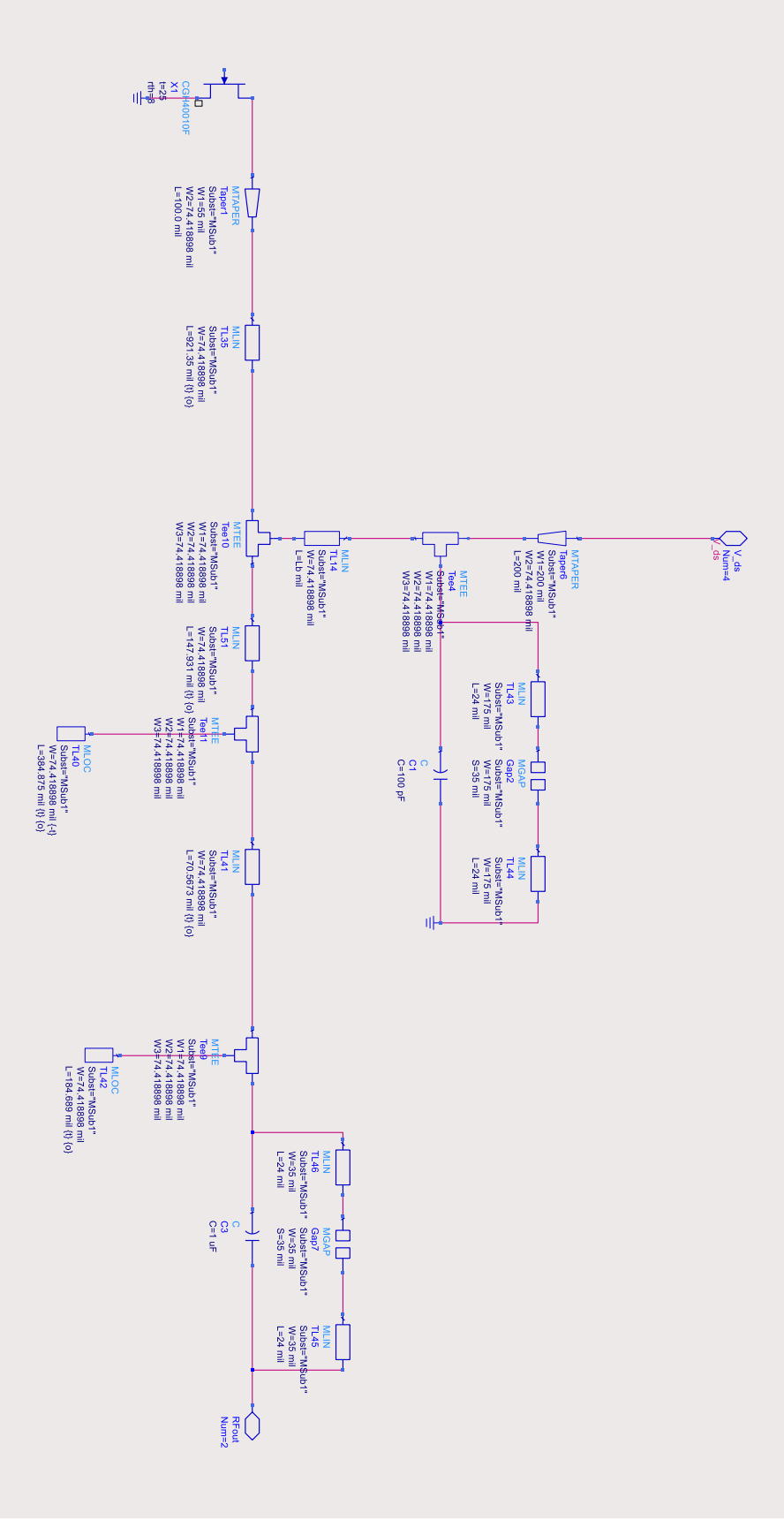

Figure 3.10: Final schematic of single-ended PA's output matching network in ADS

Table 3.3: Lengths of transmission lines in matching networks

Line	Length (mils)
L1	454.09
L2	867.90
L3	921.35
L4	147.93
L5	384.88
L6	70.57
L7	184.69
Lb	521.00

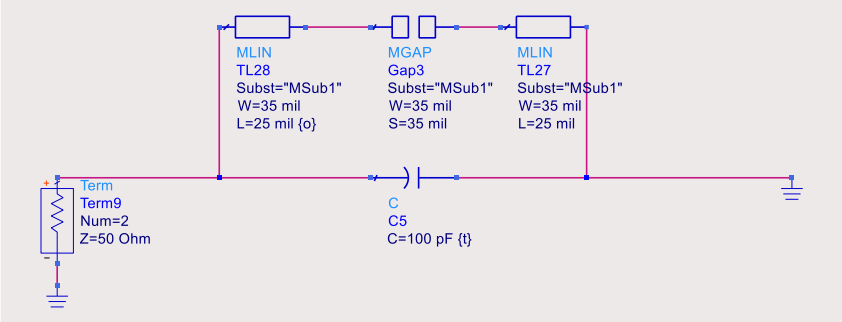

Figure 3.11: Bypass capacitor simulation

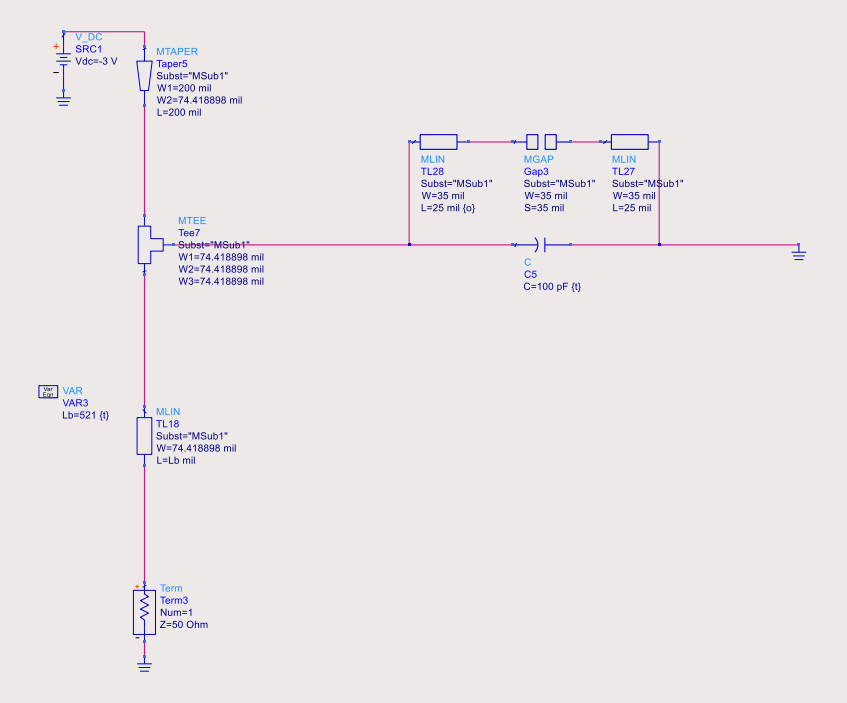

Figure 3.12: Quarter wavelength line simulation

3.1.5. Performance assessment of the single-ended PA.

3.1.5.1 CW characterization. Keysight's ADS provides a versatile environment to test the single-ended amplifier under various conditions, and in this section, the PA will be tested under 1-tone excitation signal. The test setup is shown in Figure 3.15.

Based on the simulation results, it was found that the P_{1dB} point is at 21.2 dBm input power and 36.733 dBm output power (4.71W). The linear gain of the designed PA is 16.6 dB. The PAE at the 1 dB compression point is 58%, and peaks at 74% when the PA is overdriven heavily. The gain, PAE, and drain efficiency versus output power are reported in Figure 3.16. Furthermore, the gain and PAE change as a function of the frequency are reported in Figure 3.17.

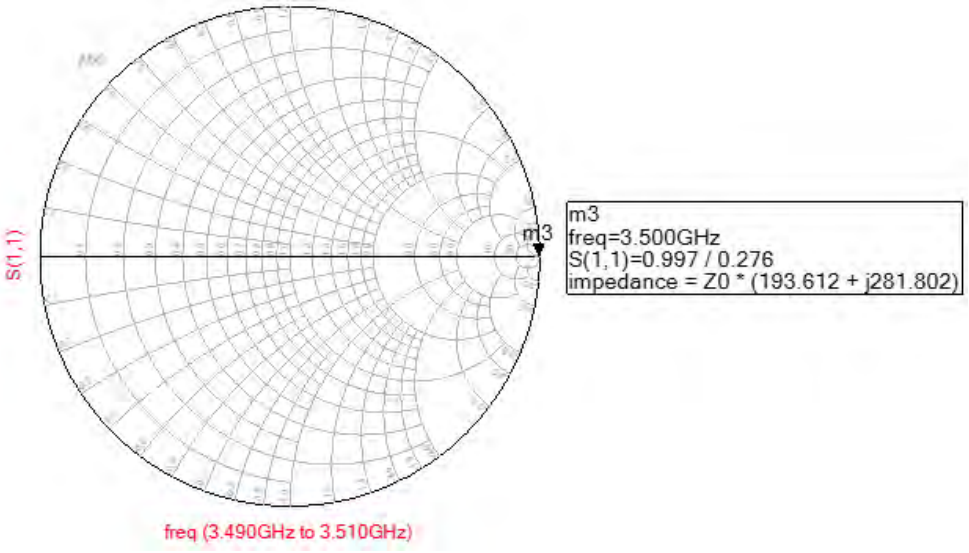

Figure 3.13: Simulated performance of quarter wavelength line

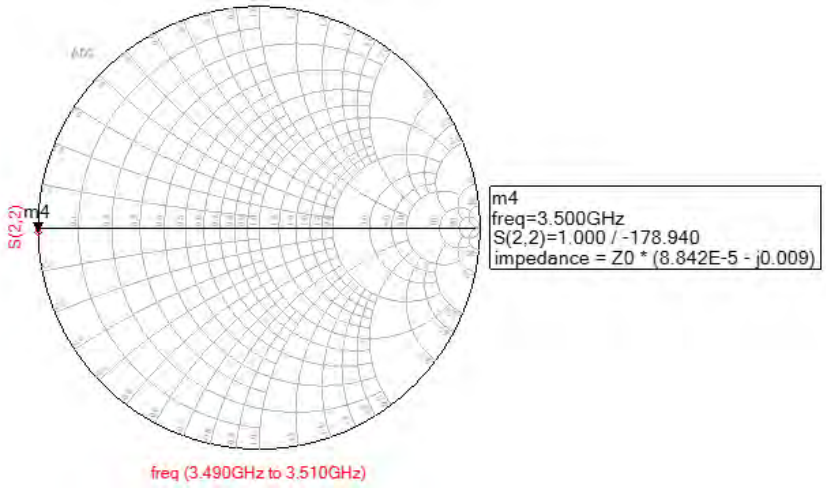

Figure 3.14: Simulated performance of bypass capacitor

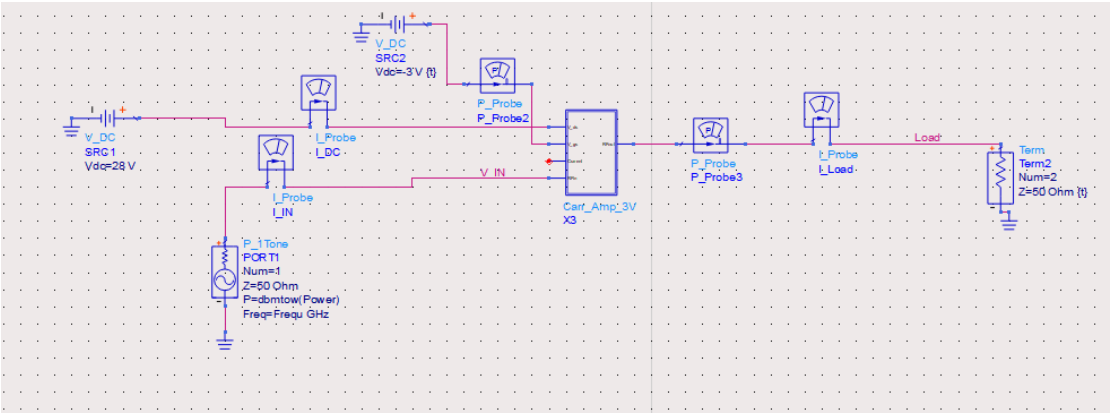

Figure 3.15: ADS setup for 1-tone test

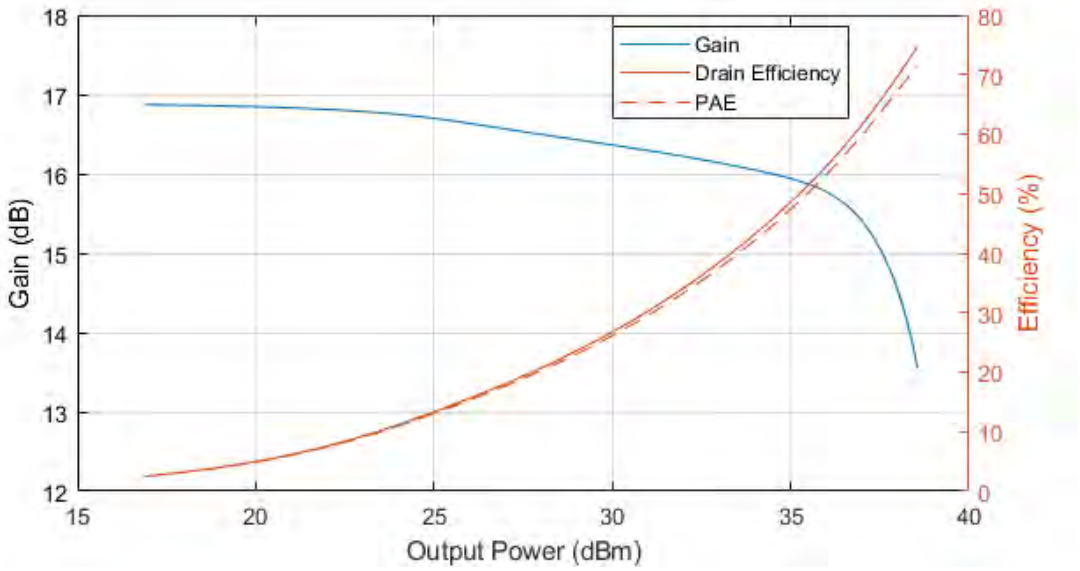

Figure 3.16: Simulated gain and PAE of single-ended PA versus output power

3.1.5.2 Test with modulated signal. The power amplifier's behavior with real signals can be verified using ADS' mixed signal design environment. The test signal is an LTE signal with 20 MHz bandwidth, sampled at 200 MHz, with 10 dB peak to average power ratio (PAPR). This signal is fed to an RF modulator block to modulate the signal to the desired center frequency and power level. Further, the modulated signal is fed to the amplifier's analog schematic and is simulated using the Envelope simulator. The Envelope simulator allows ADS to capture waveform data in time and frequency domain while using the DSP library. Finally, the output is fed to a numeric sink for further post-processing and results extraction. The setup is shown in Figure 3.18.

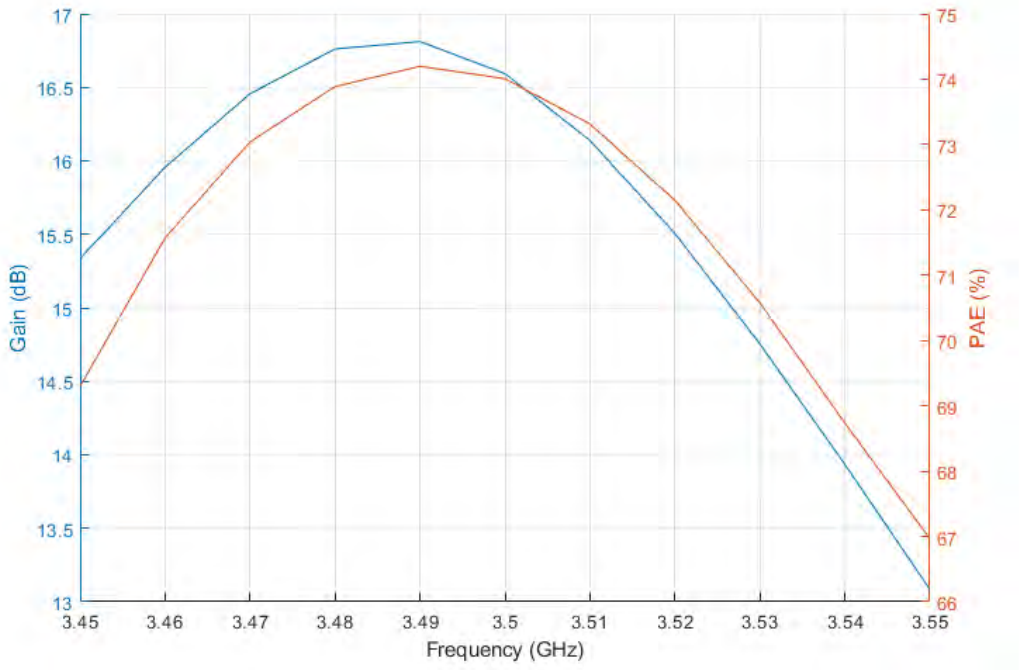

Figure 3.17: Simulated gain and PAE of single-ended PA versus frequency

The performance of the amplifier was assessed in terms of gain, PAE, and linearity. For gain and PAE, average values over the signal samples will be used, which are shown in Figure 3.19.

Since the final amplifier is intended for satellite applications in the S-band, it is useful to establish a benchmark of how does the single-ended amplifier perform in terms of linearity requirements. The radio regulations document by ITU [26] specifies the amount of out-of-band(OoB) emissions permitted in satellite applications, in the form of a mask where the output spectrum of the amplifier has to be below it (signal power output should be within the mask). The mask equation is shown in (**18**).

$$\boldsymbol{OoB = 40 \log\left(\frac{F}{50} + 1\right) \quad dBsd} \qquad (18)$$

Where F is the frequency offset from the edge of the assigned band, and dBsd is a decibel measurement relative to the maximum value of the center bandwidth of the PA.

The input signal was set to 21 dBm, with an output power of 36 dBm which drives the amplifier heavily into compression (at 2 dB compression point) showing the worst-case scenario for the amplifier in terms of linearity. The output spectrum is reported in Figure 3.20.

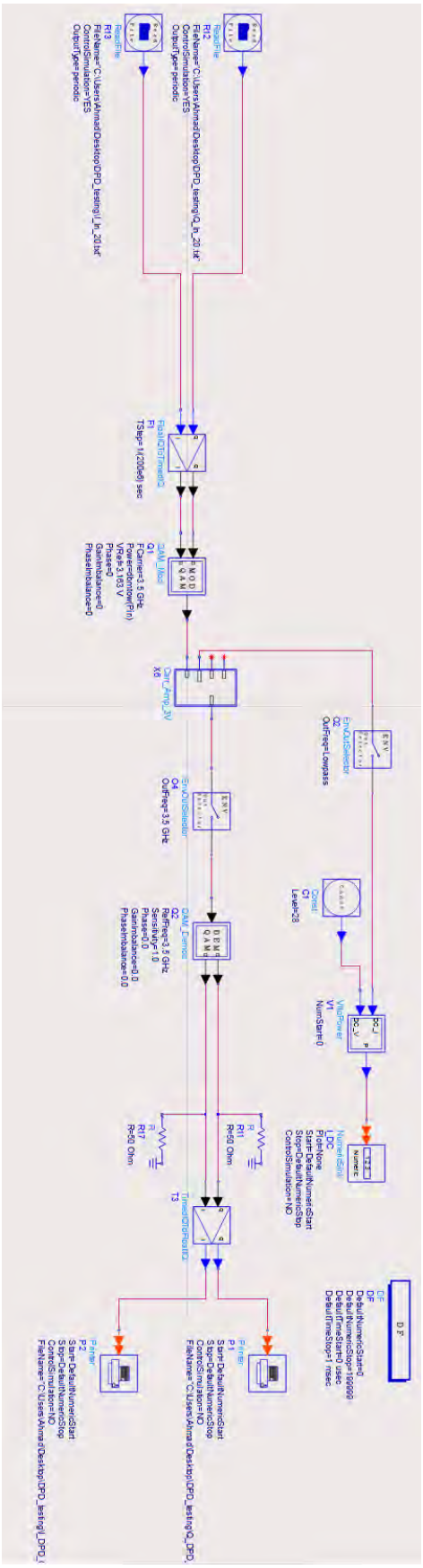

Figure 3.18: Mixed-signal testing setup in ADS

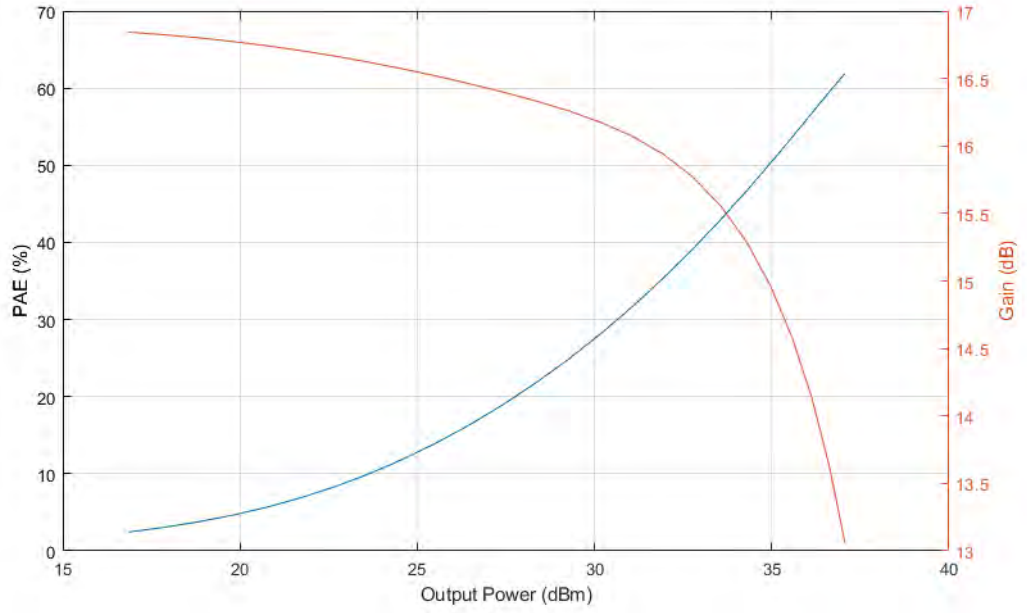

Figure 3.19: Simulated gain and PAE of single-ended PA with modulated signal

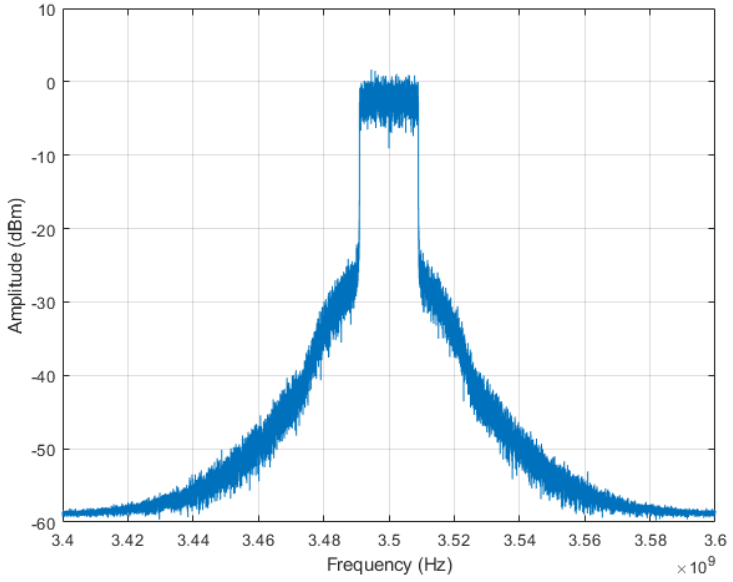

Figure 3.20: Simulated output spectrum of single-ended PA

From the ITU documentation [26], the mask was synthesized and is superimposed on the output spectrum of the single-ended PA for a 20 MHz bandwidth signal centered at 3.5 GHz in Figure 3.21. From this figure, it can be seen that the

amplifier passes the emission requirements for a satellite transmitter.

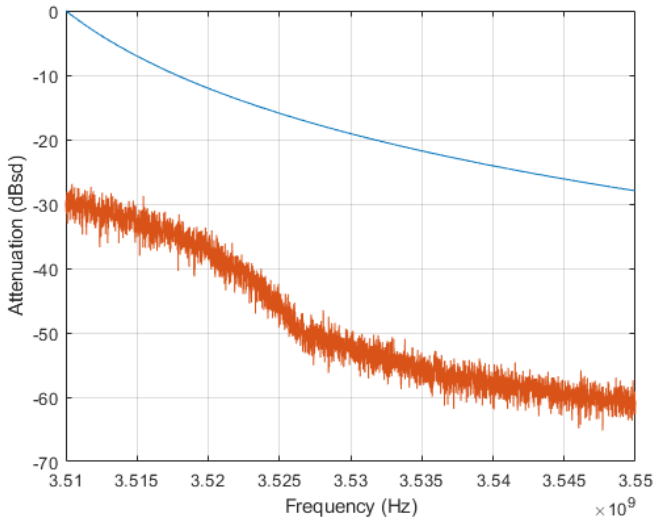

Figure 3.21: Simulation of the emission mask test for the single-ended PA

Another measure for the performance of a PA's linearity is the error vector magnitude (EVM). The EVM is a measure of how far the output constellation are symbols from the input constellation symbols. A graphical representation of the EVM is shown in Figure 3.22. The EVM is calculated across all the signal samples and is expressed as a percentage of the mean power of the error vector to the mean power of the signal [19]. The EVM equation is expressed as shown in equation (**19**).

$$\boldsymbol{EVM}(\%) = \sqrt{\frac{\frac{1}{N}\sum_{i=1}^{N}|e_i|^2}{\frac{1}{N}\sum_{i=1}^{N}|S_i|^2}} \qquad (19)$$

Where N is the number of samples, e_i is the error vector, and S_i is the reference signal sample.

The EVM for the single-ended PA was assessed using the same LTE signal used in the previous simulations. The results are shown in Figure 3.23 and indicate a satisfactory linearity performance up to an average input power of 14 dBm given that it passes the 3GPP EVM requirements for 256-QAM (i.e. less than 4.5%) [27]. However, at higher output power, the EVM performance of the single ended PA does not meet the 3GPP standard requirements. Therefore, linearizing the amplifier is needed

in order to drive it deeper into compression for larger output power and higher efficiency.

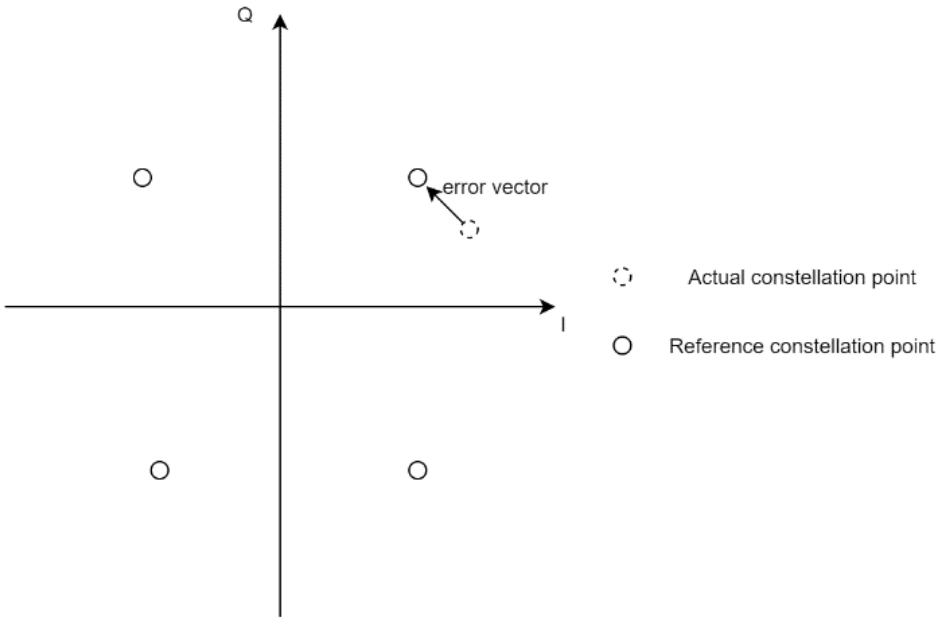

Figure 3.22: EVM graphical example for a QPSK modulation

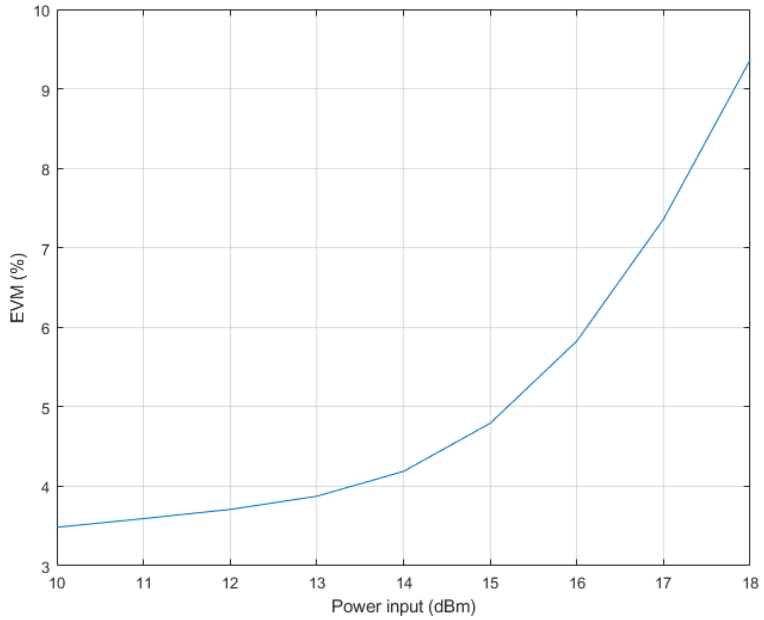

Figure 3.23: EVM results of single-ended PA

3.2. Design of Doherty Power Amplifier System

3.2.1. Hybrid coupler design. The Doherty PA requires a power divider and a 90

degrees phase shift line to the peaking amplifier. This requirement can be satisfied by the hybrid coupler which is shown in Figure 3.24. Port 1 is the RF input, ports 2 and 3 are the in-phase and the 90 degrees shifted RF outputs, respectively. Port 4 is the isolated port with 50 Ω termination to be connected to.

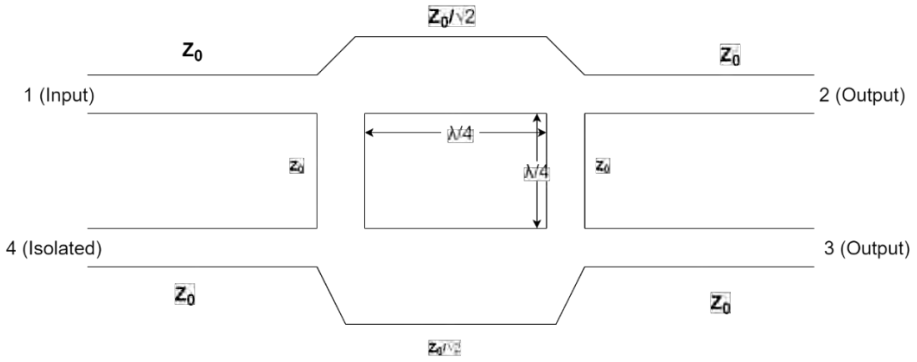

Figure 3.24: Hybrid coupler diagram

The ADS designed hybrid coupler is shown in Figure 3.25, and the results are reported in Figure 3.26 and Figure 3.27. which show acceptable power splitting with a balanced gain between the two output ports, and the desired phase shift between the ports at the operating frequency.

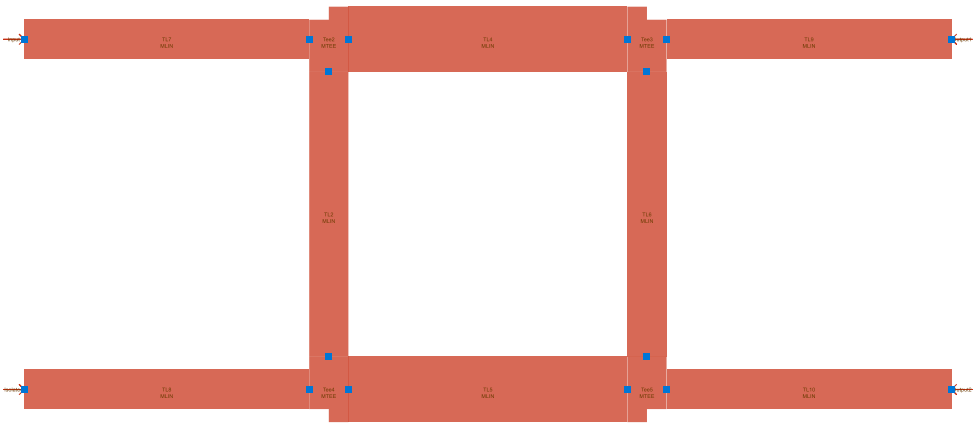

Figure 3.25: Layout of the hybrid coupler designed in ADS

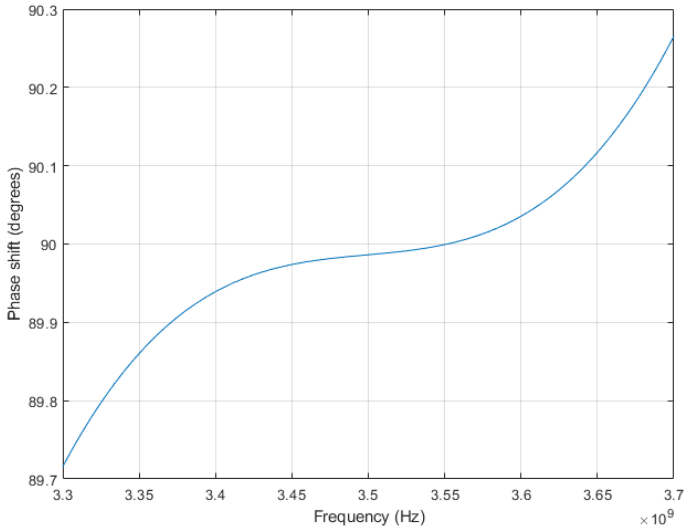

Figure 3.26: Simulated phase shift between the two output ports of the designed hybrid coupler

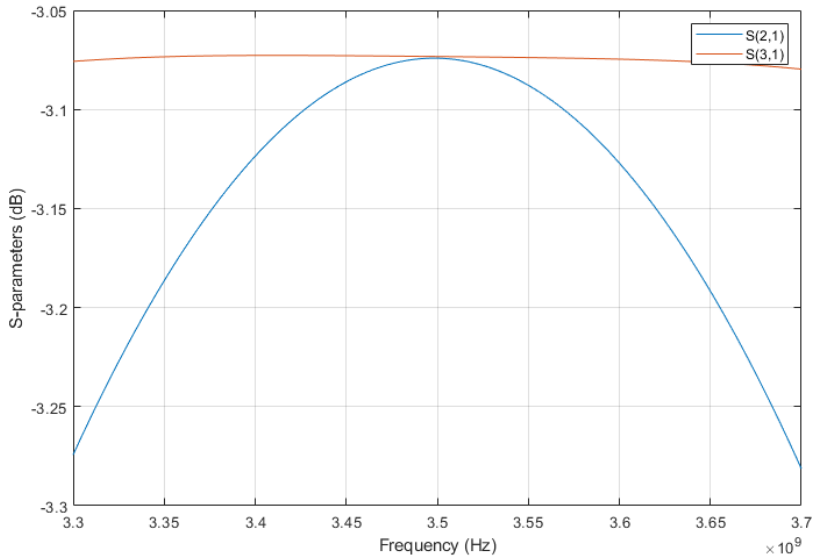

Figure 3.27: Simulated insertion loss of the design coupler

3.2.2. Load modulation implementation. After finalizing the single-ended PA design, the next step is to use it in a Doherty configuration. The architecture used is the bandwidth enhancing architecture proposed in [3]. The system level schematic of the designed Doherty PA is shown in Figure 3.28 in a single-tone test setup. The parameters of the lines are reported in Table 3.4. The phase offset lines were added at the output of the carrier and peaking amplifiers and tuned to achieve the load modulation desired for a proper operation of the Doherty configuration. This process was done using an S-parameters probe in order to ensure that an open circuit was presented to the output of

the peaking amplifier as shown in Figure 3.29. It shows that the peaking amplifier is effectively shut off as an open circuit until high power, and then the impedance drops down to around 50 Ω as desired for the load modulation. The peaking amplifier in this case is identical to the carrier amplifier, but with the bias level adjusted for class-C operation. The bias level of the carrier amplifier was adjusted to -3V as it was found to provide the optimal efficiency. The bias level was adjusted manually by sweeping the gate voltage of the peaking amplifier and observing the effect of the change of the bias level on the performance. The effects of the peaking amplifier's bias level on the Doherty PA gain and efficiency performances are reported in Figure 3.30 and Figure 3.31, respectively. In Figure 3.30, the green line shows the peaking amplifier with gate bias very close to the carrier amplifier, at -3.5V, which in effect results in a similar behavior to the single-ended amplifier with no real advantages of the Doherty architecture being apparent. This is clearly shown in Figure 3.31 where the green line shows poor efficiency in the lower power region. On the other hand, having the peaking amplifier's gate voltage far from the carrier amplifier's results in poor linearity as illustrated in gain plots but excellent efficiency range. Therefore, the compromise between efficiency and linearity is important to achieve, and a gate bias of -4.7V was chosen for the peaking amplifier. The gain and PAE of the Doherty PA designed using these specifications are summarized in Figure 3.32.

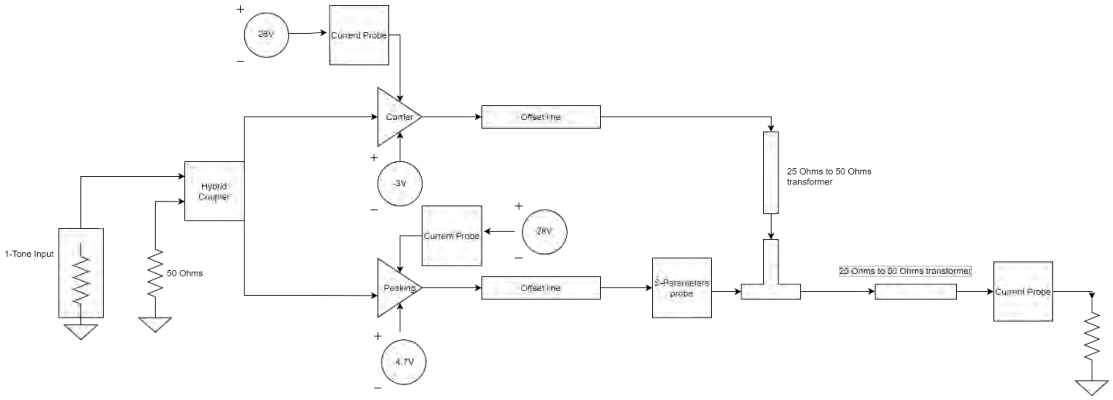

Figure 3.28: Block diagram of the Doherty PA schematic implemented in ADS

Table 3.4: Doherty PA parameters

Component	Value
Carrier and peaking offset lines	74 mils in width and 220 mils in length
Carrier amplifier's quarter wavelength line	124 mils in width and 530 mils in length
Output quarter wavelength line	124 mils in width and 530 mils in length

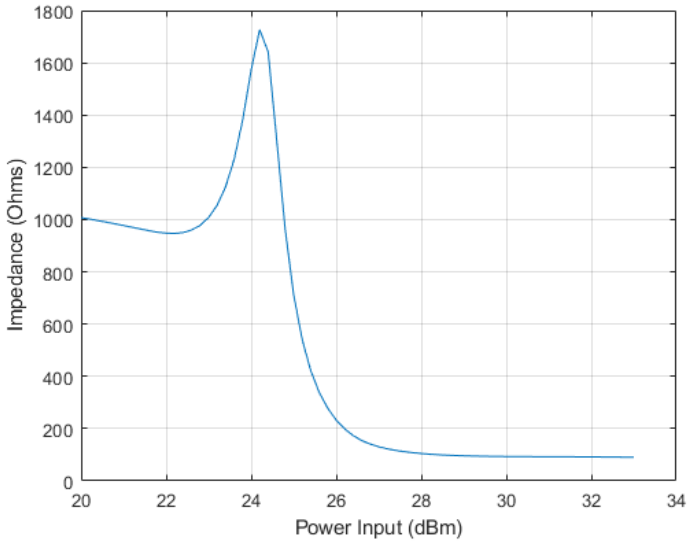

Figure 3.29: Variation of the peaking amplifier's output impedance

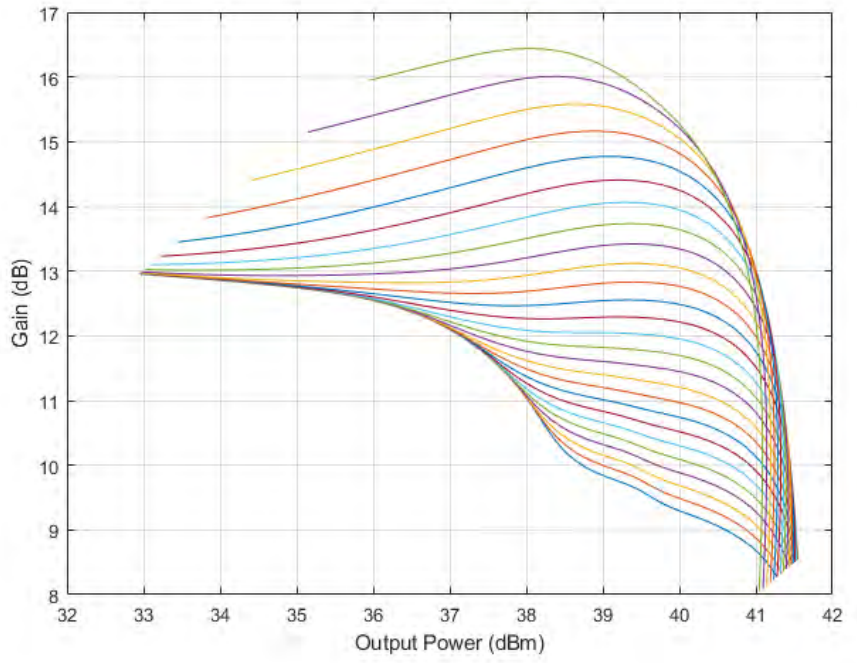

Figure 3.30: Simulated gain of Doherty PA as a function of the peaking amplifier gate bias

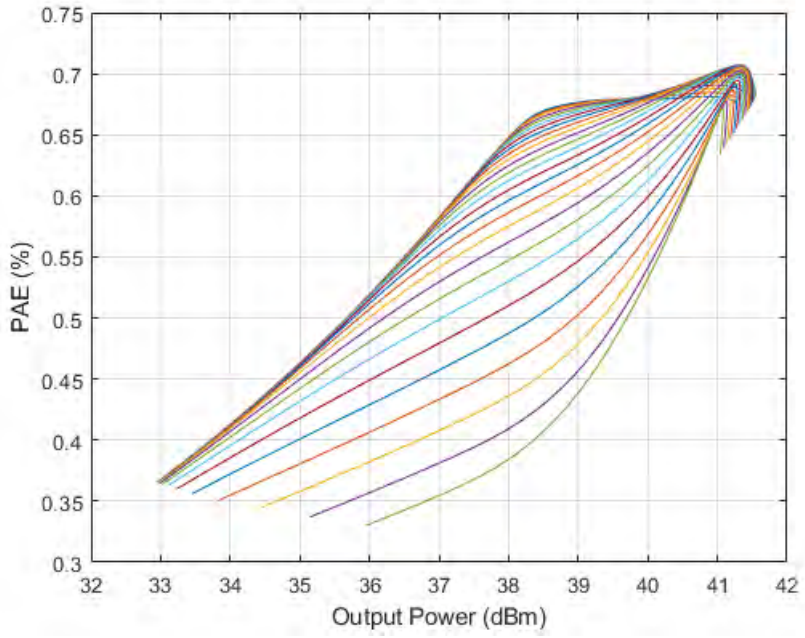

Figure 3.31: Simulated PAE of Doherty PA as a function of the peaking amplifier gate bias

Figure 3.33 and Figure 3.34 show the results of uneven power drive when applied to the designed Doherty PA. The even splitting refers to the traditional design where both the carrier and peaking amplifier get half the input signal each. The constant uneven power splitting refers to the carrier amplifier being fed more power than the peaking amplifier. Specifically, instead of having 50/50 split, the carrier amplifier is fed 67% of the input power while the peaking amplifier is fed the remaining 33%. Finally, the adaptive uneven splitting refers to adjusting the ratio adaptively with the input power to enhance the linearity while keeping the advantages of efficiency enhancement. The profile of the adaptive uneven splitting ratio of the signal fed to the carrier amplifier is shown in Figure 3.35. This figure shows that the splitting ratio starts from a 50% at lower power, and ramps up to approximately 70% around the turn-on point of the peaking amplifier, and then ramps down to 50% as the amplifier is driven towards peak power. The results show that the adaptive power splitting provide a compromise between the efficiency enhancement of the constant uneven power drive and linearity of even power drive.

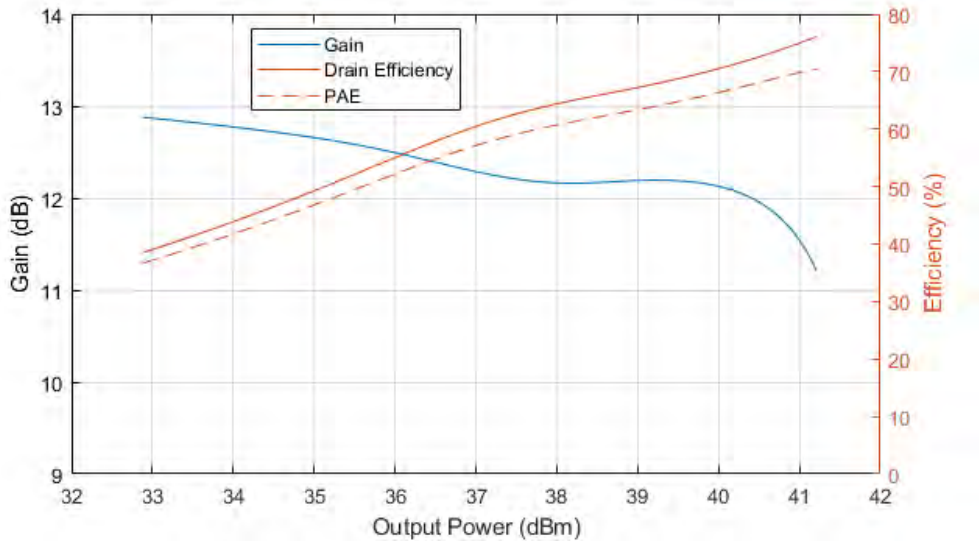

Figure 3.32: Simulated gain and PAE of the designed Doherty PA (CW)

Figure 3.36 and Figure 3.37 show the spectrum and emission mask test of the Doherty PA. As demonstrated by these figures, the designed Doherty PA passes the linearity the requirements for a satellite PA. The test was done using the same modulated signal used in the single-ended PA test.

Figure 3.38 shows the Doherty PA gain and efficiency performances with a modulated LTE signal. The efficiency of the amplifier shows the advantage of the Doherty configuration, as the efficiency shown to be increased both at saturation, and at different back-off powers. The improvement ranges from 4% at saturation to over 15% at 6 dB back-off power. In effect, this means that the amplifier is suitable to be used with high-order modulation signals with high PAPR. Figure 3.39 shows the EVM results for the Doherty PA with the same LTE signal used. It is seen from this figure that the PA needs linearization if it is to be used with power levels higher than 19 dBm.

3.2.3. Simulation of Doherty PA linearization. The AM/AM and AM/PM characteristics of the designed Doherty PA are shown in Figure 3.40 with an average input power of 20 dBm. From this figure, it is observed that the transistor model does not exhibit memory effects, and therefore, the PA can be linearized with a memoryless look-up table digital predistorter. The process was done using MATLAB, and it can be replicated using any other programming software.

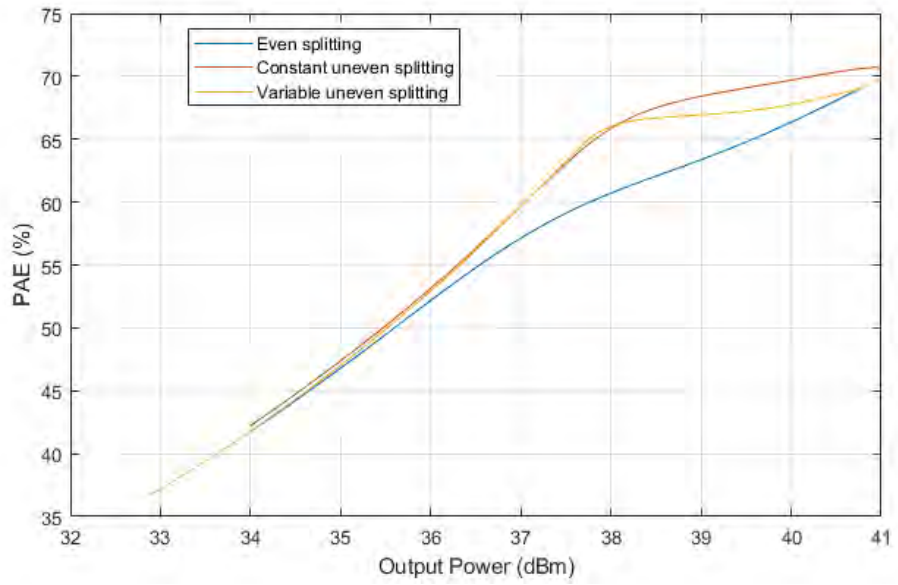

Figure 3.33: Simulated efficiency enhancement with uneven power splitting

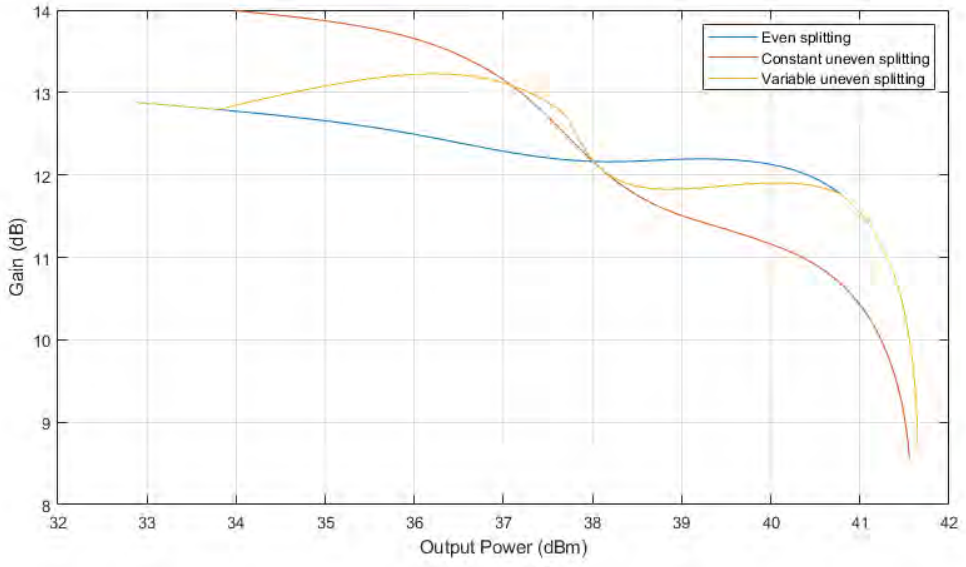

Figure 3.34: Simulated gain of the Doherty PA under uneven power splitting conditions

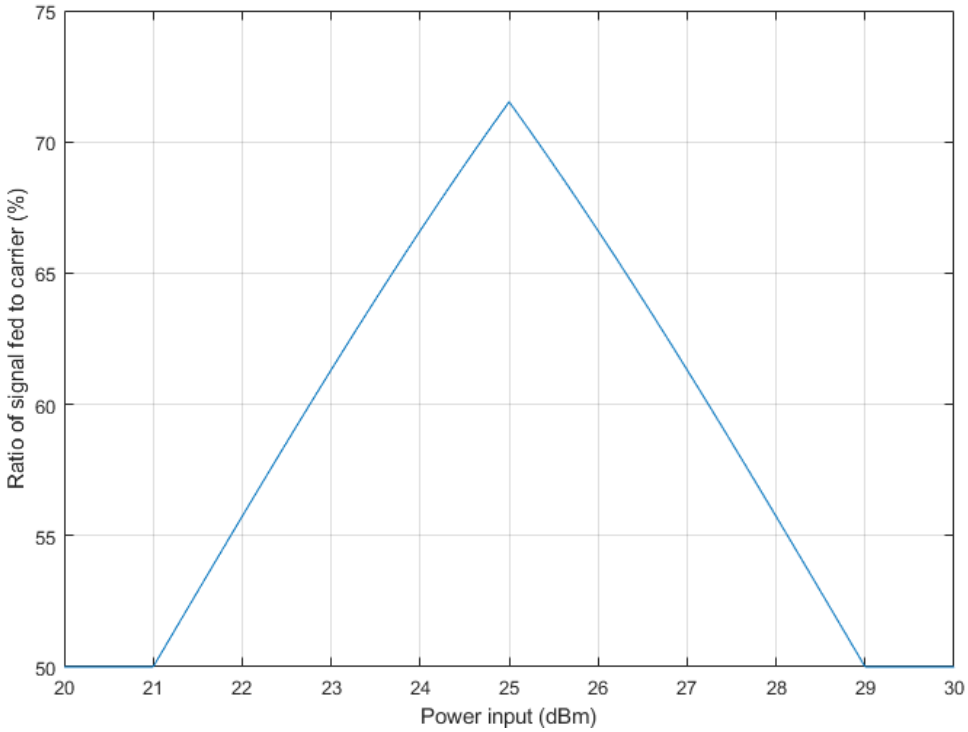

Figure 3.35: Adopted adaptive uneven split profile for the designed Doherty PA

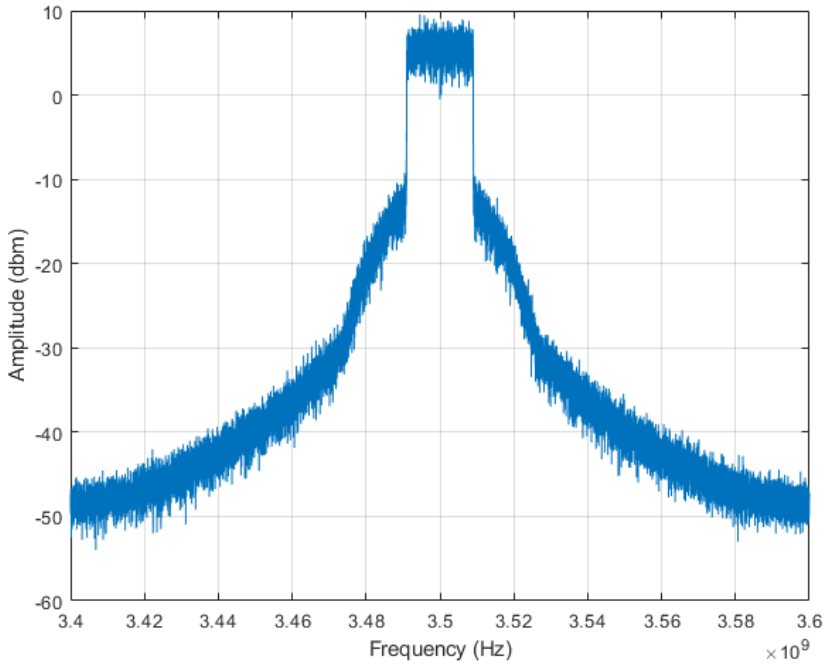

Figure 3.36: Simulated spectrum at the output of Doherty PA

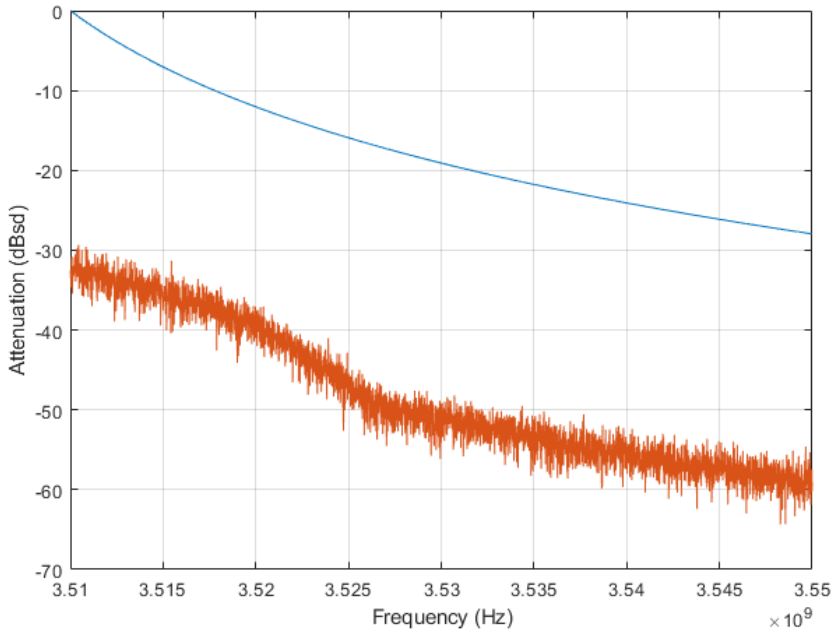

Figure 3.37: Simulated emission test of the designed Doherty PA

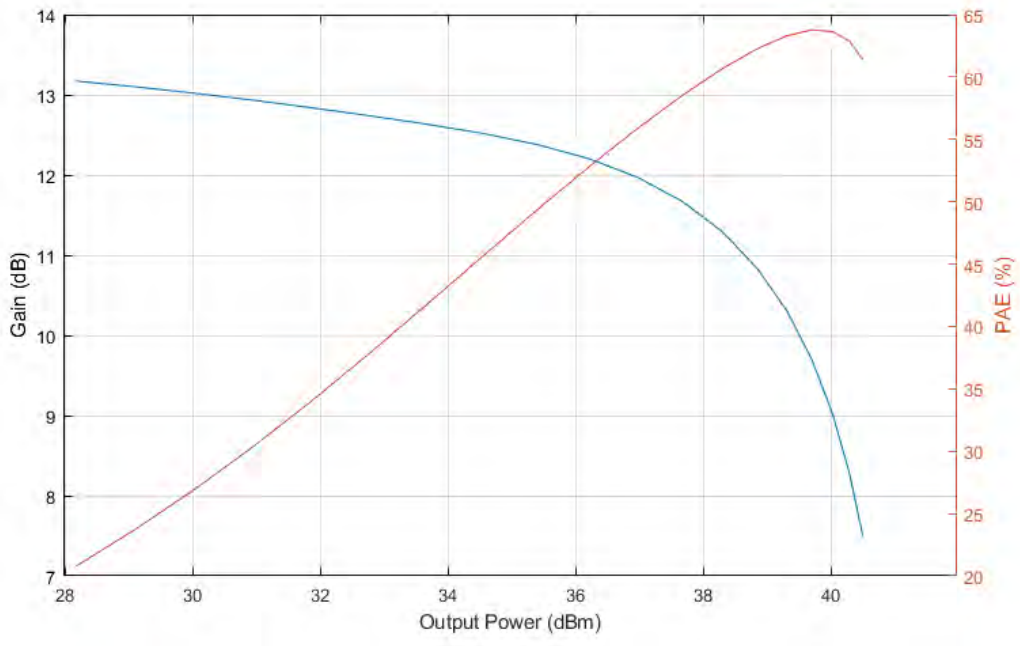

Figure 3.38: Simulated gain and PAE performances of the Doherty PA with modulated signal

Figure 3.41 shows the identification process of the DPD, where the DPD block and the identification algorithm are implemented in MATLAB, and the PA simulated on ADS. After identifying the DPD model, the power of the signal passed to the DPD must be

adjusted to ensure the gain expansion of the DPD does not overdrive the PA more than desired. Since the signal used has 10 dB PAPR, the input signal to the PA was chosen such that the maximum output of the PA is barely at saturation (42 dBm). The results of the linearization are shown in Figure 3.42 which shows significant improvement in the spectrum output. The EVM improved from 5.3% to 1.3% which satisfies the requirements for a QAM signal as per the 3GPP standard.

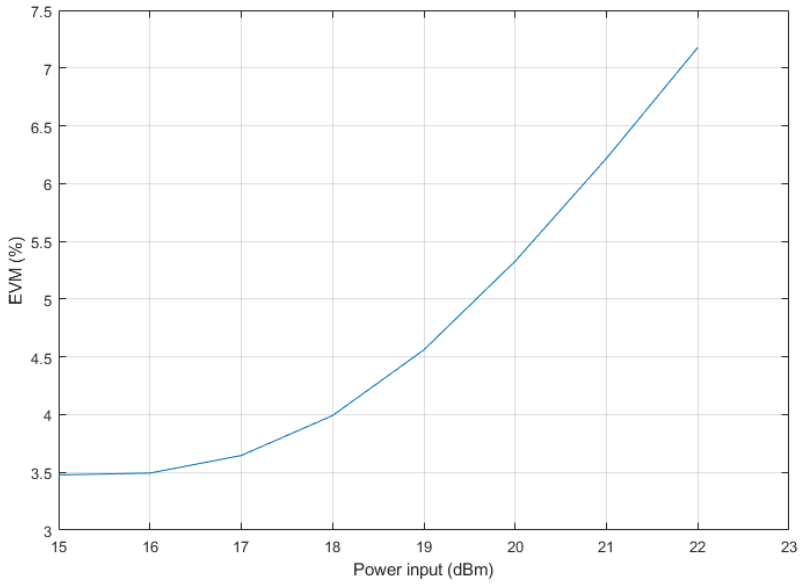

Figure 3.39: Simulated EVM results of the designed Doherty PA

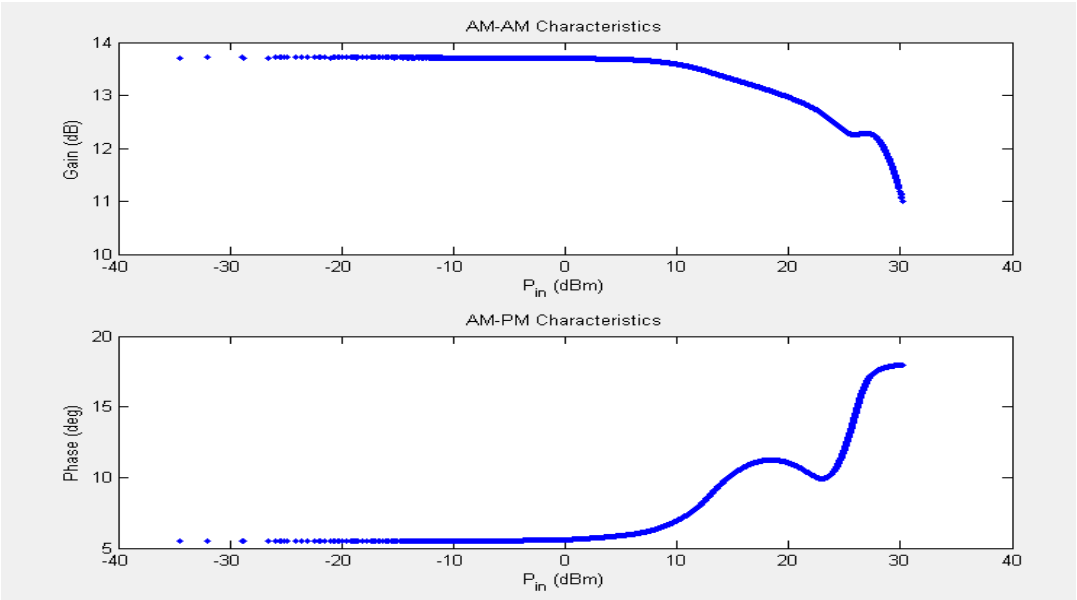

Figure 3.40: Simulated AM/AM and AM/PM plots of the Doherty PA

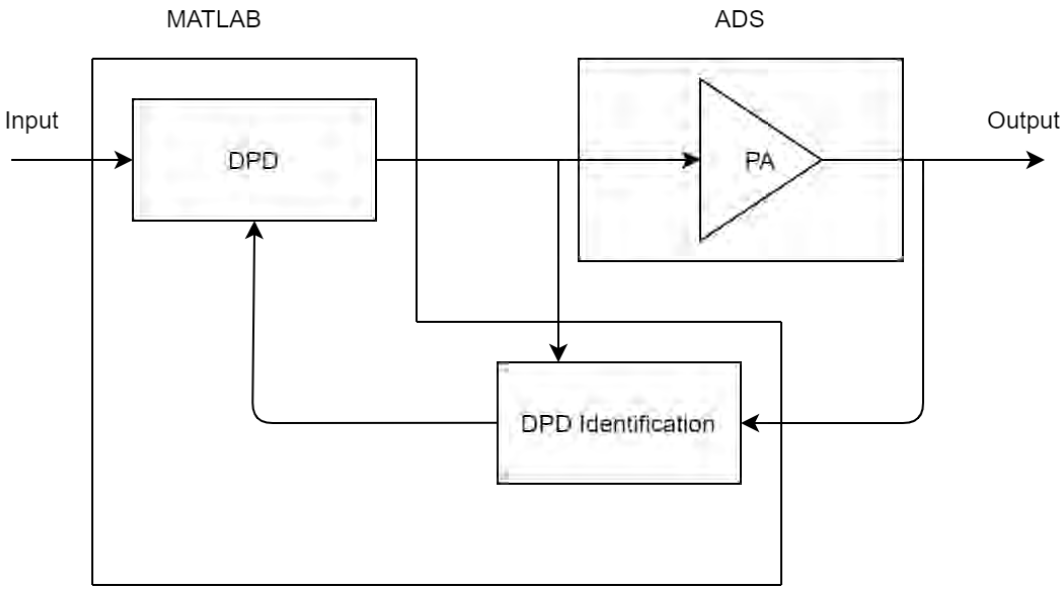

Figure 3.41: Linearization process using ADS and MATLAB

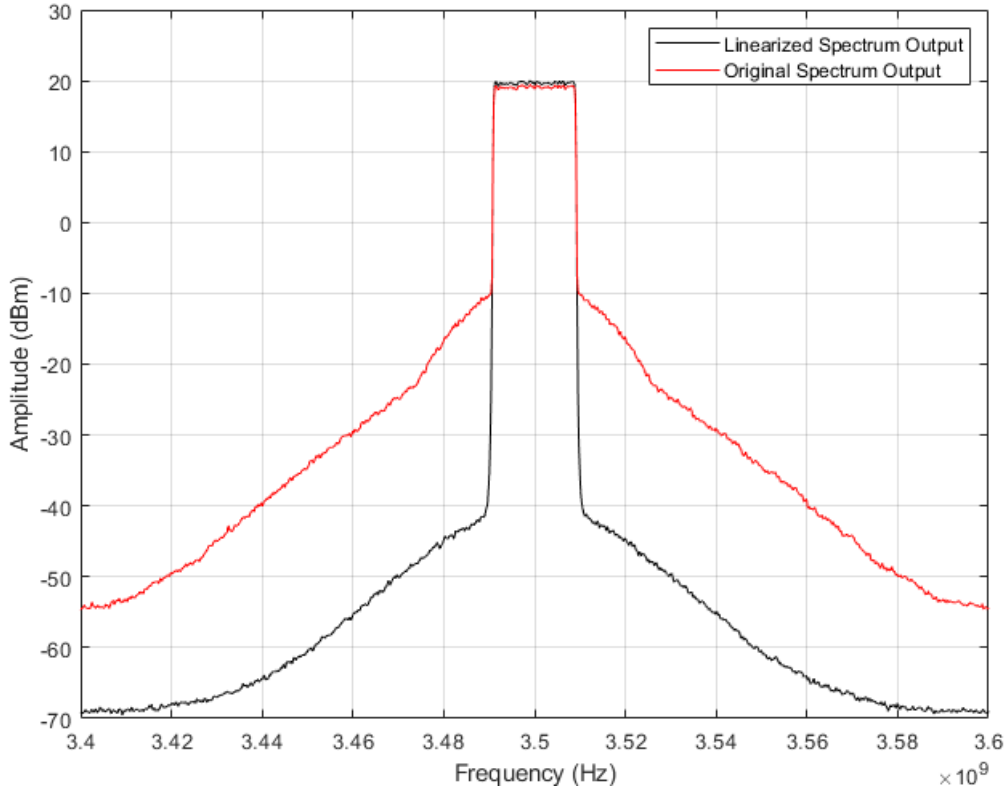

Figure 3.42: Doherty PA linearization results

Chapter 4. Layout Generation and Measurements

In this chapter, the process of layout design and generation of single-ended power amplifier and Doherty PA will be discussed. Then, the prototyping of the Doherty PA will be shown along with the measurement results of the fabricated PCB. Finally, linearization results will be reported.

4.1. Layout Design and EM Simulation of Single-ended Amplifier

The final layout design for the single-ended amplifier is shown in Figure 4.1. The layout design process was started from the optimized schematic as a basis, and then it was adjusted and further optimized to fit practical requirements and differences between schematic simulation and EM simulation. To illustrate this, the bias lines on the drain and gate end in a relatively large area, which was created to ease the soldering of the connections to DC sources and any bypass capacitors that may be needed. Furthermore, the lines on which the transistor gate and drain pads are to be soldered have to have similar widths to the leads of the transistor to ensure perfect electrical connection.

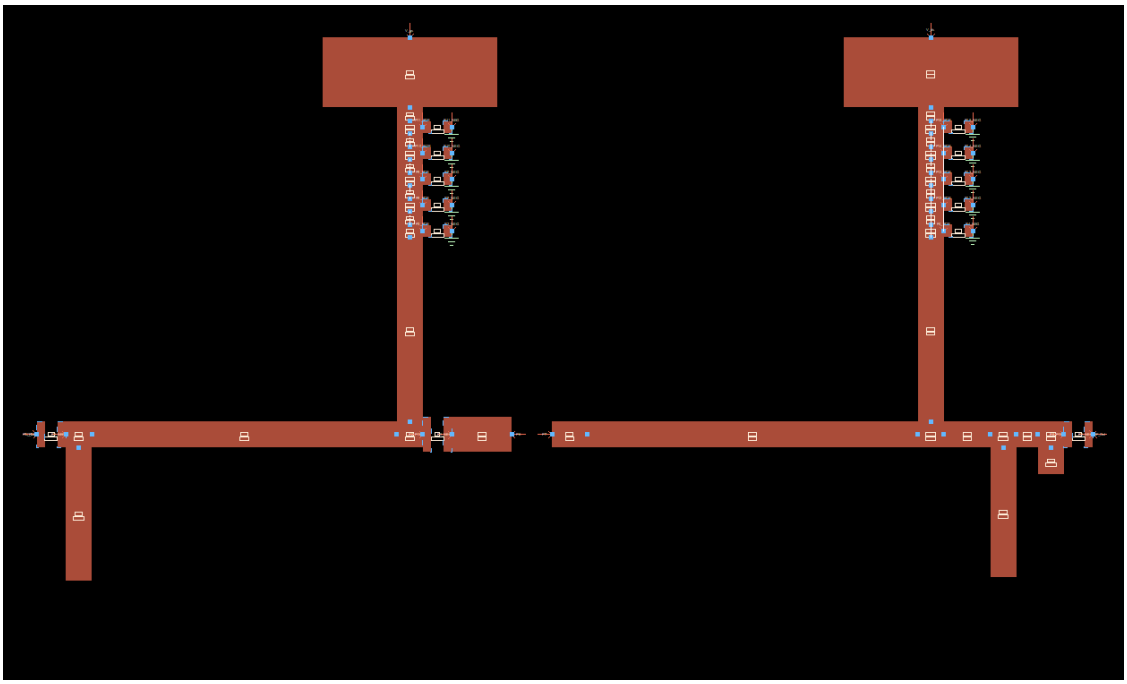

Figure 4.1: Final layout of single-ended PA

The optimization and EM simulation process was done using ADS' co-simulation workflow which is shown in Figure 4.2. The figure shows the layout being used as a component in the schematic simulation, which allows the user to connect the transistor and lumped elements to include them in the simulation, but the transmission lines will be simulated in ADS' EM simulator (Momentum). The left side of the figure shows the 1-tone input source connected to the amplifier while the right side shows its 50 Ω load. The same optimization tool used in the schematic simulation, was also used in the co-simulation, and therefore, the length of the transmission lines was adjusted to get the highest performance possible while using the more accurate simulator.

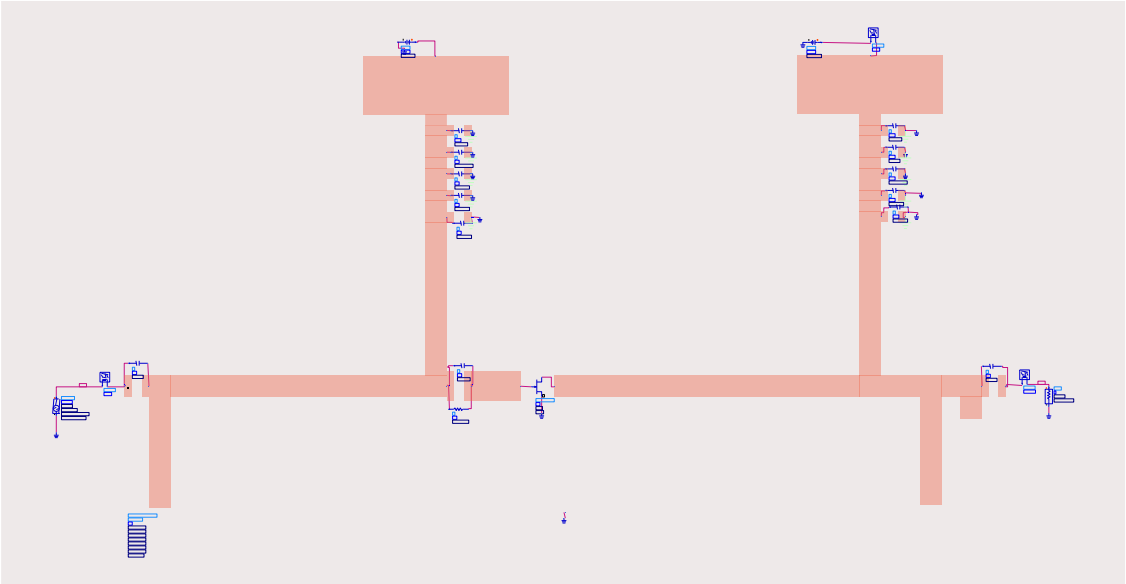

Figure 4.2: Co-simulation of single-ended PA

The results of optimization the EM simulated layout are shown in Figure 4.3, where it is seen that there is no performance loss, and the fabrication of the layout can be started with this finalized design.

4.2. Layout Design and EM Simulation of Doherty Amplifier

The process of designing the Doherty layout is heavily reliant on the finalized layout of the single-ended amplifier, since the same layout was used, along with the hybrid coupler and impedance transformers to result in a Doherty PA design. Therefore, no optimization was needed besides manually tweaking the phase offset lines at the output

of the carrier and peaking amplifiers to result in the desired load modulation behavior. The final layout designed is shown in Figure 4.4 and the results of the EM simulation are reported in Figure 4.5. The main layer is a conductive layer where the transmission lines and ground of the circuit is, and the green circles are vias, which are a vertical connection between the top layer where the components and the transmission lines are and the bottom layer representing the ground plane of the PCB. The main layer and VIA layer are shown in Figure 4.6. The bigger gray circles are cuts in the PCB to accommodate screws going from the top of the PCB to a conductive base to create a better electrical ground and mechanical support for the PCB which are shown in Figure 4.8 along with locations of passive components leads to prepare them for soldering. The middle gray rectangle is a cut in the PCB for the transistors to sit in.

4.2.1. Doherty PA performance benchmarking. The performance of the designed amplifier relative to similar designs is discussed in this section. To keep the comparison as accurate and relevant as possible, amplifiers with the same transistor used will be considered. Table 4.1 shows the performance of the proposed design relative to other works using the same transistors and about the same frequency range, in terms of gain and efficiency at both peaks of efficiency, that is, back-off efficiency peak and peak-power efficiency peak. As illustrated in the table, this work performs competitively compared to other published works at this specific frequency range using the same transistor. The results reported for this work use the EM simulations results.

Table 4.1: Literature survey of similar designs

Work	Frequency	Gain	Efficiency
[28]	3.5 GHz	10 dB	40 to 50% drain
[3]	3.4 GHz	10 dB	55 to 70% drain
[25]	3.5 GHz	12 dB	62 to 75% drain
[29]	2.4 GHz	14 dB	50 to 70% drain
[30]	2.14 GHz	12 dB	55 to 60% PAE
[31]	3.1-3.6 GHz	12 dB	60 to 70% drain
This work	3.5 GHz	12.5 dB	52 to 70% drain

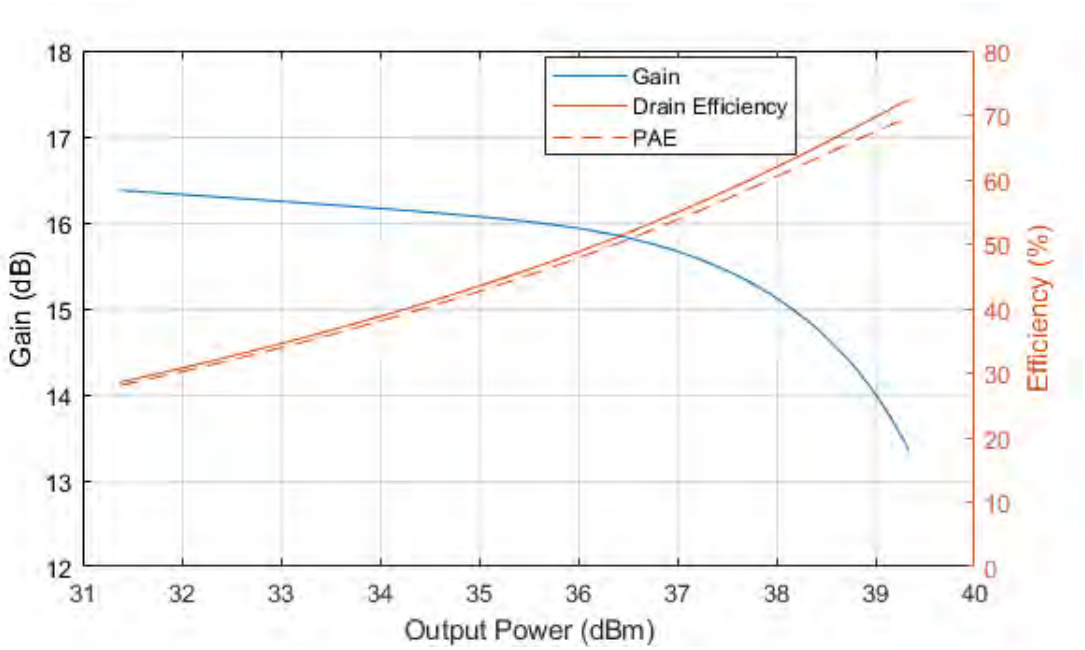

Figure 4.3: Gain and PAE of single-ended PA EM simulated

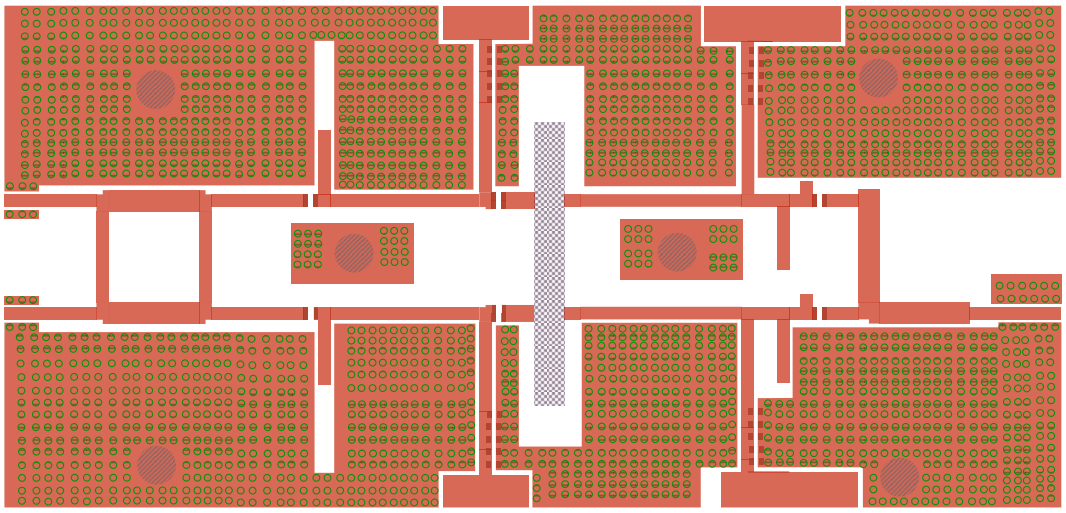

Figure 4.4: Doherty PA final layout

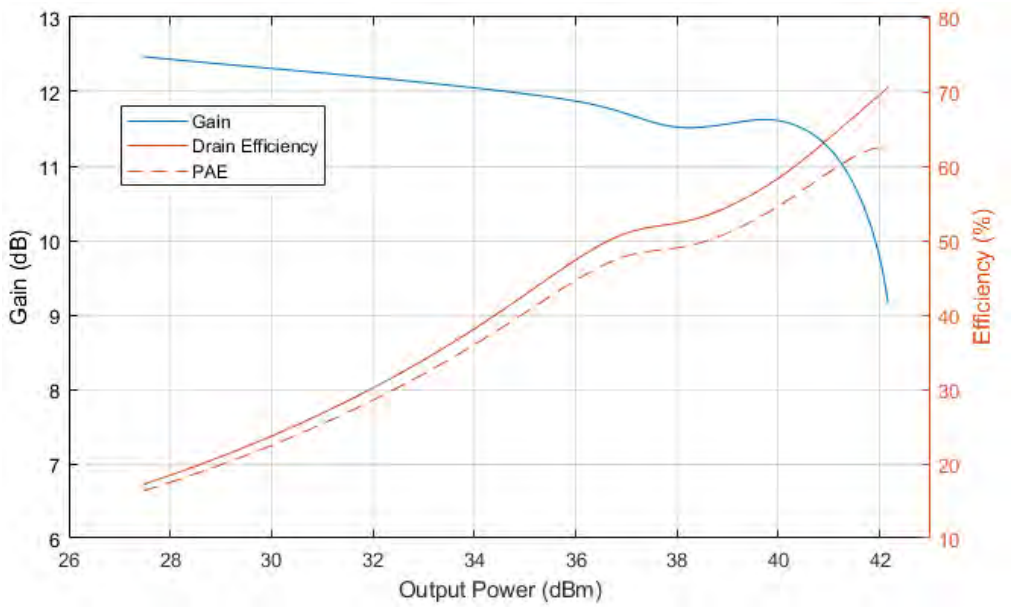

Figure 4.5: EM simulation results for Doherty PA

4.2.2. Measurement setup and testing. The measurement setup used in the testing is mainly made of the Anritsu MS2830A. The equipment has both a spectrum and a vector signal analyzer built in, with a vector signal generator all in one box. The frequency range of the signal analyzer goes up to 6 GHz and its analysis bandwidth is 125 MHz. All of this contributes to a capable measurement setup able to characterize and test power amplifiers and other RF components. The measurement setup block diagram is shown in Figure 4.7. The signal is generated from the vector signal generator into the amplifier (the signal data itself can be generated by MATLAB or ADS), and then retrieved at the input of the signal analyzer to be digitized and stored in I/Q format.

In order to automate the tedious process of setting the signal analyzer up with the correct settings and retrieving the digitized file through the LAN network to the PC, a MATLAB script was created using the VISA command system by National Instruments. As long as both the PC and the signal analyzer are connected to the network, commands and files can be shared between them to reduce the time it usually takes to upload files and retrieve them which is crucial in experiments with a lot of variations such as power, frequency, and bandwidth.

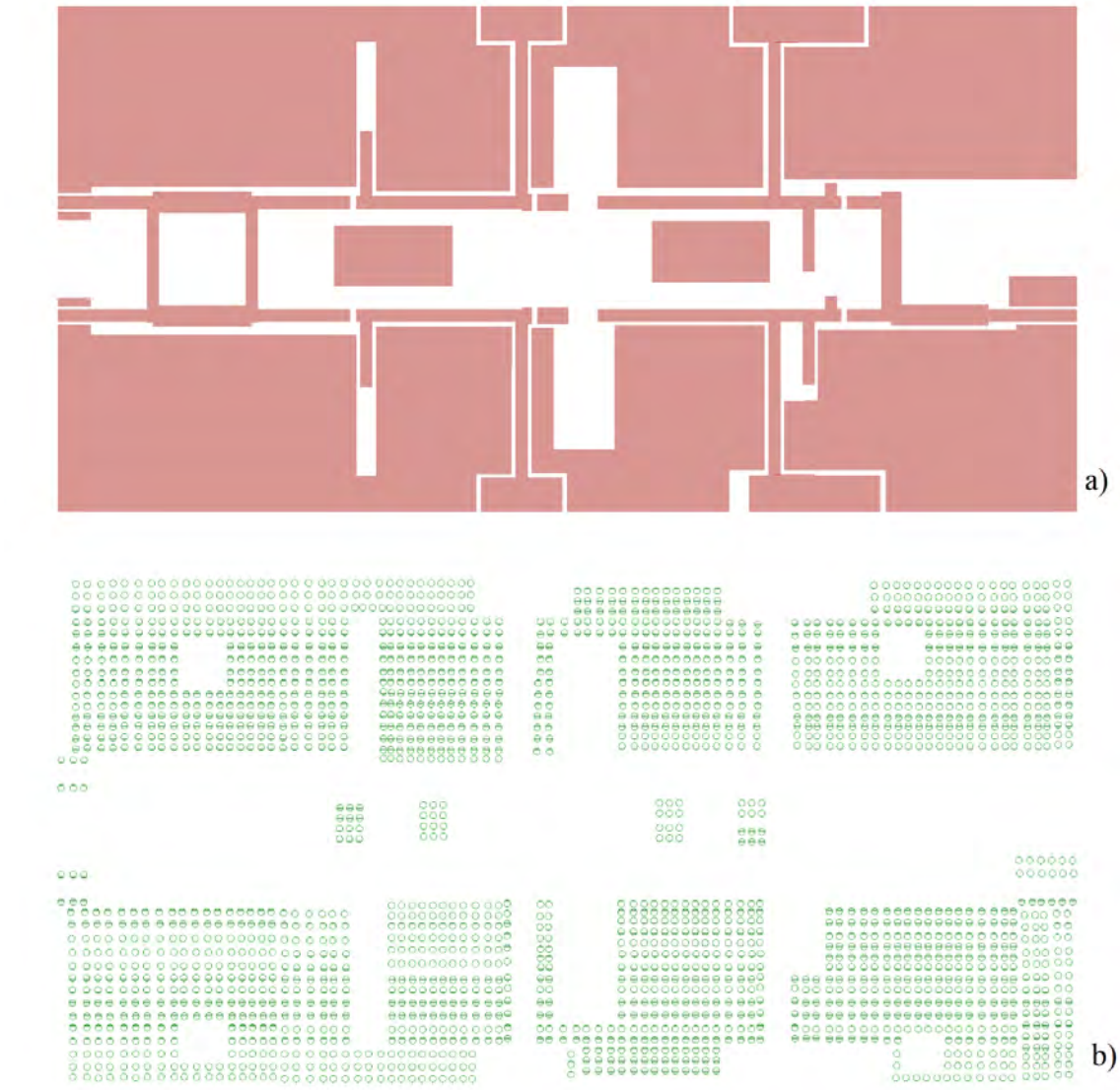

Figure 4.6: Doherty PA final layout a) Top layer b) VIA layer

Figure 4.7: Measurement setup block diagram

4.3. Measurement Results of PCB

After fabricating the PCB and soldering the passive components (capacitors and resistors), and transistors, the PCB was fastened to a heatsink to dissipate the heat generated by two 10 watts transistors. The input and output of the PCB are connected

to 50 Ω SMA connectors, and the isolated port of the hybrid coupler is terminated with a 50 Ω load. The fabricated PCB of the Doherty PA is shown in Figure 4.9.

Before testing the Doherty PA, the input power to the PA must be enough to drive the amplifier through the whole dynamic range up to saturation at 43 dBm (20 watts). Since the amplifier is expected to have a maximum gain of 13 dB, 30 dBm of input power is needed for testing. However, the signal generator can generate a maximum of 15 dBm. Therefore, driver amplifiers are used to increase the power level to appropriate levels. The drivers available to use are Mini Circuits ZHL-42+, and Cree CGH40006P. The first driver is used as a gain block, with a gain of 38 dB and 1 dB compression point of 30 dBm. The second driver, having a gain of 12 dB, is used as a power block, where it stays relatively linear up to 38 dBm output power. The setup block diagram is shown in Figure 4.10. Furthermore, the drivers were characterized in order to de-embed their effects from the measurements of the Doherty PA and are shown in Figure 4.11.

4.3.1. CW measurements. With the information about the drivers' response characterized, in addition to the output attenuators and cables losses, the power input to the Doherty PA, and output power can be measured accurately. The first set of measurement is CW measurements to characterize the amplifier. The results of these measurements are depicted in Figure 4.12. The CW frequency was set to 3.45 GHz, as it is the frequency that was found to result in the best efficiency and gain values. Such variance between simulation results and measurements is expected due to inaccuracies in the transistor model at certain bias conditions, and requires revisions to the PCB design to correct for.

4.3.2. Modulated signal measurements. A QAM-4 signal was generated with 20M symbols per second, which corresponds to 20 MHz of bandwidth. The output spectrum of the Doherty PA is reported in Figure 4.13. The amplifier passed the emission mask as specified by the ITU for this specific output power. The mask superimposed on the spectrum is shown in Figure 4.14. The amplifier’s efficiency at peak power with this modulated signal was found to be 43%, and the error vector magnitude (EVM) to be 0.9% which shows perfect linearity of the amplifier.

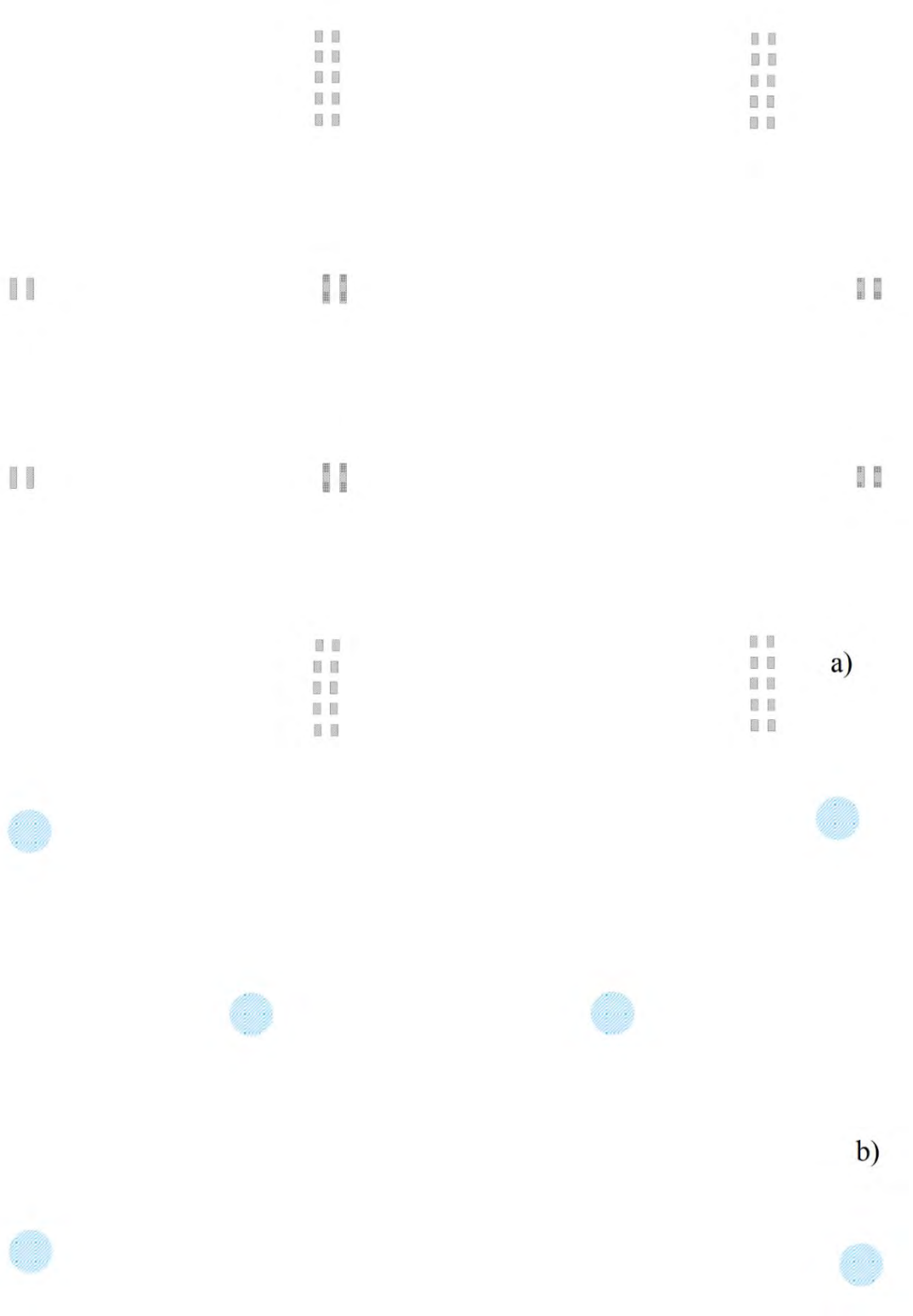

Figure 4.8: Doherty PA final layout a) Pastemask layer b) PCB screws layer

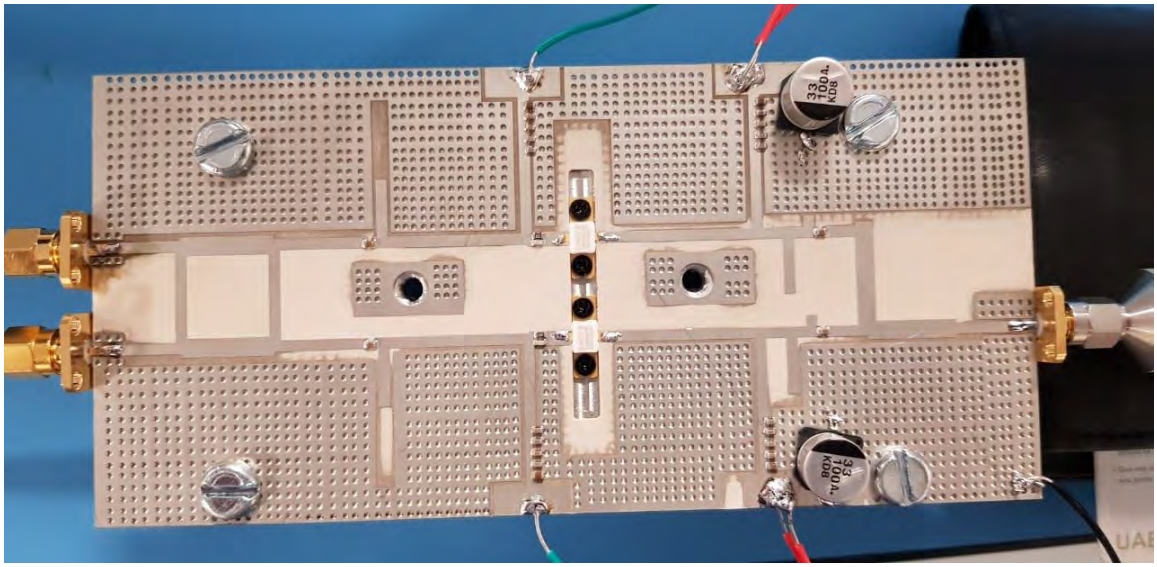

Figure 4.9: The fabricated Doherty PA PCB

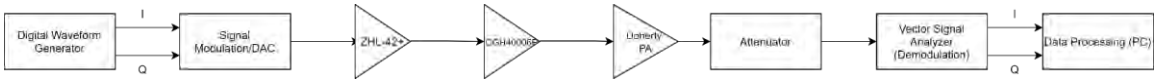

Figure 4.10: Measurement setup for Doherty PA characterization

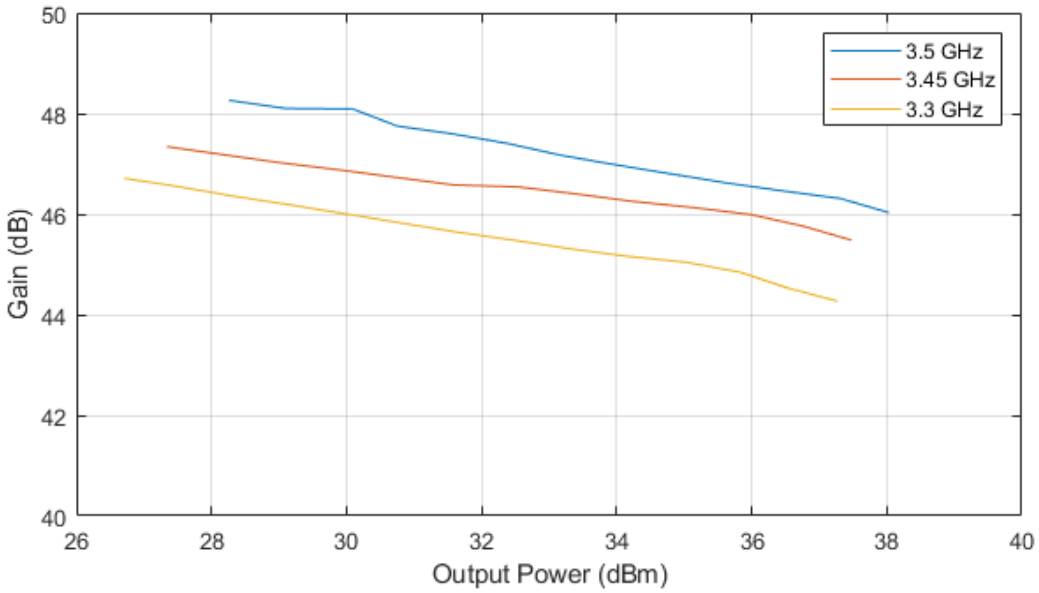

Figure 4.11: Gain characteristics of drivers

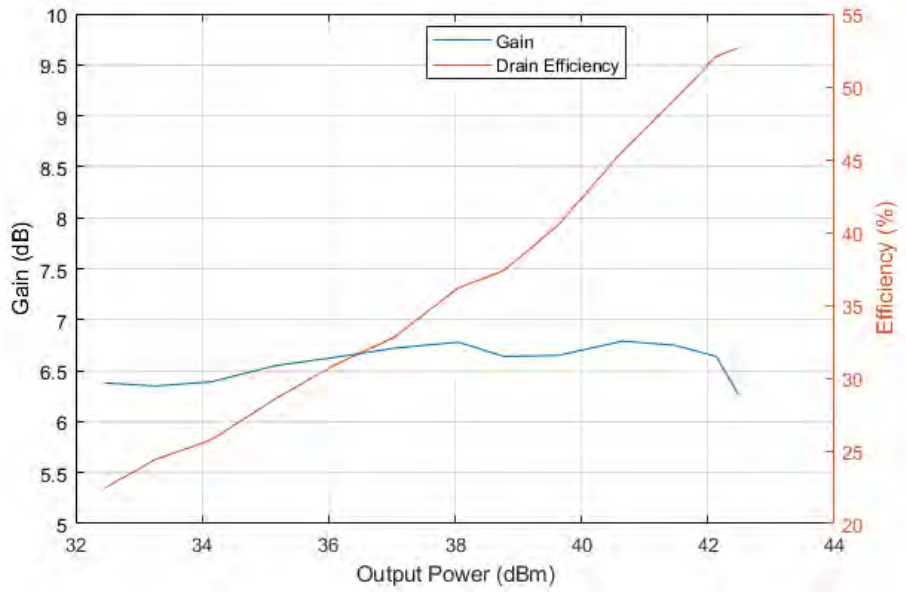

Figure 4.12: CW measurements of Doherty PA

In order to further enhance the efficiency that can be obtained from the design Doherty power amplifier while meeting the linearity requirements, the next chapter will discuss the use of a low complexity digital predistortion algorithm suitable for satellite applications which will allow the designed Doherty amplifier to operate at higher output power and thus achieve higher efficiency while meeting the linearity requirements

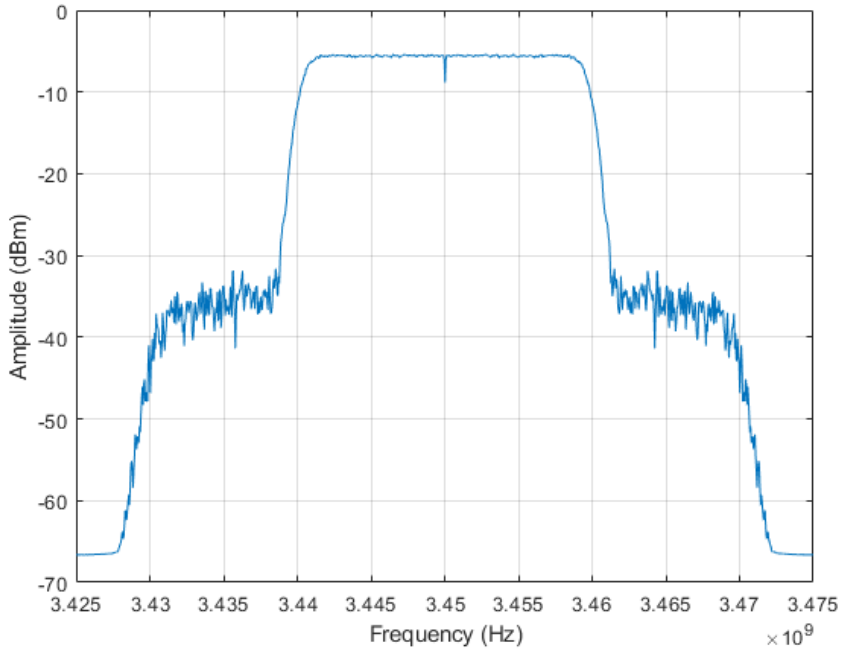

Figure 4.13: Output spectrum of Doherty PA

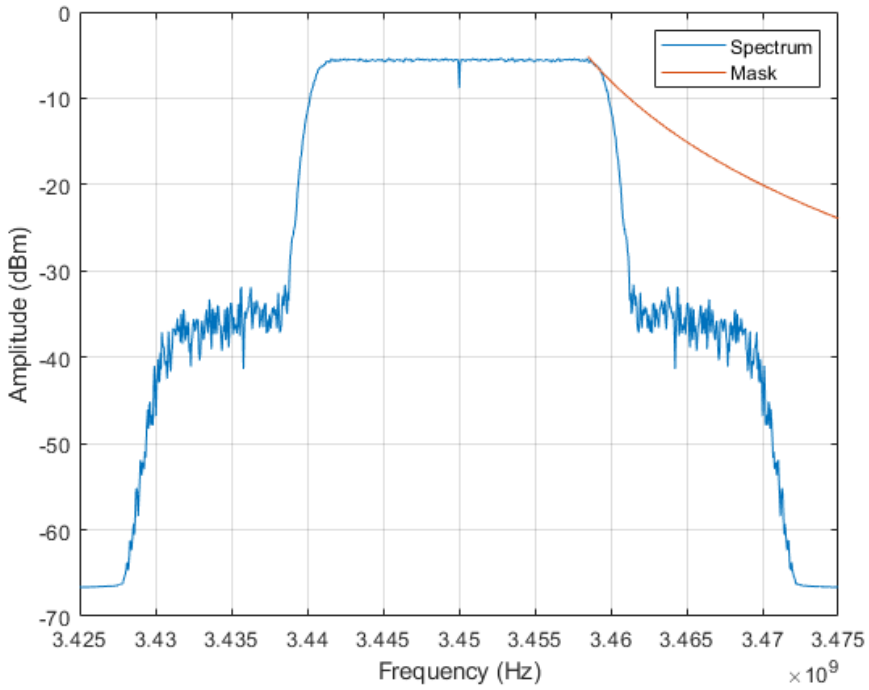

Figure 4.14: Emission mask on Doherty PA spectrum

Chapter 5. Enhancements of Doherty PA Prototype

In this chapter, two enhancements to the designed Doherty PA are investigated. First, the use of a linearization technique to enhance the efficiency-linearity trade-off is presented. Then, a size reduction of the designed power amplifier is performed by using a substrate having a higher dielectric constant.

5.1. Hybrid Look-up-table Model for Doherty PA Linearization

An improvement over the conventional NLUT model was developed in this work which is the Hybrid Look-up Table Model (HLT) [24]. The model follows a similar structure to the PTNTB as shown in Figure 5.1. The model consists of a memoryless LUT and an NLUT in parallel, and a comparator that makes the decision which block to use depending on the power level. This is based on the principle that memory effects are stronger in the low power region of the PA, while at high power, the PA exhibits mainly highly nonlinear behavior with less dominance of memory effects. Figure 5.2 shows the results of this model, with THR=0% case being the memoryless model acting alone, and THR=100%, being the NLUT model acting alone. THR in this case refers to threshold ratio, defined as the ratio between the threshold to maximum possible input magnitude. The figure shows very similar performance in the mid-region of the threshold value, which translates to more than 80% of size reduction. As a benchmark, the memory polynomial performance, expressed in terms of normalized mean-squared error (NMSE), is reported to be -32 dB, while the HLUT of -27.5 dB. These results are obtained when 50% of the data is used for training.

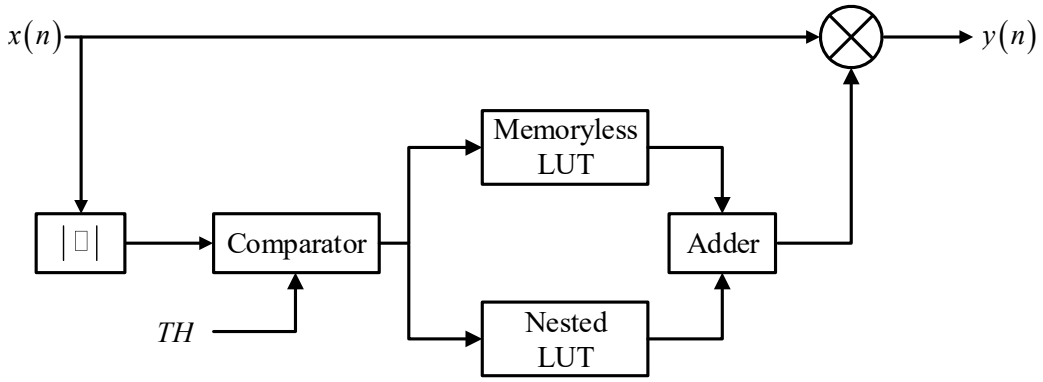

Figure 5.1: HLUT model block diagram

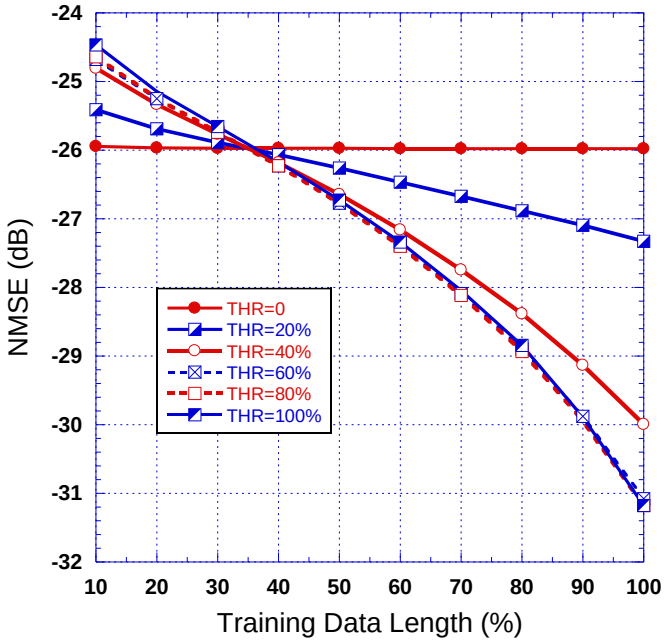

Figure 5.2: HLUT model performance

Furthermore, a bandwidth scalable architecture of the HLUT was also proposed. In this model, only the NLUT model is to be updated, keeping the LUT unchanged. The principle of this architecture is that the memoryless representation of the signal is more accurate at signals with lower bandwidths, therefore, there is no need to reidentify the LUT if the bandwidth increases. In fact, it was found that if the LUT is identified with a signal with lower bandwidth, more accurate results can be achieved as illustrated in Figure 5.3.

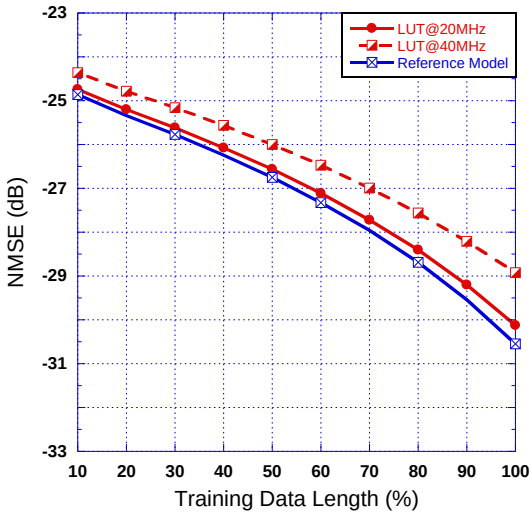

Figure 5.3: Bandwidth scalability of the HLUT model

5.2. Linearization of Doherty Amplifier

Different digital predistortion methods were tested on the fabricated Doherty PA, including a memoryless look-up table, a nested look-up table, a hybrid nested look-up table, and a memory polynomial model. The results of these models are reported in Figure 5.4. This figure shows an improvement in linearity and is quantified in

Table 5.1 which shows 5 dBc of improvement in ACLR for the memory polynomial model. The NLUT model comes close to the MP DPD with a difference of 0.6 dBc. The HLUT performance is shown to be robust and is very close to the NLUT performance but with the HLUT model being 26% the size of the full NLUT model.

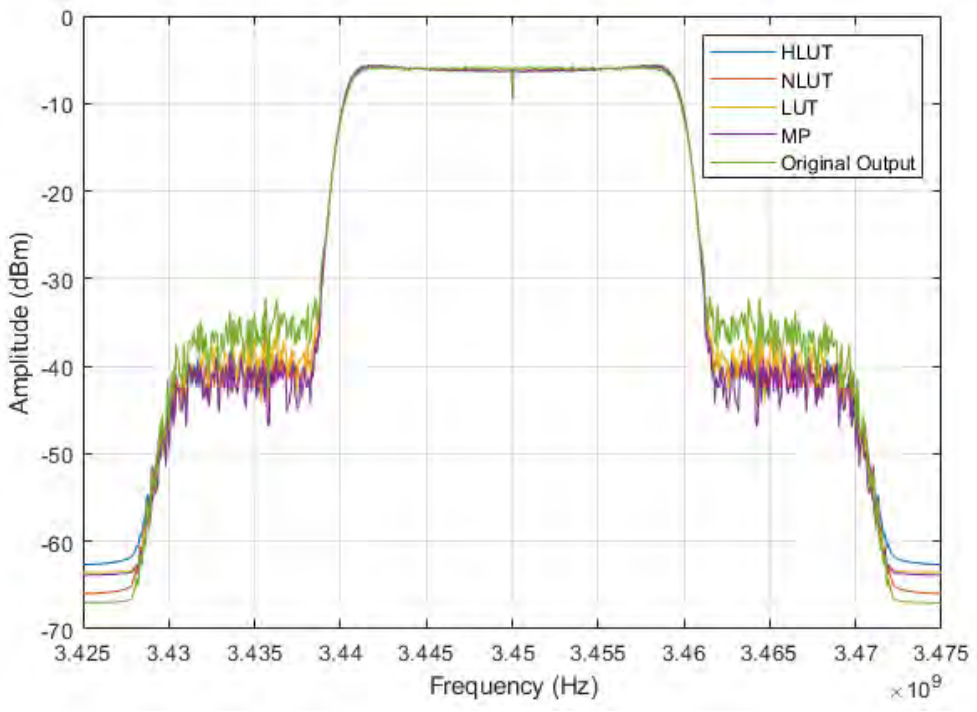

Figure 5.4: DPD results of Doherty PA

Table 5.1: ACLR measurements of linearized Doherty PA

Model	ACLR (Upper)
Without DPD	-31.40 dBc
LUT	-34.67 dBc
Memory Polynomial	-36.64 dBc
NLUT	-36.0 dBc
HLUT	-35.76 dBc

5.3. Doherty PA Size Reduction for CubeSat Operation

The amplifier is designed to fit in a CubeSat 1U system, which is 10x10x10 cm. However, as shown in Figure 5.5, the amplifier board is sized 15.7x7.5 cm, which clearly does not fit in the smallest CubeSat. Therefore, shrinking the amplifier board to a more reasonable size was done. It was not possible to manufacture this size-reduced board due to the unavailability of suitable substrate in the manufacturing facility used for this work.

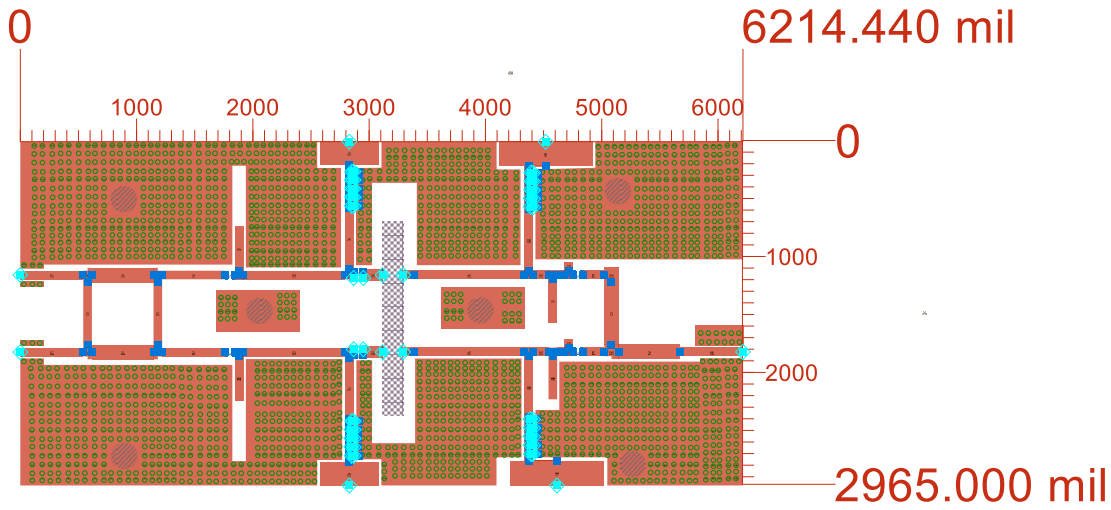

Figure 5.5: Doherty PA dimensions

The method of shrinking was the usage of a higher dielectric constant substrate, specifically the Rogers RO3010 with the parameters shown in Table 5.2. The dielectric constant of this substrate is 11.2, which is a substantial increase over the RO3003's constant of 3.0.

Table 5.2: Rogers RO3010 parameters

Substrate model	Rogers RO3010
Dielectric constant (ε_r)	11.2
Dissipation factor	0.0022
Substrate thickness	25 mils (0.64 mm)
Copper cladding	17 µm

The new board after translating the original board to the new substrate, with optimization done to match the performance of the previous board is shown in Figure 5.6. The new size came down to 7.9x5.3 cm which will comfortably sit in a 1U CubeSat.

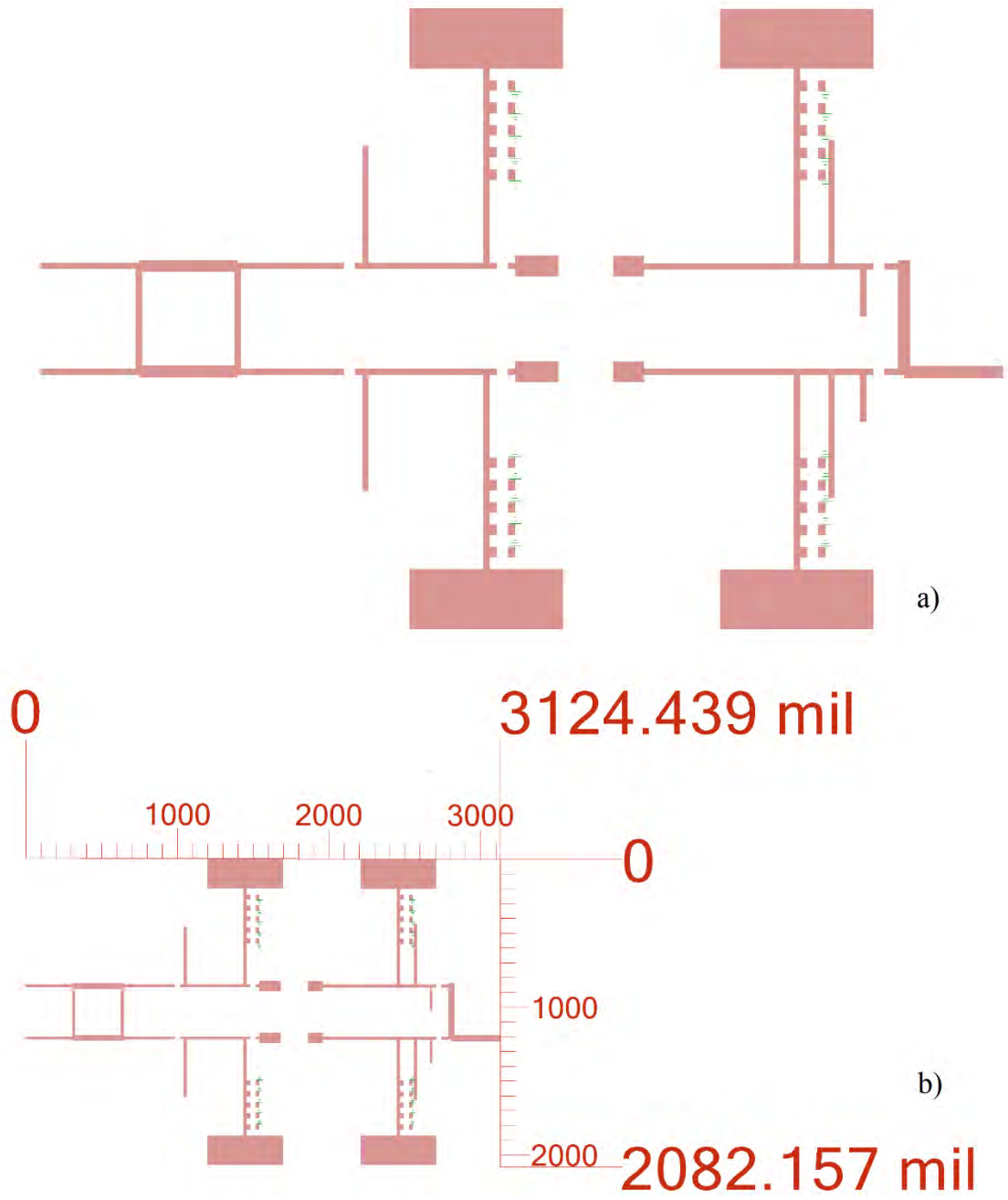

Figure 5.6: Doherty PA dimension reduction a) Original design b) Reduced size design

The EM simulated performance of the reduced size Doherty PA is shown in

Figure 5.7, which shows slightly worse performance in terms of efficiency (5% decrease in peak PAE) when compared to the previous design.

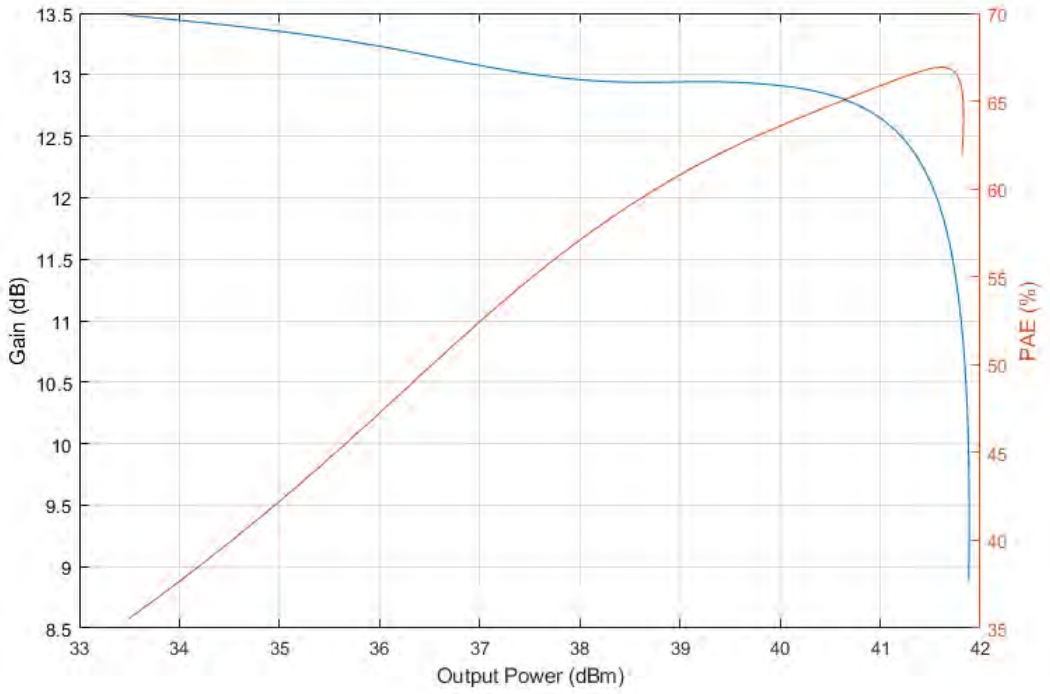

Figure 5.7: Simulated gain and PAE performances of the reduced size Doherty PA

Chapter 6. Conclusion

In conclusion, this thesis explored the existing literature on satellites, and power amplification systems for satellite applications. The satellite industry is in more demand than ever for more efficient satellites as they are getting smaller, and with it, the power sources are also getting smaller. Therefore, more efficient power amplification systems are very important, as the high-power amplification section of the satellite consumes most of the power and is usually the least efficient subsystem of the satellite. A power amplification system was designed and fabricated with high efficiency in mind, with electromagnetic simulation results having high drain efficiency of 52% to 70% that is comparable to previous solutions of 50% to 70% with 6 dB of output power backoff. Furthermore, the designed system was based on a previous work in the literature, which was improved in simulations by the adaptive uneven power drive technique. The improvement in the backoff power range was found to be 5%. The amplifier's measurement reported 6.5 dB of gain and efficiency of 35% to 52%. The system was tested using modulated signals to ensure the performance is acceptable and passes out-of-band emission requirements for satellite transmitter according to the ITU recommendations. The amplifier was then re-designed with size reduction in mind for satellite applications. Finally, the HLUT model was tested on the amplifier, and benchmarked against similar models and the full NLUT model and showed competitive results, resulting in nearly identical performance to the full NLUT while only being 26% of the size.

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Vita

Ahmad Dalbah was born in 1996, in Amman, Jordan. He received his primary and secondary education in Dubai, UAE. He received his B.Sc. degree in Electrical Engineering from the American University of Sharjah in 2018. In January 2019, he joined the Electrical Engineering master's program in the American University of Sharjah as a graduate teaching assistant and a graduate research assistant. During his master's study, he authored 2 papers which were published in different IEEE journals, and presented a paper in a local conference. His research interests are in wireless transceivers design, and DSP methods for nonlinear PA linearization applications.