EXTENDED BEHAVIORAL MODELING OF FET AND LATTICE-MISMATCHED HEMT DEVICES

by

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Dedication

To all humanity

Abstract

This study presents an improved large signal model that can be used for High Electron Mobility Transistors (HEMTs) and Field Effect Transistors (FETs) using measurement-based behavioral modeling techniques. The steps for accurate large and small signal modeling for transistor are also discussed. The proposed DC model is based on the Fager model since it compensates between the number of model's parameters and accuracy. The objective is to increase the accuracy of the drain-source current model with respect to any change in gate-source or drain-source voltages. Also, the objective of this thesis work is to extend the improved DC model to account for soft breakdown and kink effect found in some variants of HEMT devices. A hybrid Newtons-Genetic algorithm is used in order to determine the unknown parameters in the developed model. In addition to accurate modeling of a transistor's DC characteristics, the complete large signal model is modeled using behavioral modeling techniques based on multi-bias s-parameter measurements. The targeted elements to be modeled in the complete large signal model are parasitic capacitances, parasitic inductances and parasitic resistances. The way that the complete model is performed is by using a hybrid multi-objective optimization technique (Non Dominated Sorting Genetic Algorithm II) and local minimum search (multi-variable Newton's method). Finally, the results of DC modeling and multi-bias s-parameters modeling are presented, and three device modeling recommendations are discussed.

Search terms– High Electron Mobility Transistor; Field Effect Transistors; Behavioral Modeling; Optimization; Genetic Algorithm; Non Dominated Sorting Genetic Algorithms; multi-variable Newton's Method; Kink Effect; Soft Breakdown; Intrinsic Elements; Extrinsic Elements; Parasitic Extraction; DC Model; S-Parameters; Local Minimum Search; Global Optimization.

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List of Abbreviations

NSGA-II	Non Dominated Sorting Genetic Algorithm II
GA	Genetic Algorithm
LMS	Local Minimum Search
HEMT	High Electron Mobility Transistor
FET	Field Effect Transistor
pHEMT	Pseudomorphic High Electron Mobility Transistor
mHEMT	Metamorphic High Electron Mobility Transistor
C_{gs}	gate-source capacitance
C_{gd}	gate-drain capacitance
C_{ds}	drain-source capacitance
R_g	gate terminal resistance
R_d	drain terminal resistance
R_s	source terminal resistance
L_s	source terminal inductance
L_g	gate terminal inductance
L_d	drain terminal inductance
g_m	transconductance
dg_m	first derivative of transconductance
G_{ds}	output conductance
I-V	current-voltage characteristics
VNA	Vector Network Analyzers
LSNA	Large Signal Network Analyzer
PSO	Particle Swarm Optimization
CAD	Computer Aided Design

Chapter 1: Device Modeling General Background Information

The need for transistor models with high accuracy and reduced model complexity has increased. The reason is that tighter system architectures' specifications and standards are required. In many circuits and amplifier configurations, the gain can be a function of transconductance and the intermodulation products are affected by the derivatives of the transconductance. The non-linearity terms in drain current can be described as a function of transconductance, g_m, and output conductance, G_{ds} as shown in equation 1 [1].

$$i_{DS} = G_{ds}v_{DS} + \frac{G'_{ds}v_{DS}^2}{2} + \frac{G''_{ds}v_{DS}^3}{6} + g_m v_{GS} + \frac{g'_m v_{GS}^2}{2} + \frac{g''_m v_{GS}^3}{6} \quad (1)$$

As a result, a transistor model with more accurate transconductance and output conductance representations can lead to more accurate DC, AC and intermodulation products simulation of amplifier circuits. In the case of an inaccurate model, constricted requirements for gain and intermodulation products can be difficult to achieve in the amplifier's simulation process. Another impact of inaccurate models is when an engineer designs and tunes his circuit in a Computer Aided Design (CAD) tool to meet the desired specifications and sends out the circuit for fabrication. The result might be a fabricated design that does not meet the required specifications and does not match the results obtained from the simulation process. Therefore, design efforts and fabrication funding to implement the design are wasted [2].

Models that are used in circuit simulators are called *Compact* models which are transistor's equivalent circuit. Different compact models have various error performances. The error performance of a model depends on how it approaches transistors' phenomena, and how many phenomena are considered in the model. For example, equation 2 shows a typical transistor equation that relates drain current to the square of the effective gate-source voltage.

$$i_{DS} = \frac{Mu * Cox * W}{2L} * (v_{GS} - V_T)^2 * (1 + \lambda * v_{DS}) \quad (2)$$

Equation 2 implies that the transconductance of the transistor is linear and directly proportional to gate-source voltage. However, this is only true for a finite range of input voltage. As a result, the model incorporating equation 2 is only

accurate for a finite range. To obtain an accurate transistor model, there are few a steps that should be taken into account for developing, testing and validating a model. The steps are summarized in Fig. 1.

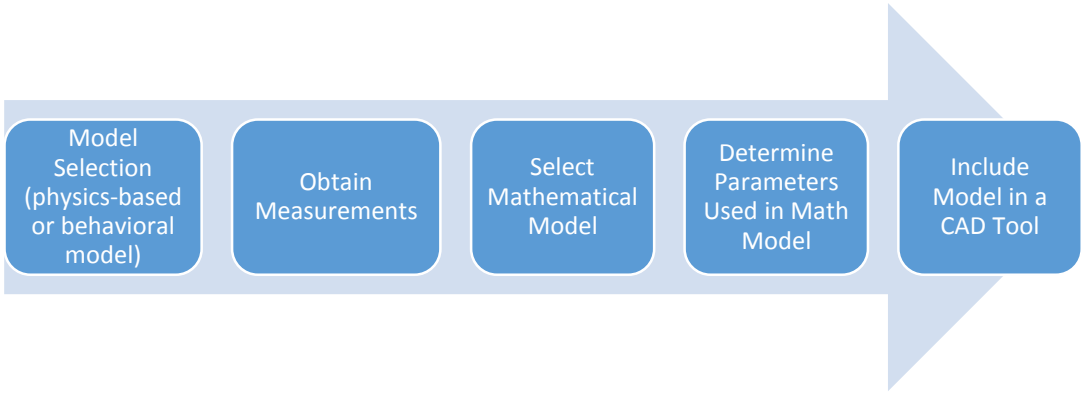

Fig. 1: Steps for obtaining a model

The first step in obtaining a model is to select a model type. There are two main types of transistor Compact models that can be implemented in CAD tools: physic-based models and measurement-based behavioral models. A physics-based model is one that utilizes a transistor's physics in order to develop a mathematical function that describes the measured data such as drain-source current, transconductance and output conductance. Also, a physics-based model is a model in which doping level, material type, carrier mobility, structure, layers spacing, channel length modulation and geometric dimensions are taken into consideration for real representation of the transistor's behavior. Sometimes, simplifications are done to the mathematical expressions found in physics-based models in order to decrease simulation runtime. Simplification of the physics-based model is done by introducing non-physical parameters that indirectly represent physical phenomena. As a result, various measurements should be done in order to determine those non-physical parameters. This technique is called Parameter Extraction. Depending on the type and role of the introduced parameters, measurements should be done in the following domains of the transistor's behavior: current-voltage characteristics, capacitance-voltage characteristics and S-parameters. After obtaining the measurements, the parameters are determined and related to the measured values using optimization techniques such as: Particle Swarm Optimization, Genetic Algorithm and Advanced Neural Networks. However, we must take into consideration that a more complex transistor's behavior requires more parameters to be determined from measurements

data. As a result, large number of parameters will be utilized, such as level 4 models, so the optimization process is made more complex. The complexity arises from the fact that determining hundreds of parameters using optimization techniques is a CPU-extensive task. The reason is the population size in an optimization process is greater than and directly proportional to the number of parameters used in a model. Also, in order to have a reliable optimization solution, a larger population size must be used [3]. This optimization requires multiple CPU's connected in parallel and more RAM sizes, which might not be available at all times, to account for bigger matrices.

A measurement-based behavioral model is a model that directly maps the measured data to a function that is chosen such that the function mimics the behavior of the data over which it is mapped to. The chosen function representation should highly represent the behavior of drain-source current, and it should be highly representative when the derivative of this function is taken with respect to gate-source voltage or drain-source voltage to yield accurate transconductance and output conductance, respectively. In contrast to the physics-based model, a measurement-based behavioral model utilizes the location of peak transconductance, transconductance elongation beyond peak transconductance, location of current compression point, channel length modulation, and shift in knee voltage with respect to applied gate voltage to behaviorally describe the transistor's operation and building up the drain-source current equation (this will be heavily discussed in the Literature Review section). In addition, most parameters in a behavioral model are non-physical parameters that indirectly relate to physical phenomena. For example, equation 3 shows a behavioral drain-source current equation.

$$i_{DS} = K * (v_{GS} - V_T)^2 * (1 + \lambda * v_{ds}) * \tanh(\alpha * v_{ds}) \quad (3)$$

This model is called the Curtice model and will be discussed in upcoming sections. It is seen from the above equation that the model parameters are K, λ and α which represent peak current, channel length modulation term and knee-voltage sharpness parameter, respectively. Those parameters will be obtained using an optimization technique to map the current, I_{ds}, shown in equation 3 to the measured data. A noticeable behavioral term chosen in equation 3 is the tanh function that does not directly reflect a physical meaning of a transistor operation. In fact, the hyperbolic-tan function is used in order to correct for the values of the drain current around the knee

voltage. As a result, a smooth transition between triode and saturation regions is obtained with higher accuracy. The main advantage of behavioral modeling is reduced model complexity in conjunction with accurate modeling of the transistor under test. However, the main disadvantage in many behavioral models is the lack of geometric scalability. In other words, once the models' parameters are obtained from an optimization process, those parameters will only be representative for a single value of transistor's *(W/L)* ratio and single channel length value since there are no input arguments for the transistor's width and length. Also, a variation of the transistor's channel length will cause a change in some parameter of the model already obtained from model optimization such as the channel length modulation parameter which is inversely related to the transistor's channel length.

In this thesis work, the accuracy of drain current's derivatives will be improved. Also, a DC model for Kink Effect and Soft Breakdown found in some variants of High Electron Mobility transistors (HEMT's) will be developed. In order to have a comprehensive model, a large signal model incorporating DC model should be developed. In the literature, there are excellent models that can have high accuracy in terms of representing measured s-parameters and as a result the parasitic element of a device at high frequencies. Different algorithms were established in order to come up with a modeling flow for determining the parasitic element of the device. For this research work, an efficient and hybrid multi-objective function optimization algorithm is used in order to determine the parasitic elements of an NMOS device.

In this thesis report, general physics concepts of heterostructure devices are discussed in Chapter 2. In Chapter 3, various techniques for developing a large signal model for HEMT's and Field Effect Transistors (FET's) are discussed. In Chapter 4, the developed model for Kink Effect and Soft Breakdown for a HEMT device is discussed. Also, Chapter 4 discusses how an efficient and hybrid multi-objective function optimization algorithm is used in order to reduce the number of steps taken to develop a large signal mode.

Chapter 2: General Physics Concepts of Heterostructure Devices

Many semiconductor devices have emerged since vacuum tube devices were used in various designs. Silicon material today and in the past is heavily used in integrated circuits. However, different materials have emerged, and they are providing advantages over silicon such as gallium arsenide, GaAs. The emerging materials allow for higher frequency of operation relative to earlier materials. Also, materials used today to develop solid-state devices cannot yet achieve really high power (i.e. in the order of hundreds of watts).

Vacuum tubes are still used for high power applications such high power transmitters [4]. The reason is that devices today are limited in terms of DC bias points that can be applied to their terminals. Furthermore, limited breakdown voltages noticed in the devices will consequently limit the high RF power operation. It can be considered that to achieve high DC and RF currents in the current devices, larger devices may be deployed. However, increasing the device area will introduce further capacitance that will limit high frequency operation. Also, more losses will be introduced that will limit power efficiency.

Further research was done to improve the breakdown voltages by obtaining different device structures and materials. It is proven that wide bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN) can achieve better high power performance as compared to silicon for example. The new structure for transistors is heterostructure-based. This kind of structure along with materials used can help achieve high power and linearity [4].

Even though high power and linearity can be obtaining by utilizing heterostructure-based transistors, there are several physical phenomena that can provide some sort of limitations to device operation due to materials used (which will be discussed later in the chapter). In this chapter, semiconductor material properties will be discussed as well as the physics of heterostructure-based transistors.

2.1 Semiconductor Materials

Generally, the behavior and performance of electronic devices are dependent on various parameters such as the thermal, electronic and mechanical properties of

material used to build up the structure for those devices [5]. Each material has its unique velocity-field characteristics which will affect carrier mobility as an example. A vacuum tube based device shows superior "material" performance as compared to solid state devices used today since electron flow does not encounter scattering. However, materials and different solid-state structures are being improved for better DC and RF handling. Table 1 shows a summary of semiconductor material properties for different materials:

Material	E_g (eV)	ε_r	K(W/°K-cm)	E_c (V/m)
Vacuum	-	1	-	-
Si	1.12	11.9	1.5	3×10^5
GaAs	1.43	12.5	0.54	4×10^5
InP	1.34	12.4	0.67	4.5×10^5
3C-SiC	2.3	9.7	4	1.8×10^6
4H-SiC	3.2	10.0	4	3.5×10^6
6H-SiC	2.86	10.0	4	3.8×10^6
GaN	3.4	9.5	1.3	2×10^6
Diamond	5.6	5.5	20-30	5×10^6

Table 1: Summary of semiconductor properties [5]

The dream and ultimately desirable semiconductor materials should show large bandgap energy (E_g), low dielectric constant (ε_r), high thermal conductivity (K) and high critical electric field (E_c) for breakdown. The reasoning for the importance of each desired property is listed below [4]:

1) Bandgap energy: higher bandgap energy allows a material to handle high electric fields due to applied voltages at the terminals of the device.
2) Dielectric constant: a dielectric constant shows the ability of a material to store electrical energy when an electric field is applied. When low dielectric constant is used, the area of the device can be increased for specified impedance. As a result, higher RF current and power can be operated.

3) Thermal conductance: higher thermal conductivity for a material means that the device will be able to dissipate heat out of the device efficiently. In other words, the device cannot relatively accumulate heat.
4) Critical electric field: high critical electric field means that the device can handle a higher magnitude of applied electric field before breakdown and before the device gets permanent damage. This results in the ability of amplifiers to have higher output swing.

2.1.1 Velocity-electric field characteristics (v-E)

An electrical current can be defined as a function of charge density and transport velocity. As a result, the flow of current in an electrical circuit is directly dependent on the material used since each material has a unique v-E relation. In order to maximize DC and RF current in a circuit, a material with the highest carrier mobility and saturation velocity should be used. Fig. 2 shows v-E relation for different types of materials.

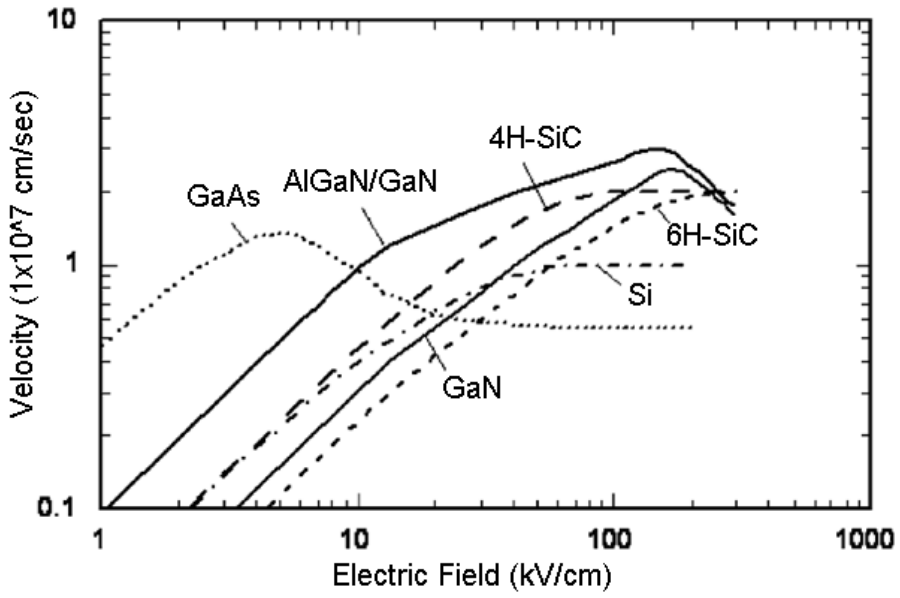

Fig. 2: v-E relation for several materials [5]

The v-E characteristics can be described by carrier mobility μ_n $\left(\frac{cm^2}{V.S}\right)$ which is the slope of the v-E curve. Furthermore, the saturation velocity $\left(\frac{cm}{S}\right)$ can be defined as the point at which further applied electric field cannot increase the carrier velocity. It can

be seen from Fig. 2 that silicon has low saturation velocity and low carrier velocity for high electric fields. Also, materials such as 4H-SiC and 6H-SiC achieve higher velocities than Si at high electric fields. GaN and AlGaN/GaN materials achieve higher saturation velocity and within a low band of electric field beyond which velocity will start to decrease. However, an attractive material such as GaAs shows high carrier velocity as compared to other materials at lower electric fields. This allows for high flow of DC and RF current at relatively lower applied voltages. Even though GaAs material has a high bandwidth of saturation current, the carrier velocity is lower as compared to materials in Fig. 2. As a result, prior knowledge of the design specifications of an electric circuit may require a specific material.

2.1.2 RF performance of different devices

Fig. 3 shows power performance versus frequency for various semiconductor devices. As shown in the figure, solid state devices can operate up to 100 GHz and less than 100W envelop [6]. Furthermore, it is shown in the figure that vacuum devices can be operated at a higher level of power and frequencies. The main reason for low power and frequency operation of solid state devices is due to lower bias voltages, low carrier velocity (which reduces mobility and current) and thermal limitations [4].

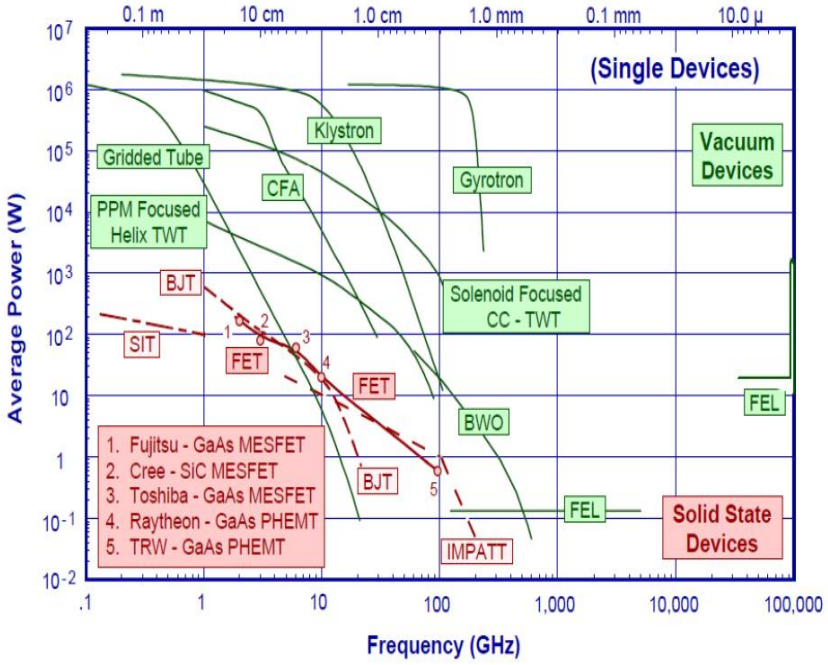

Fig. 3: Average power versus frequency for different devices [4]

Since each device has a unique structure and material used to build it, it will have a different power and frequency operation and limitations. Table 2 summarizes advantages and disadvantages for different types of devices [4].

Device (Material)	Merit	Drawback	Comment
MESFET (GaAs)	Matured technology, simple device	Max frequency operation below 20 GHz	Used in low noise and power application
HEMT (GaAs)	Matured technology, high frequency (i.e. 6 GHz [54]) operations, low noise figure	Needs negative voltage to switch off device, low output power at high frequencies	Most popular are the GaAs pHEMT devices
HEMT (InP)	High operating frequency (300 GHz – 3 THz [55]), lowest noise figure	Expensive technology	Applications limited to low-volume high-performance markets
HEMT (AlGaN/GaN)	Highest power limits, high operating temperatures, high breakdown voltage	Expensive technology	Commercially available at WiMax frequencies, used for power amplification at GHz frequencies
MESFET (SiC)	Highest power limits, high operating temperatures, high breakdown voltage	Expensive technology	Commercially available but limited to X-band, used for power amplification at GHz frequencies

Table 2: Dis/advantages of different devices [4]

2.2 Heterostructure-based Device General Physics Concepts

A heterostucture device consists mainly of two different materials each of which having different conduction and valence bands as shown in Fig. 4 [4]. Each material has its unique energy levels leading to different bandgap energy levels and so different device's power handling. As seen from Fig. 4, there are three types of heterostructure each of which has different bandgap energy: AlGaAs/GaAs, AlGaAs/InP and GaSb/InAs. Fig. 4 does not show formation of any junction as yet. This is the reason why the energy levels shown are discrete. It is seen in the figure that there is a difference between the conduction bands and valence bands labeled as ΔE_c and ΔE_v respectively. As a result, the difference between the bandgap energies will depend upon the type of materials used to form a heterostructure. For example, in type 1 as shown in Fig. 4-a, the conduction band of AlGaAs is higher than GaAs material. Also, the valence band of GaAs material is higher than the one in AlGaAs.

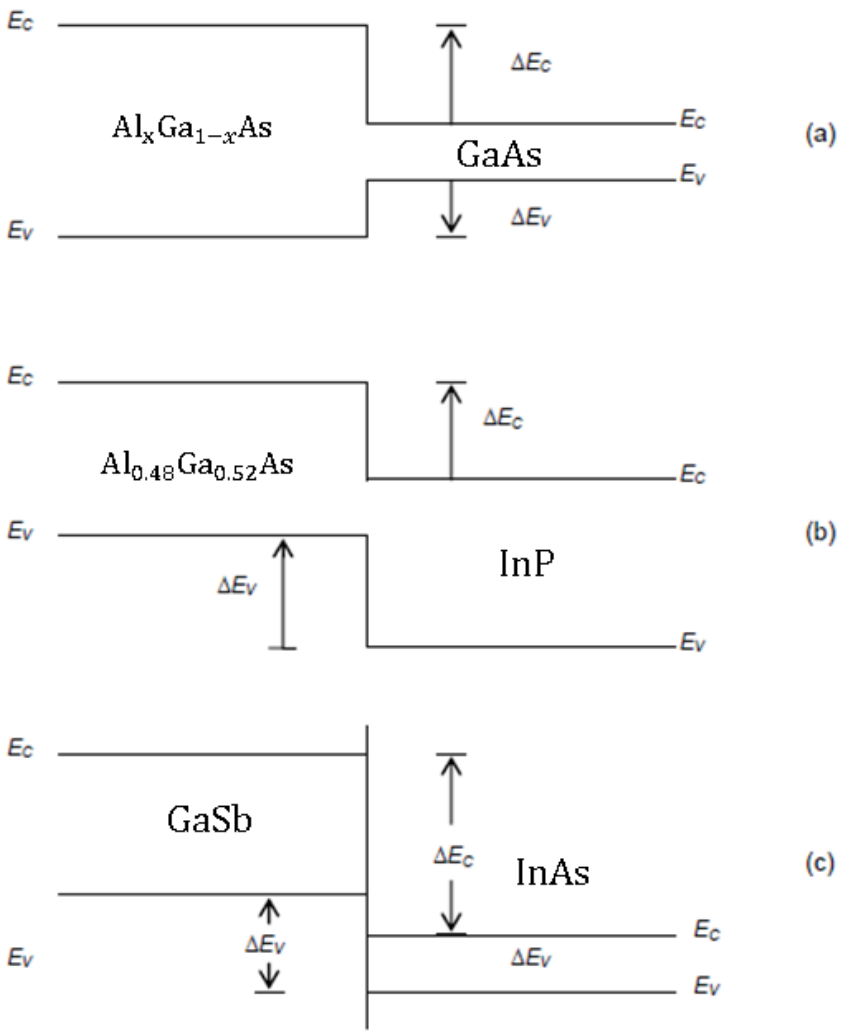

Fig. 4: Three types of Heterostructures [4]

Therefore, the difference between the bandgap energies is:

$$\Delta E_g = \Delta E_c + \Delta E_v \tag{4}$$

However, in type 2 and type 3 materials, E_v and E_c of the first material is greater than the other one. As a result, the difference in bandgap energies is:

$$\Delta E_g = \Delta E_c - \Delta E_v \tag{5}$$

ΔE_c and ΔE_v are important values when used to align Fermi levels at equilibrium (this will be discussed later in the section). Fig. 5 shows typical values of bandgap energy difference for various materials [4].

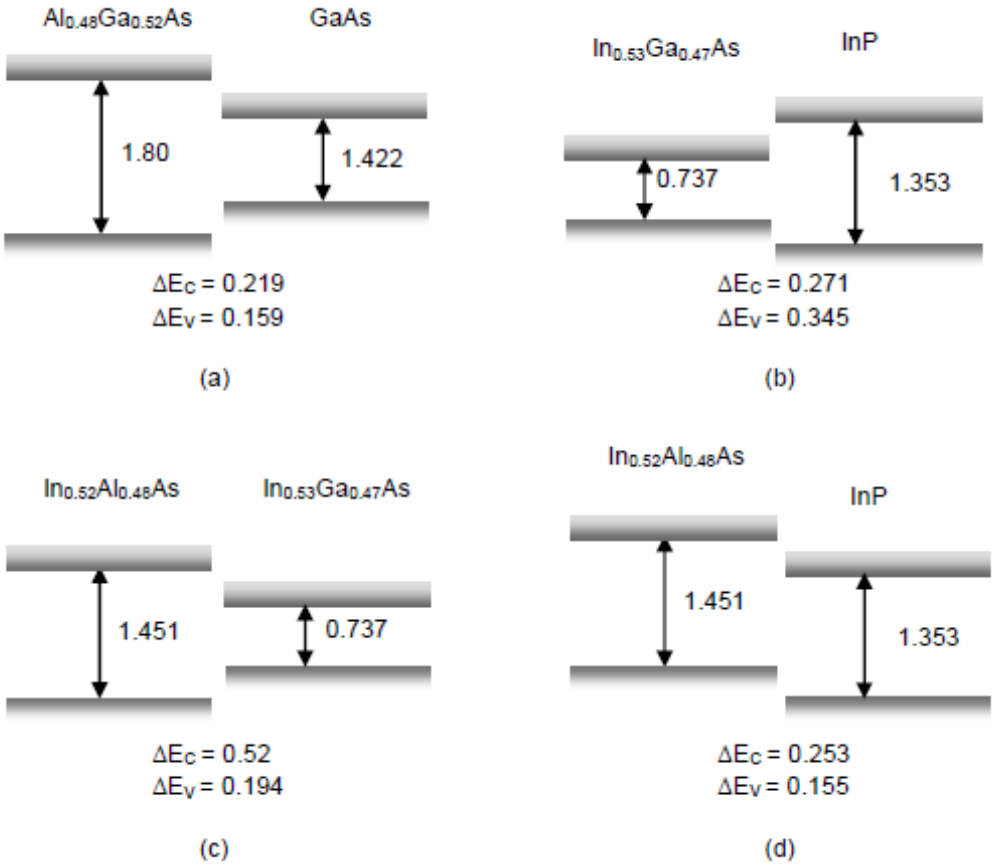

Fig. 5: Various band diagrams for heterostructures [4]

In early heterostructure-based device developments, it was believed that only material with different lattice constants can form a heterstructure in order to have aligned molecules at the junction or interface between the two materials. However, it was later discovered that materials with different lattice constants can indeed form a junction. This kind of junction formation can still be done provided that the thickness of the top material does not exceed a certain critical thickness t_c. For thickness values below t_c, the molecules of the top material will align themselves with the bottom material by strain force. Therefore, the lattice constant of the top material is ideally identical to the bottom one. The material on top in this case is normally called the pseudomorphic layer. Also, a famous device to use this principle is a pHEMT transistor (pseudomorphic high electron mobility transistor). On the other hand, if the thickness is greater than t_c, the lattice mismatch can be adjusted by strain force. This will result in dislocations and crystal defects or irregularities as shown in Fig. 6-b. Lattice mismatch in transistor's structure can cause deep level traps that can alter the electrical behavior of the device resulting in Kink Effect.

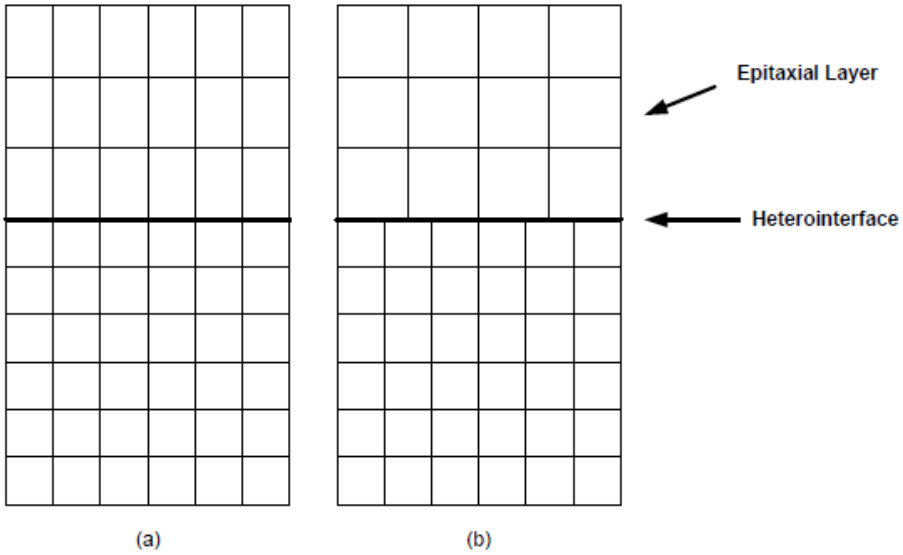

Fig. 6: (a) Different lattice constant materials adjusted by strain (b) Dislocations due to thickness greater than t_c [4]

2.2.1 HEMT general structure

It is noticed in a general p-n junction that the materials used to build its structure are the same, but each has its own doping level. This means that both materials have the same bandgap energy. However, in heterostructure devices, two different materials are used to build up the structure, so each material has a different bandgap energy. Since the bandgap energies are different in heterostructure, there will be an energy discontinuity at the interface of the device. Fig. 7 shows an example of GaAs/AlGaAs heretrostructure device where one layer has a narrow bandgap energy unlike the other one. This will lead to abrupt energy change at the heterojunction [7]. Also, the contacts of the drain and source terminals use a heavily doped GaAs layer in order to decrease the contact resistance, so the noise performance of the device is improved.

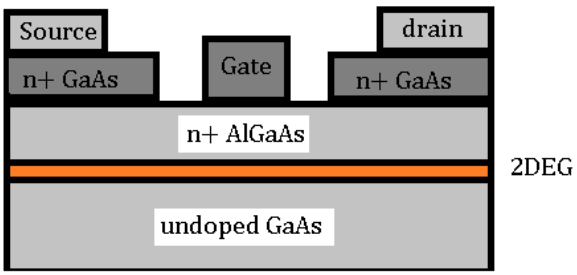

Fig. 7: AlGaAs/GaAs HEMT cross section [4]

There are two main structures that are used to build a HEMT device: pseudomorphic and metamorphic structures (pHEMT and mHEMT). In the case of pHEMT, ideally, materials used to build the device structure should have the same lattice constant. However, typical materials used such as GaAs/AlGaAs don't have the exact same lattice constant. Therefore, a thin layer of InGaAs is used between GaAs and AlGaAs to eliminate the lattice mismatch by means of compressive strain as shown in Fig. 8 [4, 9].

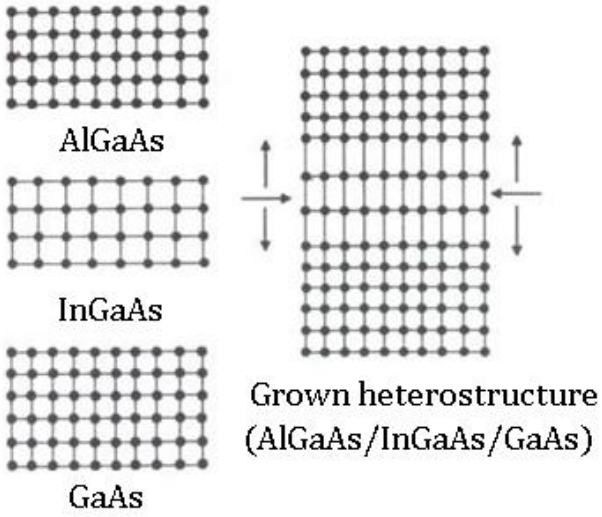

Fig. 8: Compressive strain in InGaAs in AlGaAs/InGaAs/GaAs heterointerface [4]

For the metamorphic device (mHEMT), the separation between the main materials, whose lattice constants are different, is done by introducing a buffer layer. However, the chosen material for the buffer layer should match the lattice constant of the channel layer [9]. An example of mHEMT device is shown in Fig. 9 with InP substrate.

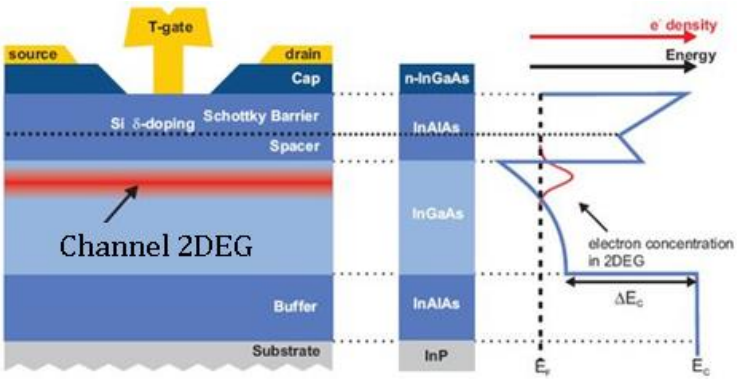

Fig. 9: InP HEMT device [10]

Fig. 10 shows the energy band diagram of each layer prior to forming a heterojunction. Generally, the vacuum level is parallel to the conduction band and valance band levels as seen in Fig. 10, this is called the *Electron Affinity Rule*. As a result, the difference in conduction and valence bands, ΔE_c and ΔE_v, will be maintained even after the heterojunction is formed [7]. Also, it is seen in Fig. 10 that the Fermi level is closer to the conduction band (E_{Fn}) in n-type material, and the Fermi level is closer to the valence band in p-type material (E_{Fp}).

In general, electrons tend to flow from higher Fermi levels to lower ones. Even if the conduction band of the material with a low Fermi level is higher than the material with a high Fermi level, the electrons still flow from higher to lower Fermi levels. The reason is that the material with a low Fermi level means that most electrons have a high probability of occupying lower energy states. Therefore, this material tends to accept electrons.

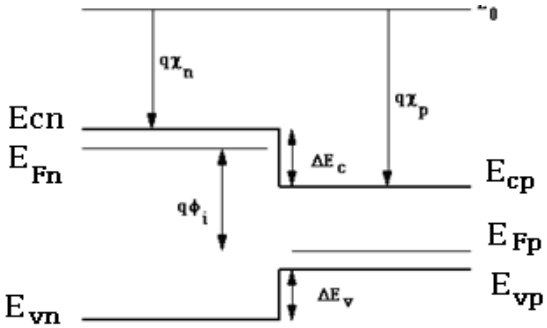

Fig. 10: narrow/wide-bandgap materials' band diagram [8]

When two different materials are joined to form a heterostructure, the Fermi levels of both materials must align to a new one. The new Fermi level is a resultant from the electron transfer from the material with higher fermi level to the material with lower Fermi level. This phenomenon is the core principle of HEMT devices' operation. In normal FET devices such as MOSFETs, the carrier concentration in the channel is increased by introducing a dopant impurity. However, this comes at the expense of scattering which will affect the electrical properties and operation of the device by decreasing carrier mobility and device speed [4]. In the HEMT device, because the carrier concentration is increased by forming a heterostructure, issue of scattering is eliminated in the device. Therefore, mobility and device speed is greatly improved. The process by which the carrier concentration is increased in heterostructures is called Modulation Doping. Modulation Doping happens whenever wide bandgap n-

type material (i.e. AlGaAs) forms a junction with lower bandgap energy undoped material (i.e. GaAs). As mentioned earlier, when a heterostructure is formed, Fermi levels of both materials will align due to electron transfer. As a result, there will be an electric field at the heterojunction due to charge imbalance. This electric field will result in band bending as shown in Fig. 11.

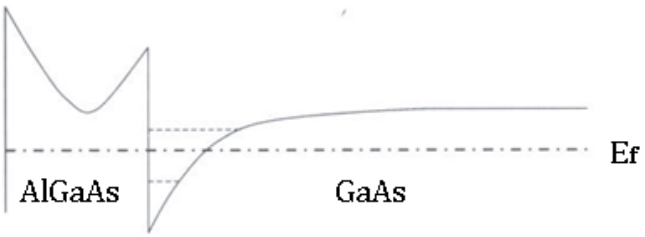

Fig. 11: Energy band diagram of AlGaAs/GaAs heterojunction [4]

Because an energy band bends upward in AlGaAs and downward in GaAs, there will be an abrupt change in energy at the hetero-interface. Therefore, a quantum well is formed. There will be discrete energy levels in this quantum well according to the solution of the Schrodinger equation. Since this quantum well contains the lowest energy in the conduction band of the heterostructure, transferred electrons tend to occupy it. Therefore, electron concentration is increased at the hetero-interface. This electron formation at the heterjunction is called Two Dimensional Electron Gas (2DEG). Electrons in the 2DEG region have high mobility since they are not obtained from dopant impurity. The carrier mobility of an HEMT device can be further improved by introducing an undoped layer at the heterojunction to decrease the coulomb interaction at the hetero-interface as shown in Fig. 12.

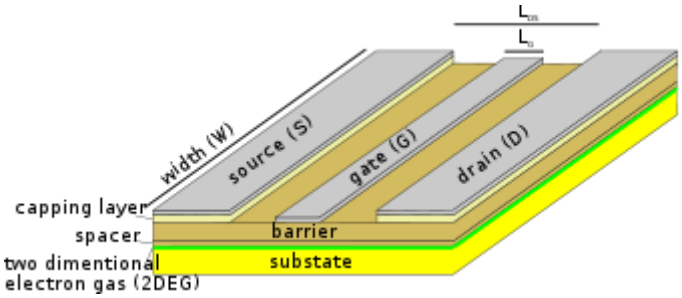

Fig. 12: Heterojunction containing an undoped spacer layer [11]

Not only can the carrier mobility be improved in an HEMT device, but also the carrier concentration, so the current density is increased in the channel. Electron concentration in the channel depends on the electron transfer from the barrier layer to

channel layer after which the heterojunction is formed. As a result, the higher the difference between the Fermi levels of the barrier layer's material and the channel layer's material, the higher the electron transfer will be to the channel layer leading to higher carrier concentrations. Therefore, it is desirable to increase the bandgap energy of the barrier layer and decrease the bandgap energy in the channel layer [12]. An example of an HEMT device with increased carrier concentration is $AlGaAs/In_xGa_{1-x}As$. When the concentration of indium is increased the bandgap energy of the channel layer ($In_xGa_{1-x}As$) is decreased. However, it is important to study the lattice mismatch in the device as indium concentration is increased to avoid deep-level traps.

Chapter 3: Large and Small Signal Modeling for FET and HEMT Devices

In order to model a transistor using behavioral modeling techniques, certain measurements have to be implemented. Those measurements will be mapped to certain mathematical functions in a behavioral model. The two main measurements necessary to characterize a transistor are DC and RF measurements to obtain transistor's I-V characteristics and s-parameters. The I-V characteristics cover drain-source current behavior, and s-parameters are used to obtain the parasitic elements of the transistor found in the transistor's equivalent circuit model. Generally, small or large signal models describe the electrical behavior of a transistor, and are often composed of nonlinear components. Fig. 13 shows a typical parasitic element for both HEMT and FET transistors and Fig. 14 shows an equivalent large signal model.

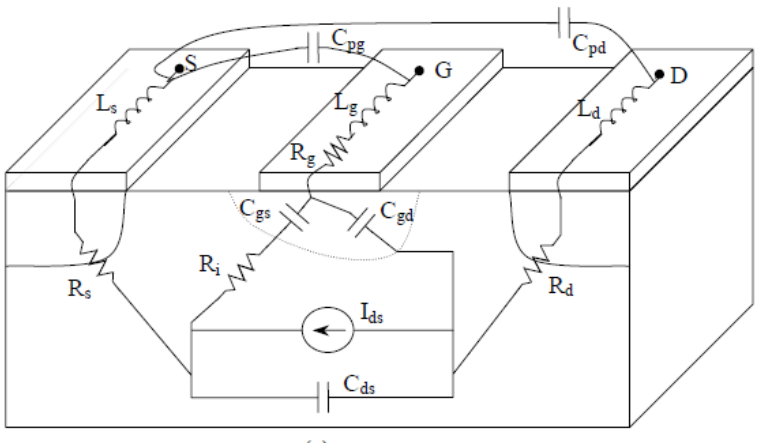

Fig. 13: Typical transistor's parasitic elements [13]

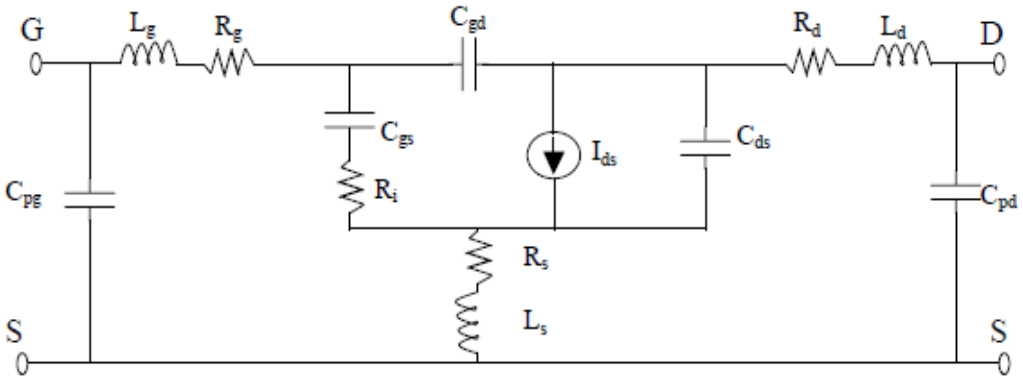

Fig. 14: HEMT/FET large signal model [13]

The large signal model can be divided into two parts: intrinsic (Cgd, Cgs, Ri, Cds, Ids) and extrinsic elements (Lg, Rs, Rd, Ld, Rs, Ls, Cpg, Cpd). The physical meaning of each element in the large signal circuit goes as follows [13]:

- Lg, Ls, and Ld are gate, source and drain inductances, respectively, due to the metal contact implanted of the surface of the device.
- Cgs and Cgd are gate-source and gate-drain capacitances, respectively.
- Rg, Rd, and Rs are gate, drain and source ohmic resistances.
- Cpg and Cpd are contact pad capacitances.

There are many methods by which parasitic parameter extraction can be done to obtain accurate s-parameters' representation at different gate and drain voltages. The main methods fall under two categories that will be discussed in the upcoming section:

1) Building a large-signal model using a small signal one.
2) Directly build a large signal model using measured DC characteristics.

3.1 Building a Large Signal Model Using a Small Signal Model

In the first step, the extrinsic elements should be determined at pinch-off conditions. The transistor's current is forced to be zero at pinch off conditions, so the circuit in Fig. 14 can be reduced to the one in Fig. 15. As a result, the number of unknown of variables is reduced. Also, at pinch off condition, most unknown variables are the extrinsic elements.

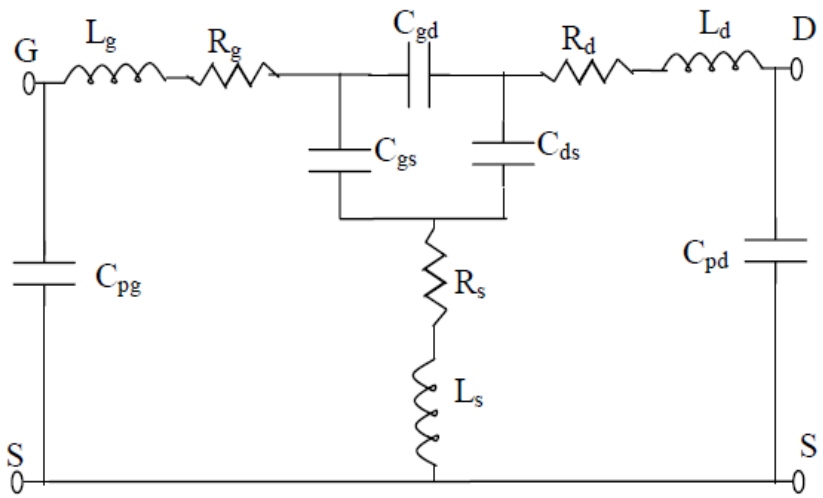

Fig. 15: Reduced circuit at pinch-off condition [13]

Parameters in Fig. 15 can be calculated from s-parameters at this condition using the following steps:

1) Convert s-parameters to admittance matrix to remove the effect of pad capacitances.
2) Convert admittance matrix to impedance matrix to remove effect of gate, drain and source impedances since they are connected in series.
3) Convert the impedance matrix in from step 2 to admittance matrix to calculate the intrinsic elements.

Those steps are further described in Fig. 16.

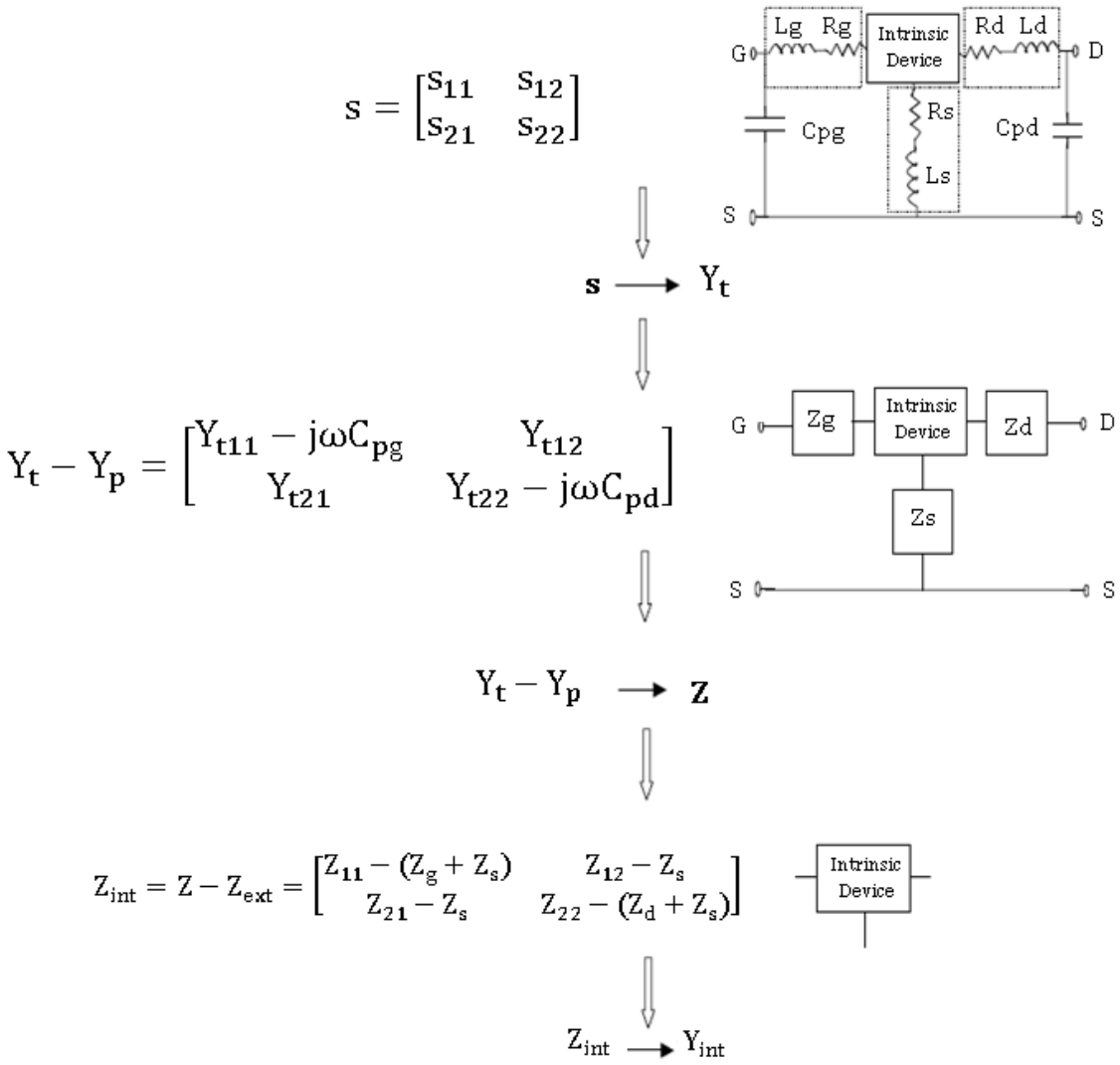

Fig. 16: Parasitic elements extraction flowchart [13]

Where Y_t is admittance obtained from s-parameters, Y_p is admittance of pad capacitances, Z_{int} is impedance of intrinsic elements, and Y_{int} is admittance of Z_{int}.

3.1.1 Parameter extraction using global optimization

The methodology of extracting extrinsic parameters shown in Fig. 16 can be applied to any case or any type of modeling. Assuming extrinsic elements are extracted at pinch-off conditions, the intrinsic elements can be calculated after de-embedding extrinsic elements from the circuit. To extract the intrinsic part of the small signal model, it is proposed in [14] that Particle Swarm Optimization (PSO), a global optimization algorithm, can be used to in order to determine intrinsic elements found in Fig. 17.

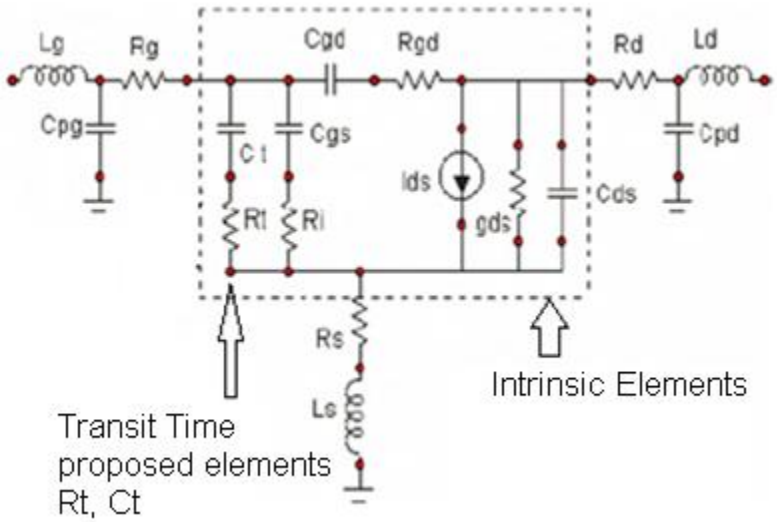

Fig. 17: FET small signal model [14]

The algorithm of PSO that can be used to determine the intrinsic part goes as follows:

1) Initialize particle: each particle is randomly set with determined bounds.
2) Update velocity: at each iteration, the velocity of each particle is updated as per the following equation (where *i* is particle's number and *k* is the iteration number) :

$$v_{i,k+1} = wv_{i,k} + c_1 * r_1 * \left(p_{i,best} - S_{i,k}\right) + c_2 * r_2 * \left(g_{i,best} - S_{i,k}\right) \quad (6)$$

3) Update position of each particle:

$$S_{i,k+1} = S_{i,k} + v_{i,k+1} \quad (7)$$

4) Stopping criteria:

$$p_{i,best,k+1} = \begin{cases} p_{i,best} & if\ F\left(s_{i,k+1}\right) > F(p_{i,best}) \\ S_{i,k+1} & if\ F\left(s_{i,k+1}\right) < F(p_{i,best}) \end{cases}$$

Where

- $v_{i,k+1}$ is the updated particles' velocity, $v_{i,k}$ is the current particles' velocity
- w is some weight, c_1 and c_2 are constants, r_1 and r_2 are random numbers between 0 and 1
- $S_{i,k}$ is current position update for all particles, $S_{i,k+1}$ is the updated position for all particles.
- $p_{i,best}$ is particles' personal best solution, $g_{i,best}$ is the best global solution found in all iterations.

The objective function *E* for PSO optimization will be as follows (where *m* is measured and *sim* is simulated s-parameters):

$$E = \frac{1}{n}\sum_{f1}^{fn} w1\left|s_{11,m} - s_{11,sim}\right|^2 + w2\left|s_{21,m} - s_{21,sim}\right|^2 + w3\left|s_{12,m} - s_{12,sim}\right|^2 + w4\left|s_{22,m} - s_{22,sim}\right|^2 \quad (8)$$

The extraction that can be applied to the PSO algorithm is shown in Fig. 18. The first step is to convert s-parameters to z-parameters. Then de-embedding of $R_g, R_s, R_d, L_g, L_s, L_d$ from z-parameter will be done. Then, z-parameters will be converted to y-parameters. Next, de-embed $c_{pg}, and\ c_{pd}$ from y-parameters. Then, estimate the intrinsic elements' error using y-parameters. Finally, if the objective function is satisfied, terminate the algorithm.

3.1.2 Global optimization-less small signal modeling

Generally, global optimization algorithms (GO), such as PSO or the Genetic algorithm, can be used in cases where the number of unknown parameters is high, i.e. 18 parameters, and the initial guess is not close to the optimal solution. Unlike global optimizations, local minimum search algorithms (LMS), such as Newton's method, should have an initial guess that is close to optimal solution in order to avoid local minima. However, choosing an initial guess that is close to optimal solution is really difficult. If the problem of choosing a good initial guess for the LMS algorithm is solved, then LMS algorithms will have an advantage over GO algorithms since LMS algorithms are less complicated in terms of programming as compared to GO algorithms.

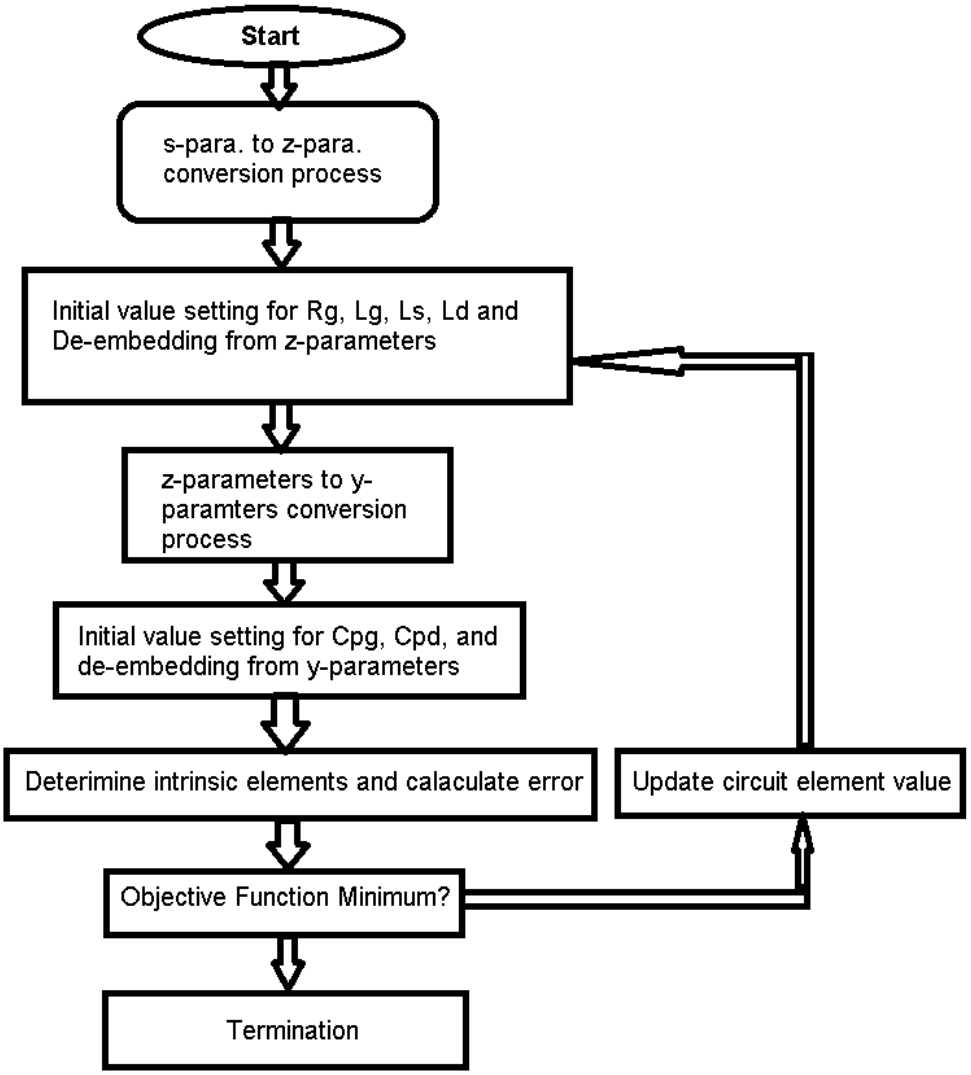

Fig. 18: Flow chart for parameter extraction using PSO [14]

This problem is solved in [15] for small signal parameter extraction. The proposed algorithm in [15] is to determine parasitic elements first from low frequency pinch-off s-parameter measurement. The reason to perform low frequency measurement is that the small signal model in Fig. 19-a can be simplified to Fig. 19-b since inductances and resistances can be ignored at lower frequencies. As a result, the number of unknown variables is reduced to the capacitive elements only.

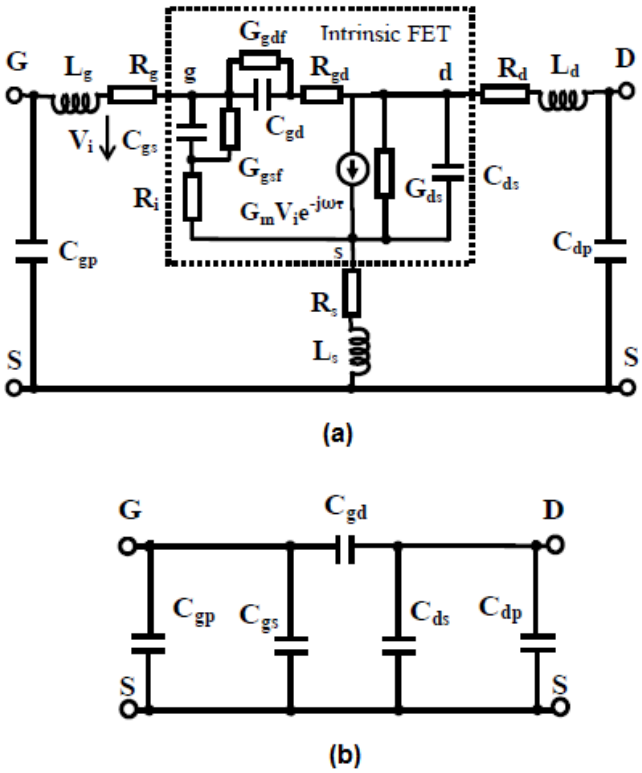

Fig. 19: (a) Small signal model for GaN of Si Substrate (b) Low frequency pinch-off equivalent small signal model [15]

The parasitic elements found in Fig. 19-b can be determined from converting s-parameter to y-parameter. Then, find the values of the unknown parasitic capacitances from the slope of the y-parameter's imaginary part as shown in equation 9.

$$y_{11} = j\omega\left(c_{gp} + c_{gs} + c_{gd}\right) \tag{9.a}$$

$$y_{22} = j\omega\left(c_{dp} + c_{ds} + c_{gd}\right) \tag{9.b}$$

$$y_{12} = y_{21} = -j\omega c_{gd} \tag{9.c}$$

After finding $c_{gp}, c_{gs}, \ c_{gd}$ and c_{ds} using any optimization algorithm, the values of c_{gp} and c_{dp} will be changed as per the flow chart found in Fig. 20 in order to have good initial estimates of the parasitic inductances and resistances shown in Fig. 21 at higher frequencies.

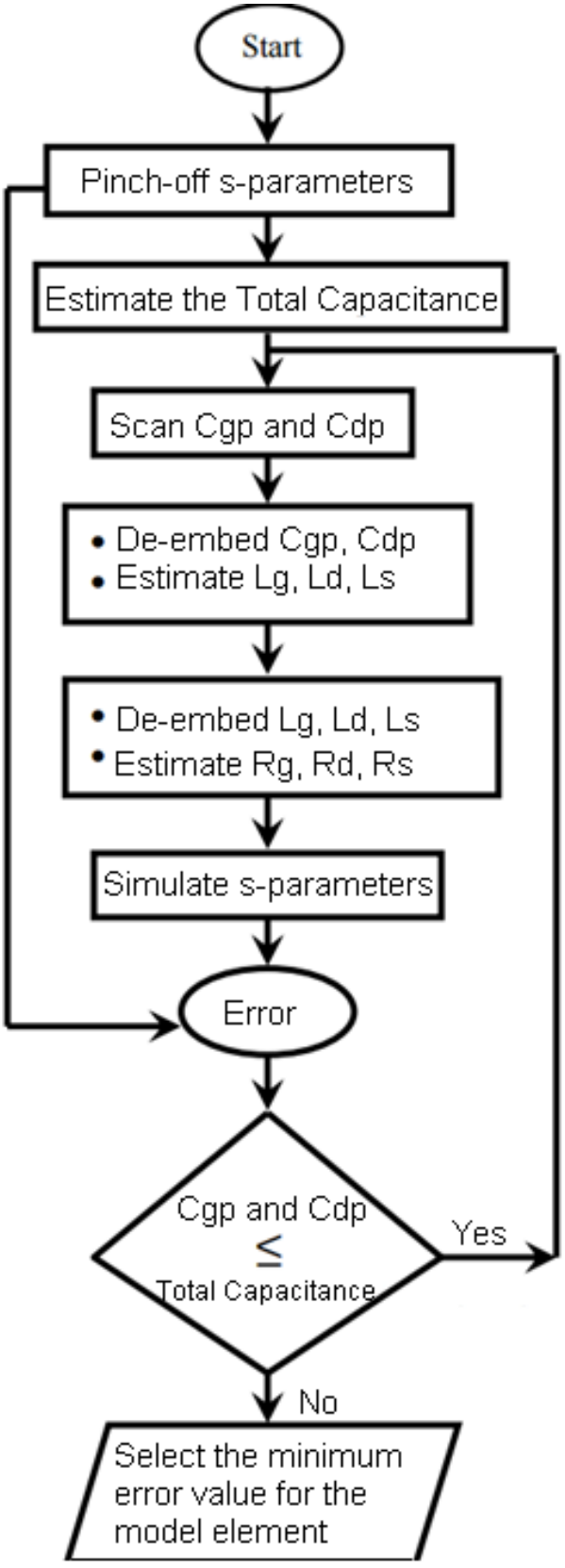

Fig. 20: Flowchart of starting value generation procedure [15]

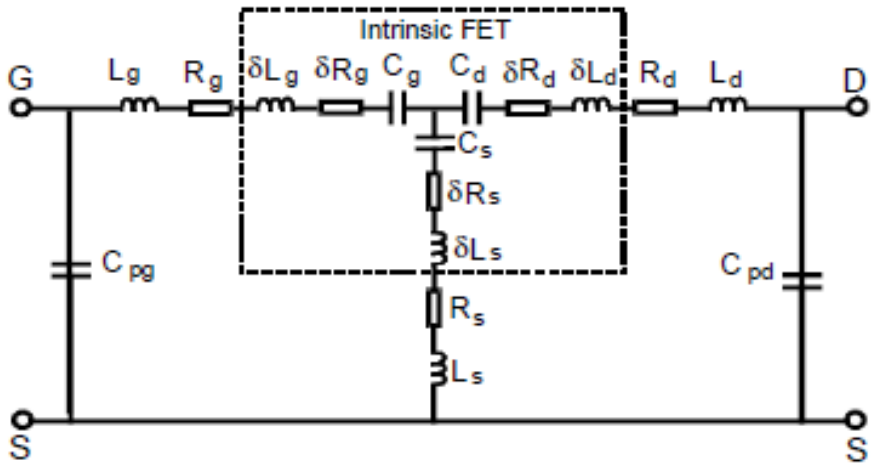

Fig. 21: High frequency pinch-off small signal model [15]

The algorithm in Fig. 20 starts by estimating parasitic capacitances as per equations 9 using any optimization algorithm. Then, capacitances c_{gp} and c_{dp} will be swept from $(0 \leq c_{gp} \leq c_{gp} + c_{gs})$ and $(0 \leq c_{dp} \leq c_{dp} + c_{ds})$ in order to find the best approximate initial guess for parasitic inductances and resistances. $(c_{gp} + c_{gs})$ is called total gate capacitance, and $(c_{dp} + c_{ds})$ is called total drain capacitance. The de-embedding discussed in the flowchart reflects upon converting y-parameters to z-parameters to de-embed the corresponding parasitic element. The best initial guess obtained as per the flowchart is the one that yields the lowest pinch-off s-parameter error. The last step is to use an LMS algorithm to refine the initial guess.

Another global optimization-less procedure for parameter extraction was applied in [16] and [17]. However, it is slightly different when it comes to determining extrinsic/intrinsic capacitances, inductances and resistances. The modeling procedure, described in the flowchart in Fig. 22, determines the external pad capacitances at low frequencies where the effect of inductances and resistances can be eliminated. Then, the algorithm estimates parasitic inductances at medium frequencies which should be high enough to show the effect of inductances and resistances. Lastly, the intrinsic parasitic capacitances will be re-determined at higher frequencies where their effect shows up.

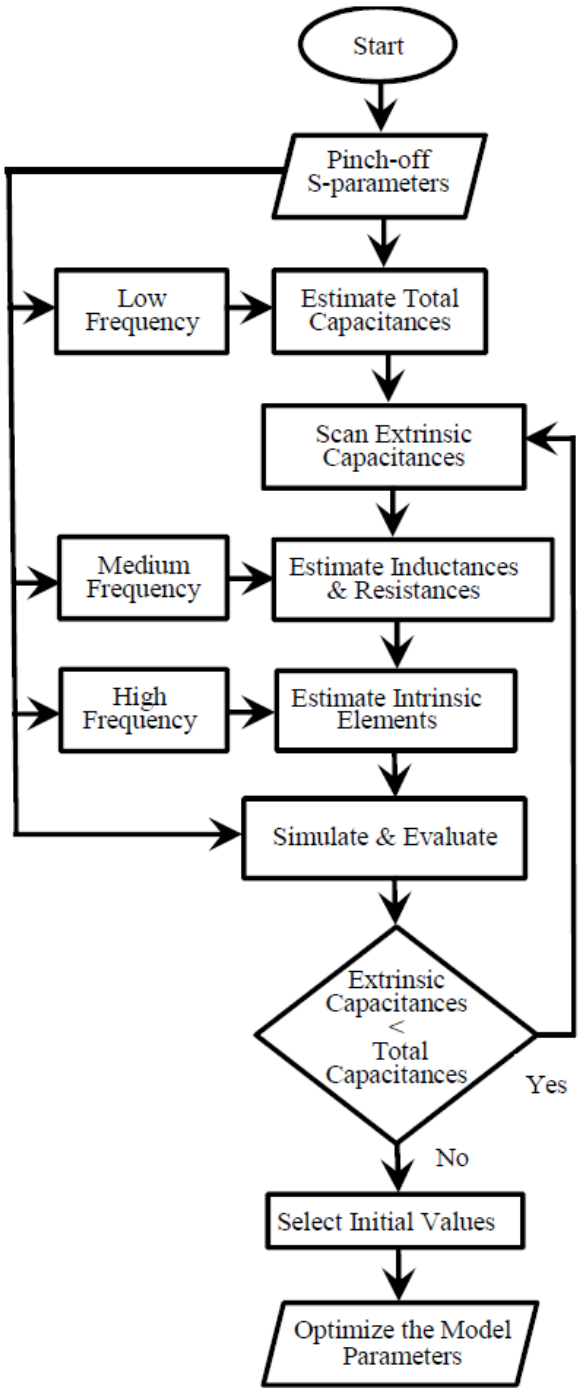

Fig. 22: Flowchart of the model parameter extraction proposed in [16]

Another global optimization-less technique for small signal parameter extraction was also developed in [18]. This developed model is almost similar to the one found in [15]. However, the definition of the objective function for the stopping criteria is different. In [15], the objective function is written only in terms of s-parameter error. On the other hand, the objective function in [18] adds another performance quantity that depends on the final application. For example, the main

application of GaN-based HEMT devices is designing power amplifiers. So, measures such as input and output impedances, gain, and stability factor (K) are important for power amplifier design. It is shown in equation 10 that stability factor can be written as a function of s-parameters:

$$K = \frac{1 - |s_{22}|^2}{|s_{22} - s_{11}^{*}\boldsymbol{\Delta_s}| + \boldsymbol{s_{12}s_{21}}} \tag{10}$$

The objective function of the stability factor will be:

$$e_K = \frac{1}{N}\sum_{i=1}^{N} |K_{meas} - K_{sim}| \tag{11}$$

Where K_{meas} is the measured stability factor, and K_{sim} is the simulated stability factor. Also, the gain of the power amplifier is G, shown in equation 12:

$$G = \frac{|s_{21}|^2 - 1}{\ln(|s_{21}|^2)} \tag{12}$$

The objective function of gain error performance is shown in equation 13:

$$e_G = \frac{1}{N}\sum_{i=1}^{N} |G_{meas} - G_{sim}| \tag{13}$$

Another modification was done on the small signal equivalent circuit model shown in Fig. 19 in [19]. The model in [19] adds the effect of capacitive loading at the buffer/substrate interface as shown in Fig. 23.

The general algorithm for obtaining the parasitic elements is still the same as the one shown in Fig. 20. However, the parasitic inductances are estimated at unbiased s-parameter measurement as shown in Fig. 24. Furthermore, the model in Fig. 23 is obtained with several transistors' widths.

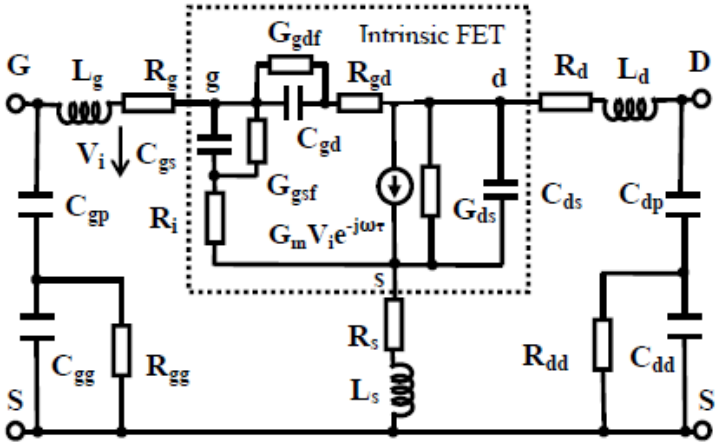

Fig. 23: Small signal model for GaN HEMT on Si substrate [19]

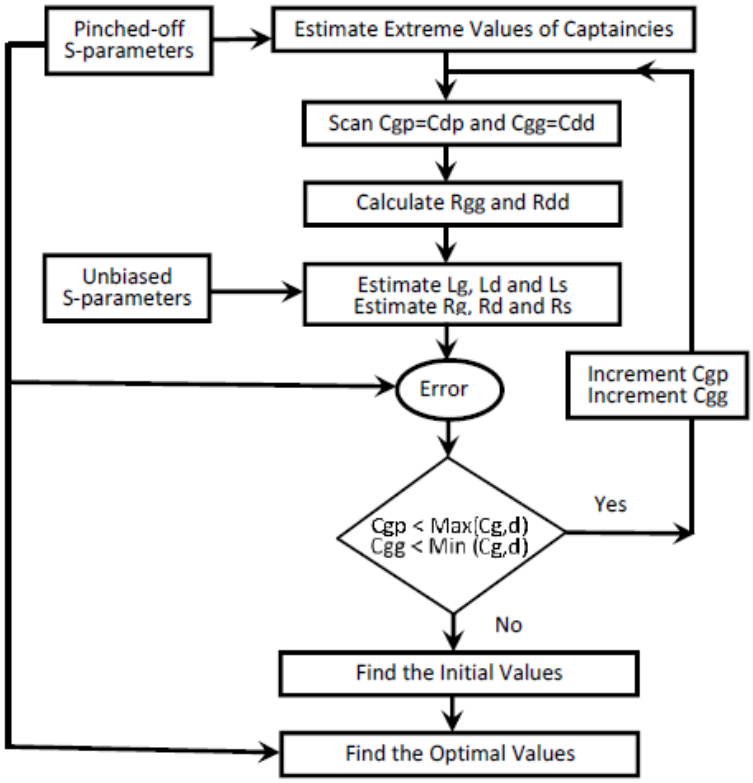

Fig. 24: Parasitic extraction flowchart [19]

3.1.3 Extending small signal model to a large signal one

As described previously, there are many methods by which small signal parameters are extracted. The extrinsic part was found at pinch off conditions, and the intrinsic part can be found at forward bias conditions. To extend small signal models to large signal ones, the previously mentioned algorithms can be used in order to find all parasitic elements while dealing with transconductance and output conductance as

unknown optimization parameters (although they are measurable quantities) that can be used to fit measured s-parameters. Then, forward bias s-parameters will be obtained to formulate the complete large signal model. At forward bias conditions, parasitic gate-source, gate-drain and drain-source capacitances will stay as optimization parameters since they are bias dependent parasitics. Meanwhile, all parasitic resistances and inductances and pad capacitances will be kept as constant at forward bias conditions since they are bias-independent parameters. The large signal model can be realized as shown in Fig. 25 [20, 21].

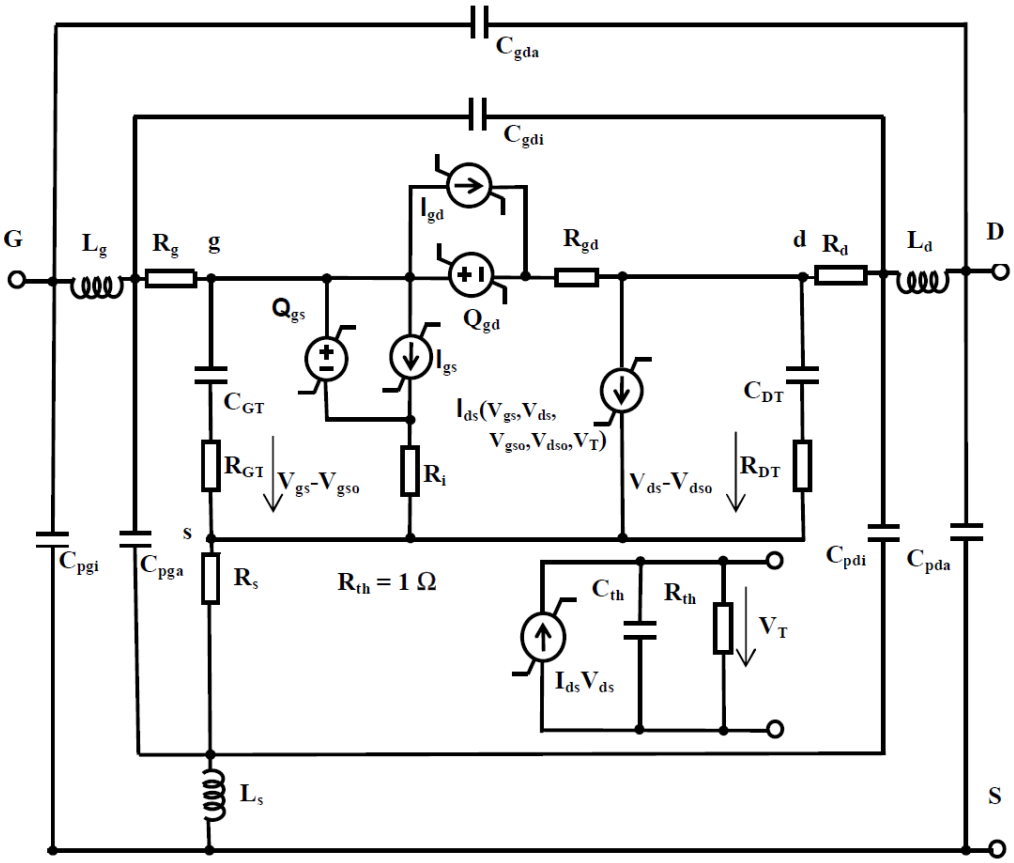

Fig. 25: GaN HEMT Large signal model [20]

The model includes gate charge sources that can be obtained by integrating c_{gs} and c_{gd}. Also, I_{gs} and I_{gd} are obtained by integrating conductances G_{gs} and G_{gd}. The drain-source current will be obtained from pulsed and extra-static DC measurements in order to characterize self-heat and trapping effects. The mathematical model that can be used to simulate this is shown in equation 14.

$$I_{ds} = I_{ds,iso}(v_{gs}, v_{ds}) + a_T(v_{gs}, v_{ds})(I_{dso}V_{dso}) + a_G(v_{gs}, v_{ds})(v_{gs} - V_{gso}) + a_D(v_{gs}, v_{ds})(v_{ds} - V_{dso}) \quad (14)$$

Where $I_{ds,iso}$ is isothermal drain current. a_T, a_G and a_D are bias dependent parameters that are used to simulate self-heating and trapping effects. To form an analytical formulation of Q_{gs}, Q_{gd}, I_{ds}, I_{gs} and I_{gd}, a genetic-neural optimization can be used where the neural networks have different activation functions, hyperbolic-tan or exponential functions as described in [20].

A different methodology was done in [22-24] to convert the small signal model into a large signal one. Instead of genetic-neural networks, a table-based model can be used in order to represent drain current model with self-heating and trapping effects. A table-based model takes discrete data (i.e. I_{ds}) and stores them in multi-dimensional tables. The circuit simulator will take care of any necessary interpolations. In other words, there are no closed-form equations to represent DC or AC behavior of transistors. As a result, table-based models can be used for any type of transistors: MESFET, MOSFETS, HEMTs, etc. However, the main limitation of table-based models is the interpolation algorithm used in them to define I-V and Q-V relations. Some table-based models have been shown to be inaccurate in terms of simulating high-order distortion products when the input signal magnitudes are comparable to or smaller than the distance between neighboring data points [25].

3.2 Direct Large Signal Modeling

It was seen earlier that in a small signal model, the parasitic parameter extraction is obtained at specific bias point (Q-point). Small signal models are only attractive when the RF circuit designer requires that the application only requires operation in the linear region of the amplifier. When the amplifier is operating in the linear region, extremely minor variation happens in the bias-dependent parameter in the small signal model such as gate-source capacitance. As a result, all parasitic parameters in the small signal model are constant and obtained from a single s-parameter measurement (single V_{gs} and V_{ds} point). A typical utilization of the small signal model is in low-noise amplifiers (LNA). The reason is that LNA circuits are generally used in cases where low-power signal captured by an antenna is needed to be amplified in a receiver implementation as shown in Fig. 26.

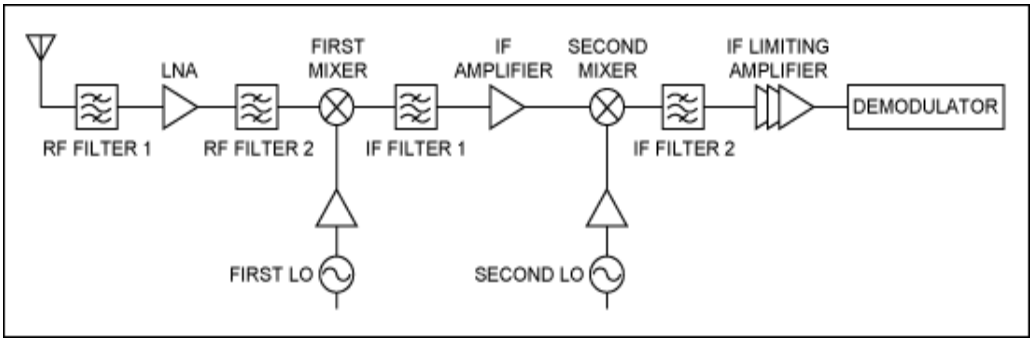

Fig. 26: General receiver implementation [26]

Then what about large signal models? Large signal models normally include both large and small signal operation. In other words, the large signal model can be used with low and high input powers (covering linear and non-linear regions) [27]. Unlike small signal models, a large signal model is obtained at various V_{gs} and V_{ds} points in order to account for variation in I-V characteristics, transconductance, output conductance, gate-source and gate-drain capacitances. Therefore, some parasitic parameters (i.e. C_{gs} and C_{gd}) in large signal models are said to be bias-dependent. Large signal models are used in cases where an application is operating at high input power levels such as mixers. The reason why a mixer circuit needs a large signal model is because the mixer needs to generate harmonics after the signal being amplified by the LNA as shown in Fig. 26. Also, large signal models are also required in the design of power amplifiers and oscillators [27].

There are various approaches to develop a large signal model for an FET/HEMT device. All parasitic elements shown in Fig. 14 can be obtained from DC (including pulse) and s-parameters measurements at different drain and gate voltages. A common practice to develop a large signal model is to use a table-based model or charge-based model as discussed earlier. A different approach is to use smooth and continuous functions to represent drain current and bias-dependent parameters such as C_{gs} and C_{gd}. The capacitance model can be described as in the following equations [28].

$$C_{gs} = C_{gs0}\left(1 + p_1 \tanh\left(p_{1gsg}V_{gs} + P_{2gsg}V_{gs}^2\right)\right)(1 + \lambda_c V_{ds}) \quad (15)$$

$$C_{gd} = C_{gd0}\left(1 + P_{2g} \tanh\left(P_{1dgd}V_{gs}\right)\right)\left(1 - P_{2d} \tanh\left(P_{1gdd}V_{ds} + P_{2gdd}V_{ds}^2 + P_{1cc}V_{ds}V_{gs}\right)\right) \quad (16)$$

Where C_{x0} is the capacitance at pinch off state, P_x is the fitting parameter. It is important that capacitance C_{x0} should be obtained from the device's structure physics-

based simulator in order to have a meaningful and physically relevant curve fitting for the capacitance models. Often, C_{x0} value is determined by the manufacturer. The advantage of the C_{gs} and C_{gd} equations being continuous functions is that they will have well defined derivatives in order to properly converge in harmonic balance simulations [29].

For DC characteristics of the transistor to be modeled, the drain-source current's unknown parameters can be obtained depending on the model used. This requires DC measurements to be taken at different voltage biases of gate-source and drain source voltage. Then, the obtained I-V characteristics data can be mapped to a behavioral model. There are many behavioral drain current models that are already found in literature. Each of the models has a different approach to map the mathematical model to the measured data. The pros and cons of the following behavioral models will be discussed in the following section.

3.2.1 Curtice model

The Curtice model was one of the first high frequency models that were implemented in circuit simulators. As an early development of models for CAD tools, the Curtice model suffered from accuracy for wide range of bias voltages. Also, this model has an accuracy tradeoff between the fitted DC and AC performance [30]. The Curtice I-V equation can be written as:

$$I_{ds} = K * \left(V_{gs} - V_t\right)^2 * (1 + \lambda * V_{ds}) * \tanh(\alpha * Vds) \quad (17)$$

$$V_t = \frac{q * Na^2}{2 * \varepsilon} - \emptyset b \quad (18)$$

Where V_t is the threshold voltage, K and α are model parameters. Parameter λ characterizes channel length modulation, and the tanh function corrects the value of drain current at knee voltage when fitting the data.

3.2.2 Angelov model

The Angelov Model is one of the most well-known empirical models when it comes to modeling the behavior of HEMT and MESFET devices. It is a simple model where its parameter can be simply extracted by inspection or by an optimization technique [31]. The main purpose of the Angelov model is to model the I-V

characteristics of the device and its derivatives. The new concept that the Angelov model brings to the table is that the drain current equation can be written as follows:

$$I_{ds}(Vgs, Vds) = f_{dsa}(Vgs) * f_{dsb}(Vds) \quad (19)$$

Where the first term, $f_{dsa}(Vgs)$, is only dependent on gate voltage, and the second term is only a function of drain-source voltage. The first function is chosen such that its derivative gives the same behavior as the transistor's transconductance. Since the transconductance of HEMT and MESFET devices are bell-shaped, f_{dsa} is chosen as tanh(ψ) in equation 20. The second term represents the channel length modulation and knee-voltage correction function $\tanh(\alpha * Vds)$.

$$I_{ds} = I_{pk} * (1 + \tanh(\psi)) * (1 + \lambda * Vds) * \tanh(\alpha * Vds) \quad (20)$$

Where I_{pk} is the drain current at which maximum transconductance exists. λ is the channel length modulation term, and α is the saturation voltage parameter. ψ is a power series function centered at Vpk while Vgs is the variable.

$$\psi = P1 * (Vgs - Vpk) + P2 * (Vgs - Vpk)^2 + P3 * (Vgs - Vpk)^3 \quad (21)$$

Where P1, P2 and P3 are fitting parameters, and Vpk is the gate voltage at which maximum transconductance occurs. However, in some variants of HEMT devices, Vpk is weakly dependent on the drain voltage in the saturation region, so Vpk can be written as follows:

$$Vpk = Vpk0 + \gamma * Vds \quad (22)$$

A modification was done in [32] in order to increase the accuracy of the drain current. The simple modification is re-writing ψ as follows:

$$\psi = P1 * (A * Vgs + B - Vpk) + P2 * (A * Vgs + B - Vpk)^2 + P3 * (A * Vgs + B - Vpk)^3 \quad (23)$$

In order to give more consideration to the input voltage on drain current characteristics, Vgs term is replaced by a polynomial function: $A * Vgs + B$. where A and B are fitting parameters. The impact of this replacement on the simulated drain current is shown in Fig. 27.

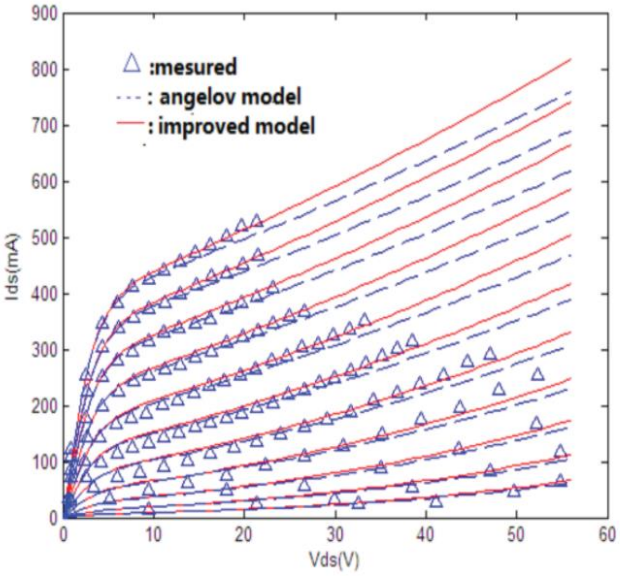

Fig. 27: Simulated vs. measured drain current [32]

3.2.3 Liu-He model

Lin-He model is an improved model over the Angelov model. The prime goal of this model is to improve the accuracy of modeled drain current and transconductance which is normally bell-shaped for an HEMT device. The drain current equation used in the Angelov model can be re-written as follows [33]:

$$I_{ds} = I_{pk} * \left(1 + \frac{\exp(\psi) - \exp(-\psi)}{\exp(\psi) + \exp(-\psi)}\right) * \left(\frac{\exp(a * Vds) - \exp(-a * Vds)}{\exp(a * Vds) + \exp(-a * Vds)}\right)$$

$$= I_{pk} * \left(\frac{2 * \exp(2 * \psi)}{1 + \exp(2 * \psi)}\right) * \left(\frac{\exp(2 * a * Vds) - 1}{1 + \exp(2 * a * Vds)}\right) \quad (24)$$

Where ψ and Vpk are the same parameters found in the Angelov model. It is seen from the equation above that the Angelov model has a restriction on saturation current that is equal to $2I_{pk}$. It is mentioned in [34-36] that this restriction will limit the accuracy of the model. The Liu-He model provides a solution for this problem by re-writing the Angelov Model as follows:

$$I_{ds} = I_{pk} * \left(\frac{(1 + A0 + A1 * Vds) * \exp(2 * \psi)}{A0 + A1 * Vds + \exp(2 * \psi)}\right) * \left(\frac{\exp(2 * a * Vds) - 1}{B0 + B1 * Vgs + \exp(2 * a * Vds)}\right) \quad (25)$$

This proposed modification adds parameter A which allows the elongation of the bell-shaped transconductance for gate-source voltage that is greater than the voltage that exists at peak transconductance. The extraction process for the modified model is the same as that found in the Angelov model [33]. Also, the inaccuracy found in the

Angelov model is that it accounts for symmetrical behavior for the transconductance which is not necessarily the case, yet the modified version allows the drain current to increase by 2*Ipk. As a result the Liu-He model corresponds to asymmetrical behavior for the transconductance as show in Fig. 28.

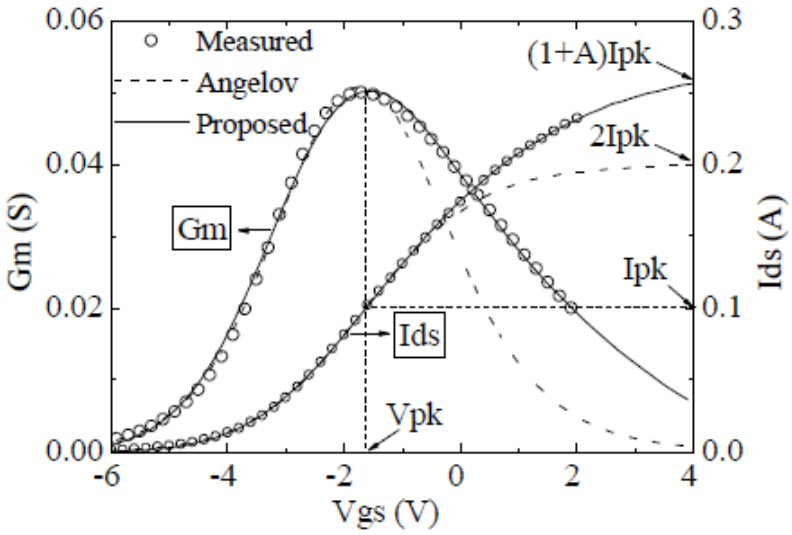

Fig. 28: Measured and modeled *Ids* and transconductance versus *Vgs* for Lin-He Model [33]

3.2.4 Yuk-McQuate model

The Yuk-McQuate model is also based on the I-V fitting principle found in the Angelov model. The drain current equation is developed and is based on [31]. The new model can be written as [37]:

$$I_{ds} = I_{pkth} * (1 + \text{Mipk} * \tanh(\psi)) * (1 + \lambda * Vds) * \tanh(\alpha * Vds) \quad (26.a)$$

$$\psi = P1th * (Vgs_{eff} - Vpk1) + P2th * (Vgs_{eff} - Vpk2)^2 + P3th * (Vgs_{eff} - Vpk3)^3 \quad (26.b)$$

$$Mipk = 1 + 0.5 * dMipk * (1 + \tanh(\psi_m)) * \tanh(a * V_{ds}) \quad (26.c)$$

$$\psi_m = Q_m * (Vgs_{eff} - Vgs_M) \quad (26.d)$$

$$dMipk = Mipkth - 1 \quad (26.e)$$

$$P_n = (P_{n0} + P_{n1} * V_{ds}) * \tanh(a_{Pn} * V_{ds}) + P_{n0} \quad (26.f)$$

$$Q_m = (P_{Q0} + P_{Q1} * V_{ds}) * \tanh(a_Q * V_{ds}) + P_{Q0} \quad (26.g)$$

Where Pn parameters are model parameters and coefficient of ψ. Mipk is hyperbolic-tan's function multiplier for peak current, Ipk. ψ_m controls the shape of the multiplier Mipk as a function of Vgs centered around VgsM. Also, Qm is the coefficient for.

ψ_m, and Mipk is the upper bound for Mipk. Where $P_{n0}, P_{n1}, \alpha_{P_n}$ describe the V_{ds} relationships for P_n; $P_{m0}, P_{m1}, P_{m2}, P_{m3}$, describe the V_{ds} relationships for $\mathrm{M_{ipkb}}$; and P_{Q0}, P_{Q1}, α_Q describe the V_{ds} relationships for Q_m. In this model, Ids the shown formulation of drain-current equation accurately represents the highly asymmetric bell-shaped gm of the high power GaN HEMT transistors in contrast to what was developed in the Angelov model. The main modifications applied in this model are two things. The first one is writing the voltage at which peak transconductance occurs, V_{pk}, such that it has unique value to each polynomial term in ψ. The described modification allows the whole transconductance curve to be shifted. The second modification allows the transconductance curves to be elongated for gate-source voltages beyond V_{pk} using the $\mathrm{M_{ipk}}$ multiplier. The second modification is shown in Fig. 29.

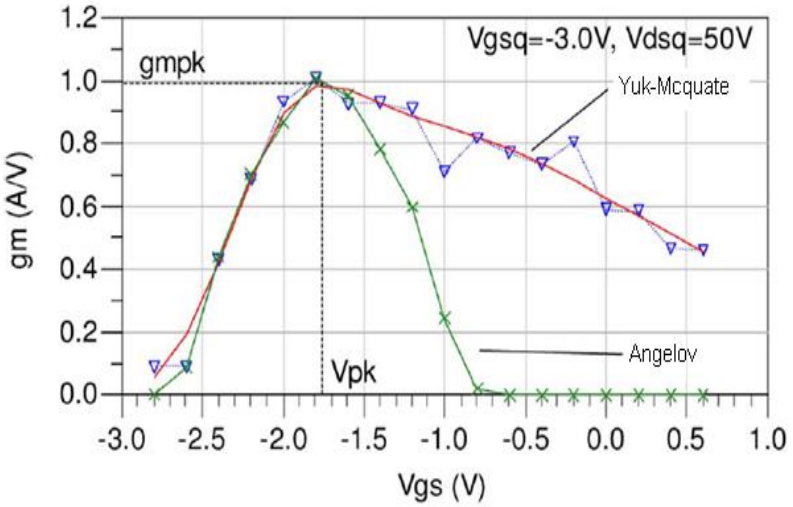

Fig. 29: Elongation of transconductance of Yuk-McQuate vs Angelov Models [35]

3.2.5 Cao Model

The Cao model is also an empirical model which was originally developed for MESFET devices but also can work with HEMT devices. The focus of this model is to improve the accuracy of saturation voltage and channel length modulation coefficients. The reason why the coefficient of the saturation velocity needs to be adjusted is because the knee voltage may heavily vary with applied gate-source voltage. The drain current expression that the model proposes is given as follows [38]:

$$I_{ds} = I_{dss0} * \left(1 - \frac{V_{gs}}{V_t}\right)^2 * \left(1 + \lambda(V_{gs}) * V_{ds}\right) * \tanh\left(a(V_{gs}) * V_{ds}\right) \qquad (27.a)$$

$$\lambda(V_{gs}) = \lambda_0 + P_1 * V_{gs} \quad (27.b)$$

$$a(V_{gs}) = a_0 + P_2 * V_{gs} \quad (27.c)$$

Where V_t is the threshold voltage of the transistor, I_{dss0} is linearly extrapolative drain saturation current at zero applied gate voltage, λ_0 is the channel length modulation coefficient zero applied gate voltage, a_0 is the saturation voltage coefficient at zero applied gate voltage, P_1 and P_2 are fitting parameters. In this model, channel length modulation and saturation voltage are considered to be varying with applied gate voltage. The second order function, $\left(1 - \frac{\mathrm{Vgs}}{\mathrm{Vt}}\right)^2$, is used to ensure that the drain current falls to zero when $V_{gs} < V_t$.

3.2.6 Fager model

The purpose of this model is to increase the accuracy of the derivatives of the drain current. This model offers higher flexibility in modeling transconductance and its derivatives by allowing deploying more flexible functions to describe the highly asymmetric behavior of transconductance. This model is given as follows [39]:

$$I_{ds}(V_{gs}, V_{ds}) = \beta * \left(\frac{V_{gs3}^2}{1 + \frac{V_{gs3}^{plin}}{V_L}} \right) * (1 + \lambda * V_{ds}) * \tanh\left(\frac{a * V_{ds}}{V_{gs3}^{past}} \right) \quad (28.a)$$

$$V_{gs3} = VST * \ln\left(1 + exp\left(\frac{V_{gs2}}{VST}\right)\right) \quad (28.b)$$

$$V_{gs2} = V_{gs1} - 0.5 * \left(V_{gs1} + \sqrt{(V_{gs1} - VK)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2} \right) \quad (28.c)$$

$$V_{gs1} = V_{gs} - V_t \quad (28.d)$$

Where β is peak current, λ is channel length modulation, a is knee voltage parameter, VST is fitting parameter, VK is voltage at which drain current compresses and Δ is range required for V_{gs2} function to change from linear to saturation behavior. The important point that this model tackles is accuracy of drain current at sub-threshold conduction and soft turn-on. This point is reflected in the V_{gs3} equation. The second function V_{gs2} reflects the gate voltage saturation as shown in Fig 30. V_{gs2} implies that any further increase in gate voltage, there will be significantly low drain current value changes (drain current compression). As a result, the collapse

behavior of the transconductance is assured as shown in Fig. 31 [40]. It can be noticed from the drain current equation that the argument of tanh function reproduces the displacement of the knee voltage with certain applied gate voltage.

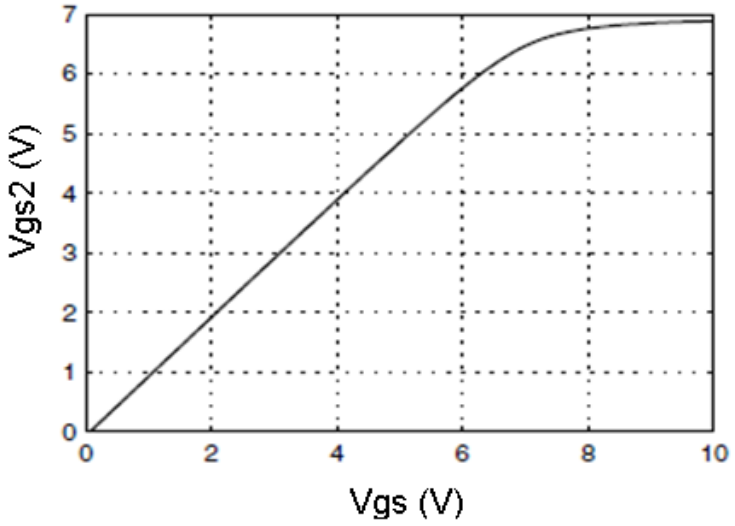

Fig. 30: Saturation of gate voltage [2]

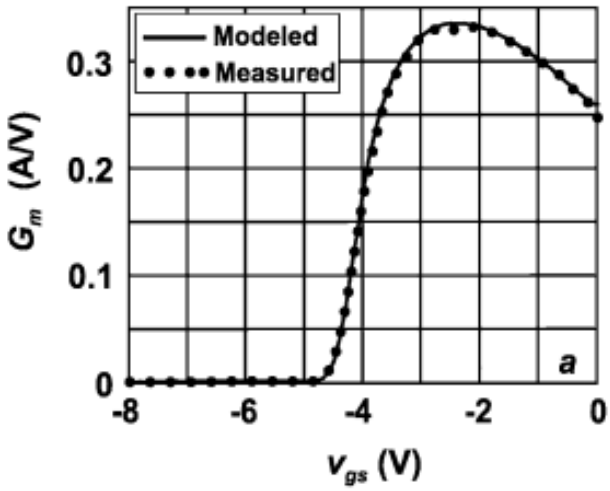

Fig. 31: Typical transconductance for HEMT device [40]

3.2.7 Lin-Ji model

The main objective of this model is to improve the behavior of the large signal model in terms of drain current accuracy and its derivatives as well as intermodulation distortion simulations [41]. Unlike what was done previously, the drain current equation is written in terms of its Taylor series as a function of static drain current, transconductance and its derivatives, output conductance and its derivative up to third-order terms as shown in equation 29.

$$I_{ds}(V_{gs},V_{ds}) = I_{ds}(V_{gs0},V_{ds0}) + Gm * V_{gs} + Gds * V_{ds} + Gm2 * V_{gs}^2 + Gd2 * V_{ds}^2 + Gmd * V_{gs} * V_{ds} + Gm3 * V_{ds}^3 + Gm2d * V_{gs}^2 * V_{ds} + Gmd2 * V_{gs} * V_{ds}^2 + Gd3 * V_{ds} \quad (29)$$

Where $I_{ds}(V_{gs0},V_{ds0})$ is called the static DC operating point, and lower term V_{gs} and V_{ds} are time varying parameters. The other difference that this proposes is that it utilizes cosine function in order to capture the behavior of the transconductance, Gm, as shown in equation 30.a.

$$I_{ds} = I_{sat} * 0.5 * \left(1 - \cos(\pi * V_{gs3})\right) * \tanh(a * V_{ds}) * (1 + \lambda * V_{ds}) \quad (30a)$$

$$V_{gs3} = P1 * V_{gs2} + P2 * V_{gs2}^2 + P3 * V_{gs2}^3 \quad (30b)$$

$$V_{gs2} = \frac{\frac{V_{gs1}}{V_k - V_t}}{\left(1 + \left(\frac{V_{gs1}}{V_k - V_t}\right)^n\right)^{1/n}}, V_k > V_t \quad (30c)$$

$$V_{gs1} = \frac{1}{m} * \ln\left(1 + exp\left(m * (V_{gs} - V_t)\right)\right) \quad (30d)$$

It can be noticed that the Fager model forms the basis operation for this model. Unlike the Fager model, higher order power series terms shown in equation 30.b are used in order to increase the reliability of the model as higher derivatives of drain current equation are calculated. The importance of cosine used in the above equation is that its derivative is $\sin(\pi * V_{gs3})$. As a result, this model account for the shift of the derivative of the transconductance around its peak value as shown in Fig. 32.

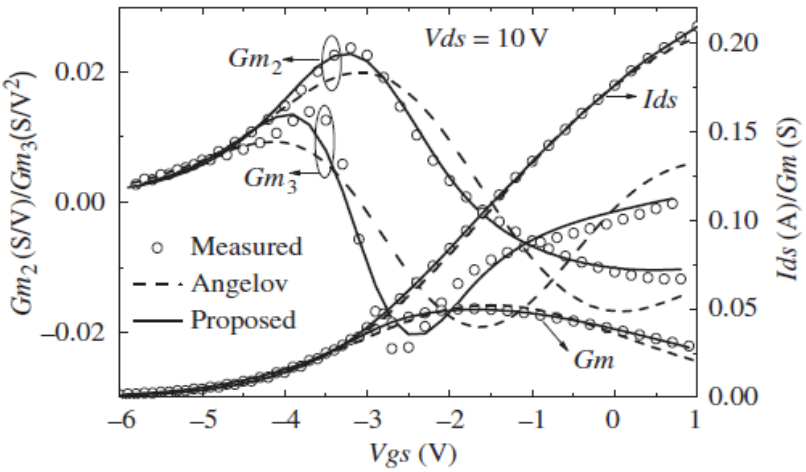

Fig. 32: Modeled (lines) Vs. Measured (dots) drain current and transconductance and its derivatives [41]

3.2.8 Genetic-Neural model

Neural network models can be used to predict the behavior of a transistor's drain current. A neural network contains three different layers: input layer, hidden layer and output layer. The input layer holds two vectors: gate-source voltage and drain source voltage. The hidden layer relates the input layer to output layer through various weights as shown in Fig. 33 [42]. The output layer (Y) contains a matrix of drain current measurements. At each neuron, an activation function, f(.), is required to map input layer to output layer. Also, the activation function will be chosen as a hyperbolic-tan function for this kind of mapping. The mathematical representation of the neural network found in Fig. 33 is shown in equation 31. Where Y represents I_{ds}.

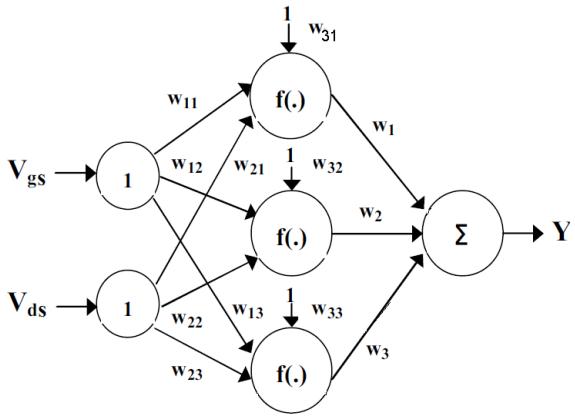

Fig. 33: Neural network structure [42]

$$Y = \sum_{i=1}^{3} w_i * f\left(w_{1i}V_{gs} + w_{2i}V_{ds} + w_{3i}\right) \tag{31}$$

Since this model has 12 different optimization parameters, the Genetic algorithm which is a global optimization algorithm should be used to train the neural network and helps the objective function, *E*, shown in equation 32 avoid a local minimum.

$$E = \frac{1}{M}\sum_{m=1}^{M}\left(Y_{act,m} - Y_{sim,m}\right)^2 \tag{32}$$

Where $Y_{act,m}$ is the m^{th} measured admittance and $Y_{sim,m}$ is the m^{th} simulated admittance. The intuition of using the genetic-neural modeling technique came from the fact that the backpropagation methods used earlier to determine the network's weights have shortcomings such as low convergence speed and can be easily trapped

in a local minimum [43]. Furthermore, the main advantage of using the genetic-neural model to predict drain current behavior is its accuracy and it does not require any assumption of any type of analytical functions to be used [44].

3.2.9 Angelov Soft-Breakdown model

The Angelov Soft-Breakdown model is a one that extends the original Angelov model into the soft drain-source breakdown effect region [45]. In his research work, he showed that many GaAs devices show at low voltages (close to pinch off), the drain current is very close to the exponential behavior. Also, Angelov noted that this soft breakdown gets masked by thermal heating effects. This is the reason why soft breakdown is smaller at higher input voltages. The modification on the original Angelov model is show in equation 33.

$$I_{ds} = I_{pk}(1 + \tanh(\psi)) \tanh(aV_{ds}) (1 + \lambda V_{ds} + L_{sb}) \quad (33.a)$$

$$L_{sb} = L_{sb0}\left[\exp\left(L_{sd1}V_{dgt} + \cdots\right) - 1\right] \quad (33.b)$$

$$V_{dgt} = \frac{V_{ds} - K_{trg}V_{gs}}{V_{tr}} \ , L_{sd1} = L_{d1}\left(1 - L_{g1}V_{gs}\right) \quad (33.c)$$

L_{sb0} and L_{sd1} are coefficients matching the drain current dependencies. Also, V_{dgt} combines the gate and drain voltages such that soft breakdown characterized by L_{sb} will be masked by thermal effect as shown in Fig. 34 at higher input voltages.

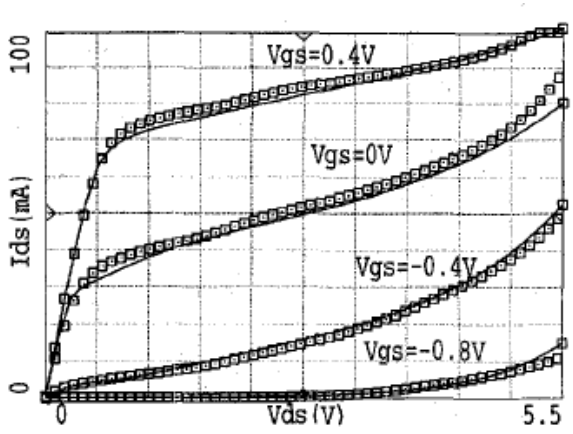

Fig. 34: Drain current characteristics showing soft breakdown, measurements (squares), modeled (solid lines) [45]

As seen from this chapter, there are different ways towards developing a comprehensive large signal model (DC and parasitic element extraction). Each

modeling approaches tackles a different transistor's characteristics. The main step in developing a comprehensive large signal model is to first develop a DC model that can be incorporated in the extraction of parasitic elements. In the next chapter, a developed DC model that shows better derivatives is discussed. Also, the improved model is extended to cover Kink Effect and Soft Breakdown characteristics of HEMT devices. Finally, an efficient hybrid algorithm will be developed in order to reduce the number of steps taken to develop a complete large signal model.

Chapter 4: Proposed Large Signal Modeling for FET and HEMT Devices

4.1 Improved and Extended DC Modeling for FET and Lattice-Mismatched HEMT Devices

To obtain a model for a transistor, DC and s-parameters' measurements should be done for complete characterization. The first step in building a model is to start modeling the DC characteristics of the device. Then the DC model can be incorporated in the parasitic parameter extraction while modeling the measured s-parameters (or y-parameters). Each model has its own approach to model the DC characteristics in order to improve upon the accuracy of that model. Inaccurate representation of the device leads to relatively wrong circuit design when sizing the transistor using the g_m/I_{DS} technique. Furthermore, inaccurate representation of the device can lead to a relatively wrong harmonic distortion simulation. The reason is that the harmonic distortion simulation is based on the modeled transconductance as proved in [46].

As seen from the literature, there are many ways to represent the drain-source current using behavioral modeling techniques. Three main ways are used to represent the variation of drain current as a function of gate-source voltage:

- Square law: Cao model, Curtice model.
- Peak transconductance location: Angelov model, Liu-He model, Yuk-McQuate model.
- Compression point behavior: Fager model, Lin-Ji model.

Each of the models has different error performances as will be shown later. For example, in theory, the Liu-He model, Fager model and Yuk-McQuate model improve upon the issue of transconductance elongation beyond peak transconductance which is caused by drain current compression. However, it is shown that the Fager model achieves transconductance elongation with fewer number of parameters. However, it is observed that some parameters are holding back the Fager model from obtaining better accuracy. For example, the Fager model depends on parameter *VK* and Δ to represent the voltage at which the current compression point starts and voltage range for which V_{gs2} function goes from linear to saturated behavior, respectively. Though, the function V_{gs2} was not found to be very smooth when

applied to NMOS transistor. In this thesis work, the argument of V_{gs2} function is changed to a hyperbolic tangent function with higher order power series of the input effective voltage. The mathematical description of the proposed model is as follows:

$$Vgs_{eff} = v_{GS} - Vt \tag{34.a}$$

$$Vgs2 = p1 * \tanh\left(\sum_{i=1}^{3} x_i * Vgs_{eff}^{i}\right) \tag{34.b}$$

$$Vgs3 = k * \ln\left(1 + \exp\left(\frac{Vgs2}{k}\right)\right) \tag{34.c}$$

$$Ids0 = \beta \frac{Vgs3^2}{1 + \frac{Vgs^{plin}}{VL}} * (\lambda_0 + \lambda_1 * Vds) * \tanh\left(\frac{a * Vds}{Vgs3^{psat}}\right) \tag{34.d}$$

Where:

- a is knee voltage parameter.
- λ_0 and λ_1 are channel length modulation parameters.
- β is peak drain current.
- Vgs_{eff} is effective input voltage.
- V_{gs2} is an intermediate function.
- V_{gs3} simulates non-linearity behavior of drain current with respect to gate voltage only.

It is seen from the above equations that: *p1*, x_i, *k*, β, λ_0, λ_1, *VL*, *plin* and *psat* are optimization parameters. In order to determine the values of those parameters, Genetic Algorithm will be used. The Genetic Algorithm (GA) is a direct, parallel, stochastic method for global search and optimization, which imitates the evolution of living beings, described by Charles Darwin. GA is part of the group of Evolutionary Algorithms (EA). The evolutionary algorithms use the three main principles of natural evolution: reproduction, natural selection and diversity of the species, maintained by the differences of each generation with the previous. The Genetic Algorithm works with a set of individuals, representing possible solutions of the task. The selection principle is applied by using a criterion, giving an evaluation for the individual with respect to the desired solution. The best-suited individuals create the next generation. The flow of the Genetic algorithm is shown in Fig. 35. The steps are described as follows:

1) Initialize a random population.

2) Evaluate each probable solution in the population using certain fitness/objective function.
3) Select the solutions with the best objective function evaluation.
4) Perform crossover to create new population from the selected solutions, and also perform mutation which means randomly change a probable solution to create new population.
5) Check if error is less than tolerance. If not, go to step 1.

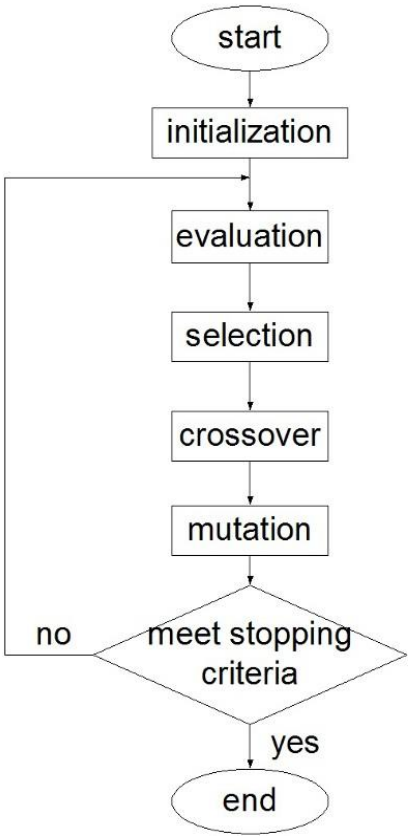

Fig. 35: Genetic Algorithm [47]

The objective function, *E*, that will be used to map the measured drain current to the proposed model will be as follows:

$$E = \sum_{i=1}^{Nvgs} \sum_{j=1}^{Nvds} (I_{dsm} - I_{ds0}(Vgs_i, Vds_i))^2 \quad (35)$$

Where *Nvgs*, and *Nvds* are number of gate-source voltage and drain-source voltage axis points obtained from measurements, and I_{dsm} is the measured drain current data points, and I_{ds0} is the proposed model. To perform DC characterization of the device under test, pulse DC sources will be used with different configurations in order to obtain either drain current as a function of drain bias voltage (while sweep is done on gate voltage) or gate bias voltage (while sweep is done on drain voltage). Fig. 36 and

37 show the necessary connection implemented to obtain $I_{ds} - V_{gs}$ and $I_{ds} - V_{ds}$, respectively. Dashed lines in the figure dictate no wire or BNC cable connection. The solution of the proposed model is shown in Fig. 38 to 40.

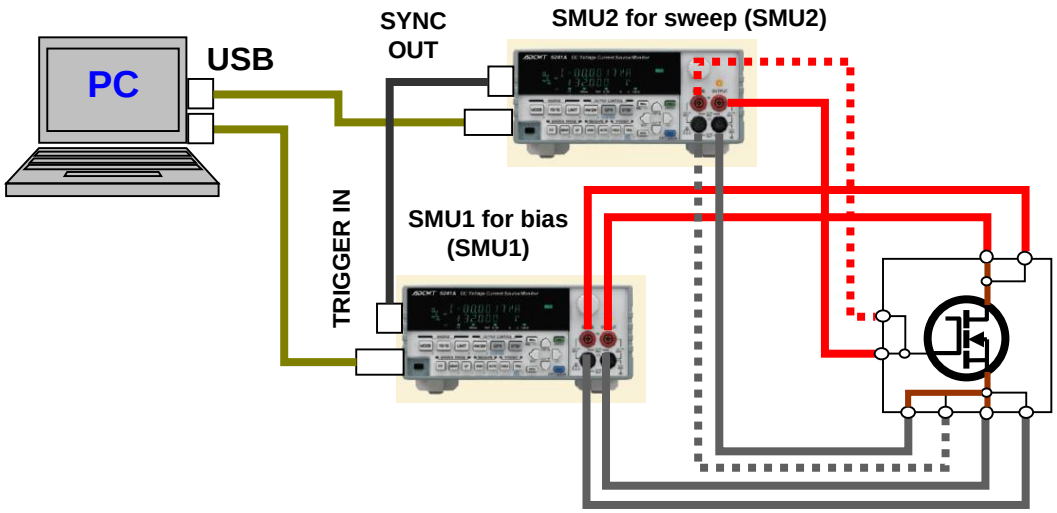

Fig. 36: Measurement setup for $I_{ds} - V_{gs}$ relation [56]

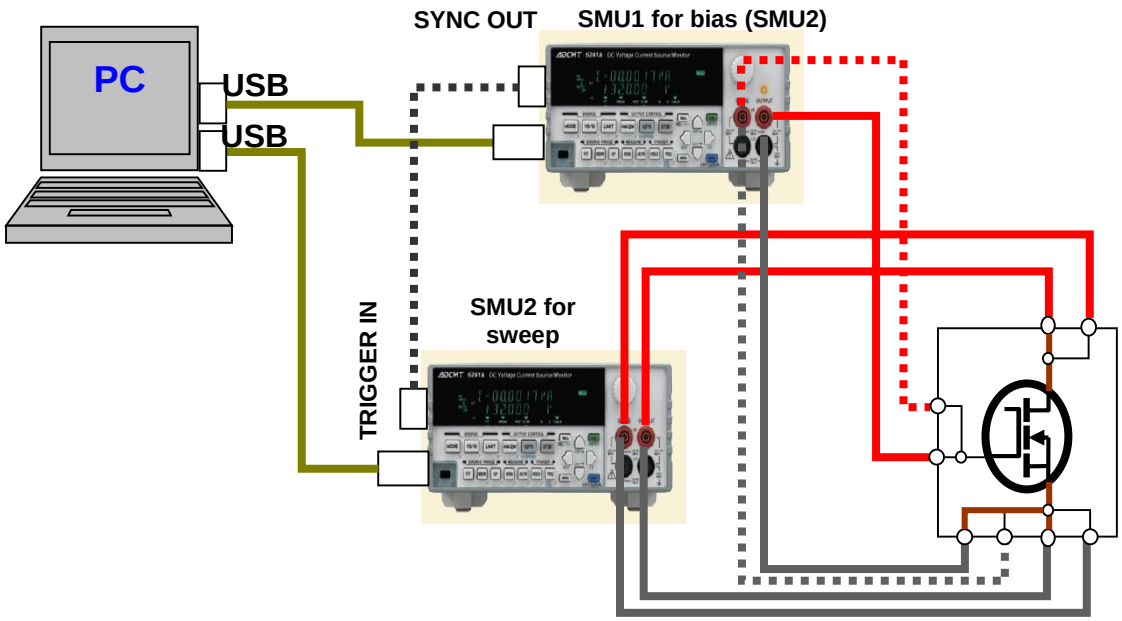

Fig. 37: Measurement setup for $I_{ds} - V_{ds}$ relation

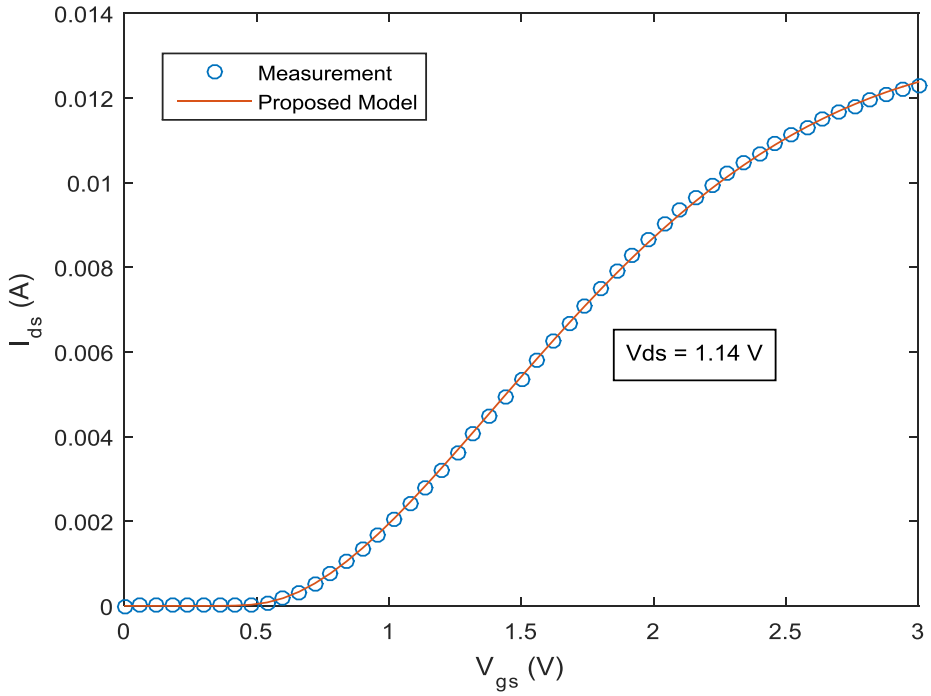

Fig. 38: Drain current at Vds =1.14 V

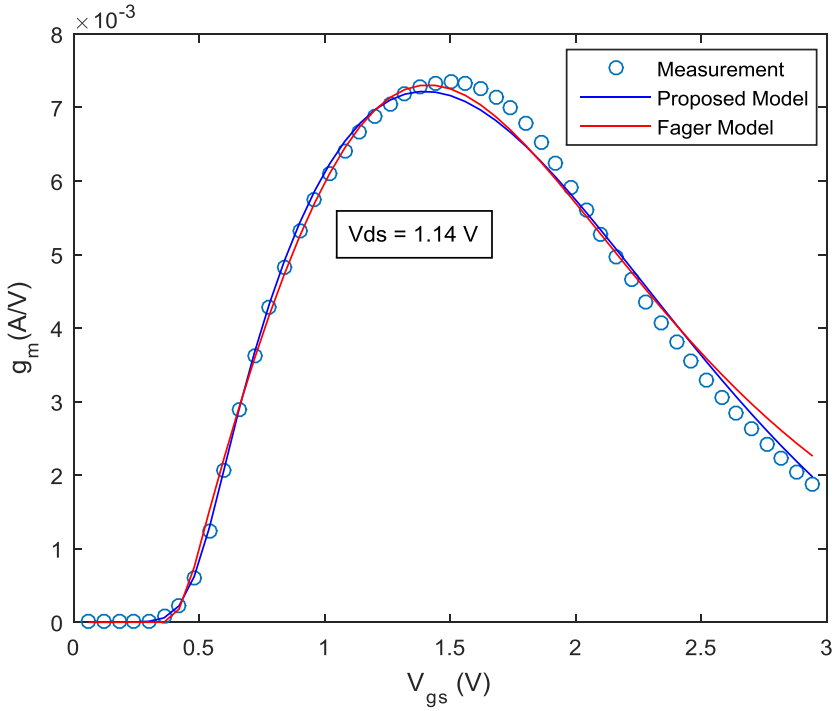

Fig. 39: Transconductance at Vds =1.14 V

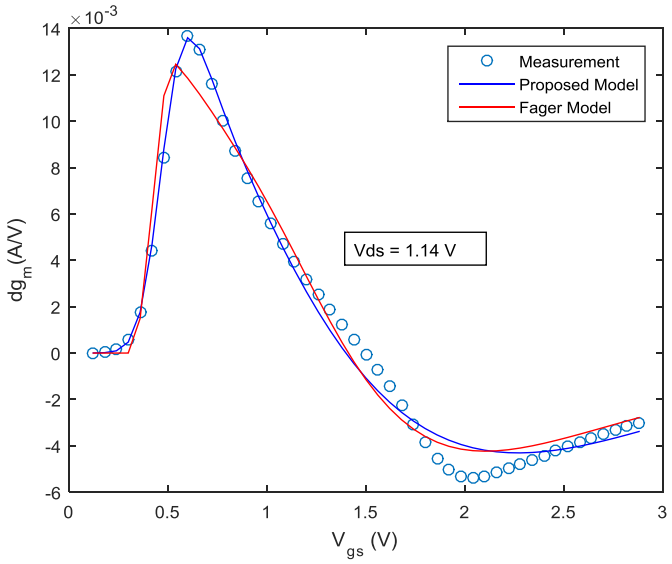

Fig. 40: Derivative of transconductance at Vds =1.14 V

The proposed model can also be applied to different type of transistors such as LDMOS, MESFET and HEMT devices. However, in some cases of HEMT devices, kink effect and soft breakdown can be noticed in the DC characteristics of the device. There are models that are developed to describe the soft breakdown behavior of HEMT devices such as the Angelov extended model in [45], yet, this extended model only accounts for soft breakdown for lower drain voltages. Regarding kink effect, there are look-up tables that are used to accurately simulate this effect such as the one in [53]. However, look-up tables are relatively not accurate when it comes to simulating high-order distortion products since a table-based model does not have a well-defined derivative as compared to functions.

A model combining both kink and soft breakdown effects was not found in the literature. Therefore, the proposed model will be adjusted to account for both phenomena using a single time-independent drain current model. Also, the drain voltage range of the model will be further extended unlike the Angelov extended model. The proposed mathematical formulation for kink and soft breakdown effects goes as follows:

$$v_{gs1} = v_{GS} - v_t \tag{36.a}$$

$$v_{gs2} = p1 * \tanh\left(p2 * v_{gs1}\right) \quad , \quad v_{gs3} = VST * \ln\left(1 + exp\left(\frac{v_{gs2}}{VST}\right)\right) \tag{36.b}$$

$$m = \tanh\left(A7 * V_{gs1} + A8\right) * e^{-A9 * v_{gs} + p3} \tag{36.c}$$

$$KB = A0 + A1 * e^{A2*v_{DS}-A3-A4*v_{gs}} + m * A10 * e^{A13*\tanh(A11*v_{DS}+A12)+A14)} \quad (36.d)$$

$$KV = a * \operatorname{sech}(A15 * v_{gs}) + A16 * v_{gs}^2 + A17 * v_{gs}^3 \quad (36.e)$$

$$i_{DS} = B * \frac{v_{gs3}^2}{1 + \frac{vgs_3^{plin}}{VL}} * (1 + L * v_{DS}) * \tanh\left(KV * \frac{v_{DS}}{v_{gs3}^{psat}}\right) * KB \quad (36.f)$$

- $plin, VL, VST,\ psat,\ p_i, A_i$ are optimization parameters.
- B and m are saturation current and masking function for kink effect, respectively. L is channel length modulation parameter.
- KV simulates knee voltage as a function of gate-source voltage.
- KB is a function that extends the modeled drain current from saturation region to kink effect region then soft breakdown region.

The unknown optimization parameters will be determined by a hybrid algorithm: Genetic Algorithm with Newton's Method in order to further reduce the error between the measured and simulated drain current. Fig. 41 shows the measured versus simulated drain current including soft breakdown and kink effect for a GaAs HEMT device.

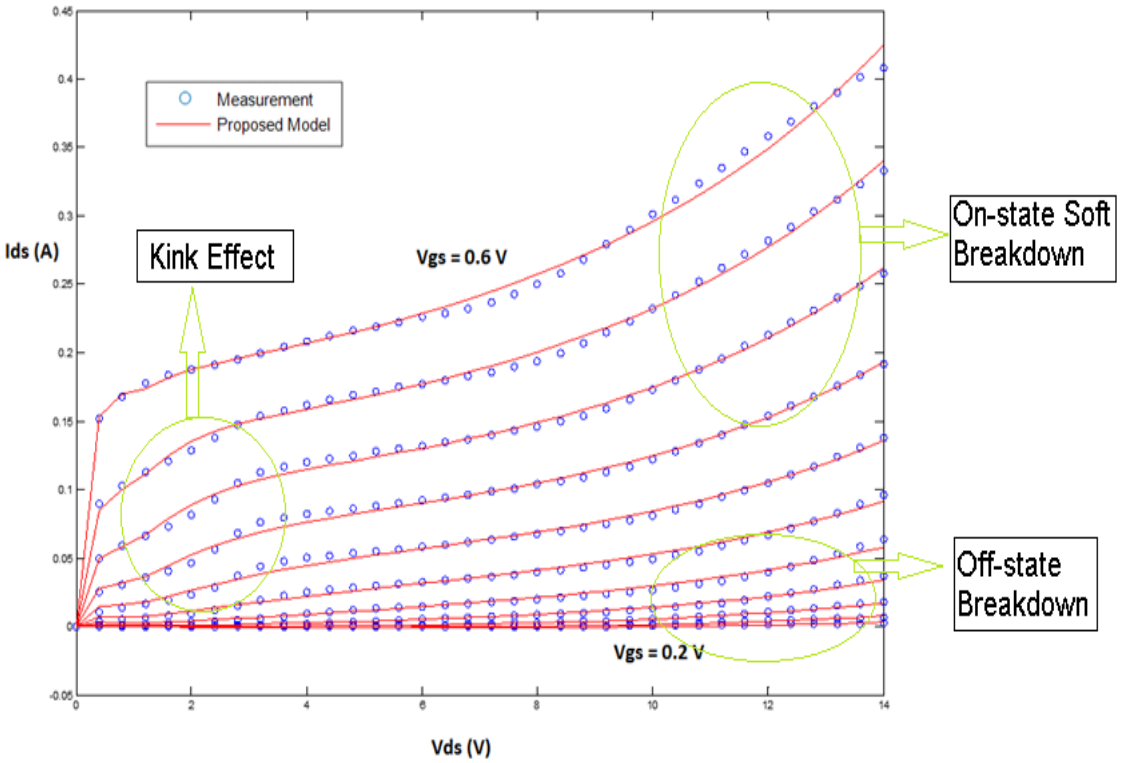

Fig. 41: Measured and simulated DC characteristics of GaAs HEMT

4.2 Efficient Parasitic Parameter Extraction for FET/HEMT Devices Using Hybrid NSGA-II-Newton Algorithm

Extracting parasitic parameters such gate-source and drain-source capacitances were extensively studied and implemented in the literature. There are various approaches to model a transistor: small and large signal modeling. In small signal modeling, parasitics are only obtained at single bias points whenever it is necessary to deal with small input voltages. However, it is required to obtain multi-bias model (large signal model) whenever it is necessary to deal with large input voltages. As described in the literature chapter, it is first required to obtain extrinsic parasitics at pinch-off s-parameters measurements ($V_{gs} = V_{ds} = 0$). The transistor model is reduced to the one in Fig. 42 at pinch-off conditions. Then, those parasitics should be de-embedded as described earlier. Then, the intrinsic part will be determined from forward bias s-parameter measurement. The intrinsic part of the transistor model can be described as in Fig. 43.

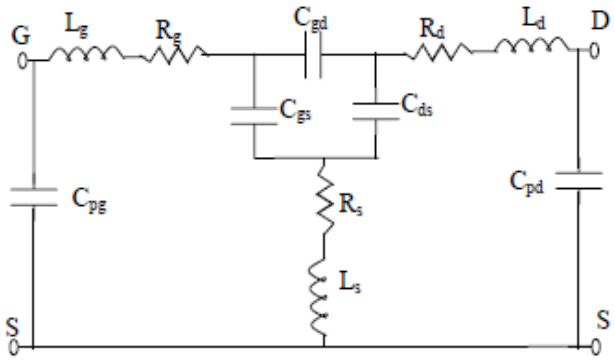

Fig. 42: Transistor model at pinch-off conditions [13]

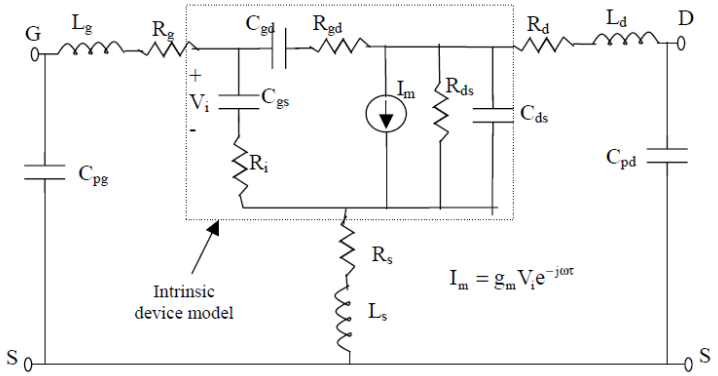

Fig. 43: General FET model including extrinsic and intrinsic parts [13]

The pinch-off capacitances can be obtained from low frequency y-parameters, and parasitic resistances and inductances can be obtained at high frequency z-parameters.

To obtain the intrinsic parasitics, s-parameter measurement should be converted y-parameters. Equations 37 show the derived y-parameters equation (when $R_{gd} = 0$) [13].

$$y_{11} = \frac{\omega^2 R_i C_{gs}^2}{\left|1 + j\omega R_i C_{gs}\right|^2} + jw\left(\frac{C_{gs}}{\left|1 + j\omega R_i C_{gs}\right|^2} + C_{gd}\right) \quad (37.a)$$

$$y_{12} = -j\omega C_{gd} \quad (37.b)$$

$$y_{21} = \frac{g_m \exp(-j\omega\,\tau)}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} \quad (37.c)$$

$$y_{22} = g_{ds} + j\omega(C_{ds} + C_{gd}) \quad 37.d)$$

All the capacitances will be determined from the slope of y-parameters (either real or imaginary parts). Transconductance and output conductance can be determined from DC measurements. R_i and τ (delay constant) are considered as optimization parameters. This model was used in different types of FET transistors in the literature. Furthermore, it showed excellent error performance in terms of representing measured s-parameters in the GHz-region. However, it was found that existing parasitics extraction techniques require many steps to reach to a final large signal model. In other words, if N multi-bias s-parameter measurements were obtained, it is required to perform N+2 (N+3 for MOSFET devices) optimizations in order to get a complete a large signal model. The additional 2 (or 3 for MOSFETs) optimizations come from the fact that after obtaining multi-bias C_{gs} and C_{gd} (also multi-bias C_{ds} for MOSFETs) points, those capacitances must be curve fitted or mapped to functions that represent their behavior. To reduce the number of steps it takes to model a device, multi-objective optimization will be used to obtain all multi-bias parasitics at the same time using single optimization run.

Multi-objective optimization, or Pareto optimization, is a mathematical process used whenever multiple criteria should be met, or a set of objective functions should be simultaneously minimized or maximized. Multi-objective optimization is used in many fields where optimal decisions have to be made for two or more conflicting objective functions [48]. In mathematical notations, a minimization problem for multiple objective functions can be written as:

$$\min_{x \in X} \left(f_1(x), f_2(x), \ldots., f_k(x)\right) \quad (38)$$

Where $f_k(x)$ is the k^{th} objective function, x is the decision vector containing the unknown parameters and X is the solution space. In real and practical problems, it is difficult to find a solution x that minimizes all objective functions. In other words, a state will be reached by optimization where improving one objective function will degrade the performance of the other. The solution x at which this happens is called Pareto optimal solution. As a result, finding Pareto optimal solutions are the ones of concern. A solution $x^1 \in X$ is said to dominate another solution $x^2 \in X$ if [48]:

1) $f_i(x^1) \leq f_i(x^2)$ for all indices {i=1,2,3,…,k}, or
2) $f_i(x^1) < f_i(x^2)$ for at least one index i

There are many variants of multi-objective optimization algorithm. For this thesis work, Non-dominated Sorting Genetic Algorithm II, NSGA-II, will be used [49]. The algorithm is based on two functions: non-dominating solution sorting and crowding distance metric. The first one classifies the probable solutions in the solution space into Pareto fronts (which is a set of Pareto optimal solutions), and the second one examines how diverse are the probable solutions (population) in order to avoid trapping in local minima. The algorithm goes as follows:

1) Create new random population, P_0 and Q_0. Then, create children of P_0, Q_0, using selection, crossover and mutation operators.
2) Create initial population R_t by joining P_0 and Q_0. Length of R_t will $2N$ since each P_0 and Q_0 is of length N.
3) Sort R_t by non-dominating solutions first with ranks {1,2,..,n} in order to identify the Pareto fronts.
4) Generate the next population, P_{t+1}, of size N using crowding distance metric.
5) Create the next children Q_{t+1} from P_{t+1} using selection, crossover and mutation.
6) Calculate objective functions for stopping criteria. If criteria are not met, start from step 1 again.

To prove that the algorithm can be used for the suggested parasitic parameter extraction, a general purpose NMOS device will be used. A capacitance model was

already developed in the literature for an NMOS device as shown in equations 39 [50].

$$C_{gs} = C_{gs-max} - C_{gs0}\left[1 + \tanh\left(\frac{s_1}{c_s}\left(V_{gs} - V_{s1}\right)\right)\right]\left[1 + \tanh\left(\frac{s_2}{c_s}\left(V_{gs} - V_{s2}\right)\right)\right] \quad (39.1)$$

$$C_{ds(gd)} = C_{ds0(gd0)}\left(\frac{\varphi + E_{ds}}{\varphi + V_{ds}}\right)^{m} \quad (39.2)$$

Where:

- $C_{gs(max)}$ is the oxide capacitance.
- C_{gs0} is a model fitting parameter.
- $C_s = (C_{gs(max)} - C_{gs(min)})/2$
- $s_1 = \left.\frac{\partial C_{gs}}{\partial V_{gs}}\right|_{V_{gs}=V_{s1}}$ and $s_2 = \left.\frac{\partial C_{gs}}{\partial V_{gs}}\right|_{V_{gs}=V_{s2}}$
- m is junction sensitivity.
- φ is the contact potential, a value of which depends on a doping profile.
- $C_{ds0(gd0)}$ is the junction capacitance when $V_{ds} = E_{ds}$.

The way to obtain the capacitance models for a device as suggested by the literature is to determine all capacitances at each bias point. Then perform curve on the capacitance data point in order to have a large signal model covering all voltage ranges. However, in the proposed algorithm, the capacitance models are directly fitted to the measured multi-bias s-parameters by means of multi-objective optimization. There are two main parts in the determining the parasitics at pinch-off and forward bias conditions. Furthermore, there should be four objective functions defining the multi-objective optimization:

1) The first two objective functions are dedicated to pinch-off s-parameter measurement. The main parameters that are important in modeling the pinch-off state of the device are: $R_g,\ R_s, R_d, L_d, L_g, L_s, C_{gs-max}, C_{ds0}, C_{gd0}$. In the pinch-off state, the s-parameter data should be segmented such that capacitances can be found in the low frequency region, and the parasitic inductances are found in the high frequency range. Objective (error) function E_1 is defined such that the capacitances C_{gs-max}, C_{ds0} and C_{gd0} are found in the low frequency region using y-parameters. Objective (error) function E_2 is

defined such that the parasitic resistances and inductances are found at high frequency z-parameters (where *meas.,k* and *sim.,k* are the kth measured and simulated data points respectively).

$$E_1 = \frac{1}{M}\sum_{k=1}^{M}\sum_{j=1}^{2}\sum_{i=1}^{2}\left(|y_{ij,\ low\ freq.}^{meas.,k} - y_{ij,\ low\ freq.}^{sim.,k}|\right)^2 \tag{40}$$

$$E_2 = \frac{1}{N}\sum_{k=1}^{N}\sum_{j=1}^{2}\sum_{i=1}^{2}\left(|Z_{ij,\ high\ freq.}^{meas.,k} - Z_{ij,\ high\ freq.}^{sim.,k}|\right)^2 \tag{41}$$

2) The second set of objective functions are dedicated to finding the rest of unknown parameters in the capacitance models at forward bias conditions. Objective function E_3 is used to minimize the error in measured and modeled y_{12} set. Objective function E_4 is used to minimize the error in measured and modeled data points of the rest of y-parameters. The reason behind separating y_{12} from the rest of y-parameters is that C_{gd} is curve fitted alone. As a result, a better convergence was observed.

$$E_3 = \frac{1}{M}\sum_{k=1}^{M}\left(|y_{12}^{meas.,k} - y_{12}^{sim.,k}|\right)^2 \tag{42}$$

$$E_4 = \frac{1}{M}\sum_{k=1}^{M}\sum_{j=1}^{2}\sum_{i=1}^{2}\left(|y_{ij}^{meas.,k} - y_{ij}^{sim.,k}|\right)^2,\ \ i,j \neq 1,2 \tag{43}$$

The proposed algorithm for parasitics extraction using multi-objective optimization goes as follows:

1) Create initial population size, P_0 and Q_0, containing all unknown values. The unknown values include extrinsic part's parasitics ($R_g,\ R_s, R_d, L_d, L_g, L_s$) and the intrinsic part's parasitics, which are the unknown values in the capacitance models in equations 39). Then, create children of P_0, Q_0, using selection, crossover and mutation operators.
2) Create initial population R_t by joining P_0 and Q_0. Length of R_t will be $2N$ since each P_0 and Q_0 is of length N.
3) De-embed the effect of ($R_g,\ R_s, R_d, L_d, L_g, L_s$) from s-parameters. Then convert the de-embedded s-parameters to y-parameters.

4) Calculate all Objective functions: $E1, E2, E3$ and $E4$.
5) Sort R_t by non-dominating solutions first with ranks {1,2,..,n} in order to identify the Pareto fronts.
6) Generate the next population, P_{t+1}, of size N using crowding distance metric.
7) Create the next children Q_{t+1} from P_{t+1} using selection, crossover and mutation operators.
8) De-embed the effect of $(R_g, R_s, R_d, L_d, L_g, L_s)$ from s-parameters. Then convert the de-embedded s-parameters to y-parameters.
9) Calculate all objective functions $E1, E2, E3$ and $E4$ for stopping criteria. If criteria are not met, start from step 5 again.

4.2.1) Parasitic Parameter Extraction Results and Modeling Recommendations:

In order to perform s-parameter measurement, Vector Network Analyzer (VNA) should be used. The connection of the device under test to a VNA is fairly simple as show in Fig. 44.

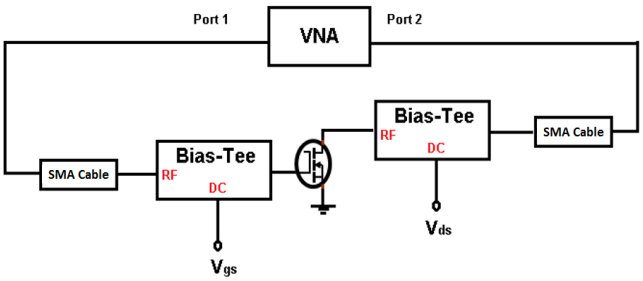

Fig. 44: s-parameter measurement setup

The transistor whose s-parameters were obtained for this thesis work was already mounted on a low cost FR4 material with SMA connectors. To de-embed the effect of the transmission lines of the PCB where the transistor was mounted, a separate PCB with no mounted transistor was developed in order to include the PCB's transmission lines' effects in the calibration process of the VNA. As a result, the obtained s-parameters are only unique to the transistor excluding the transmission lines insertion loss. However, this process created an additional problem while calibrating the VNA. Since there are female SMA connectors mounted on the PCB, an additional gold male SMA connector must be used when calibrating through-ports (port1-to-port2). On the one hand, the additional connector in the calibration process will not affect the real

part of s-parameters, but it will affect the imaginary part of S_{21} at high frequency. As a result, the transistor could only be modeled up to 20 MHz. On the other hand, the model used in this work to model an NMOS device was already shown in the literature to work up to GHz region. Therefore, in this work, the frequency range of the model is not of concern, since the proposed modeling solution is a modeling flow rather than a new model. Since the frequency range of the model is downgraded for this work, the second objective function described in the previous section can be ignored. Therefore, the first modeling recommendation is to model a die-based transistor (unpackaged) in order to reduce modeling variables and sources of error.

The second recommendation is to use a hybrid algorithm combining both the local minimum search (LMS) algorithm and global optimization. The reason is that better convergence was noticed when LMS was used. The hybrid algorithm that is used in this work is the NSGA-II-Newton's hybrid method. Fig. 45 shows great improvement in the solution of $\angle S_{11}$, as an example, when the output values of NSGA-II algorithm are used as initial points in Newton's method.

The Pareto front plot that shows the conflict between all objective functions is shown in Fig. 54. As illustrated in the figure, the Pareto optimal (X, Y, Z points) is chosen such that all objective functions are minimized without degrading the error performance of the other.

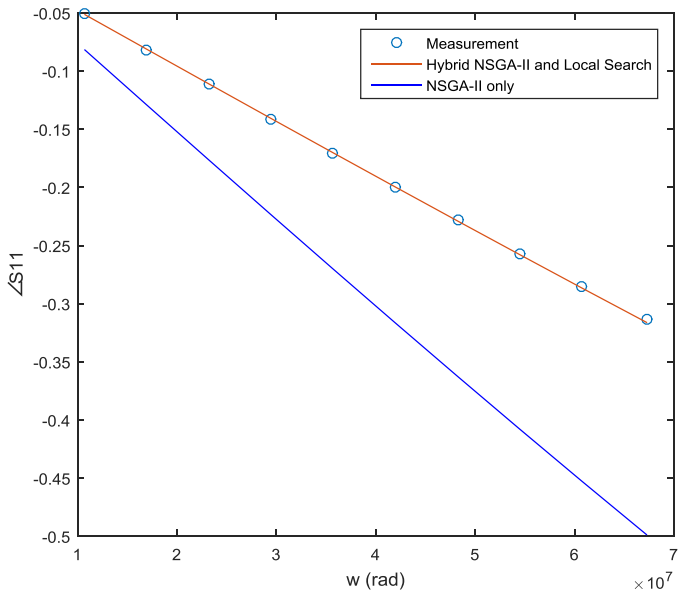

Fig. 45: Improvement over NSGA-II solution

The complete solutions for the multi-bias s-parameter model obtained from the hybrid algorithm are shown in Figs. 46-53.

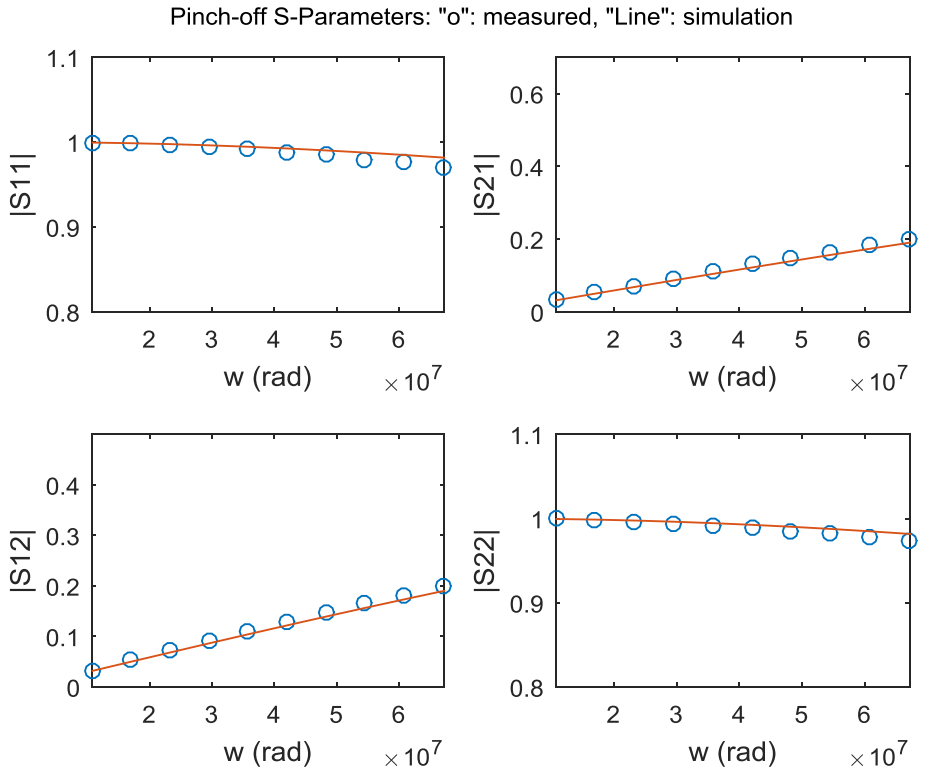

Fig. 46: Magnitude of pinch off s-parameters ($|S_{ij}|$)

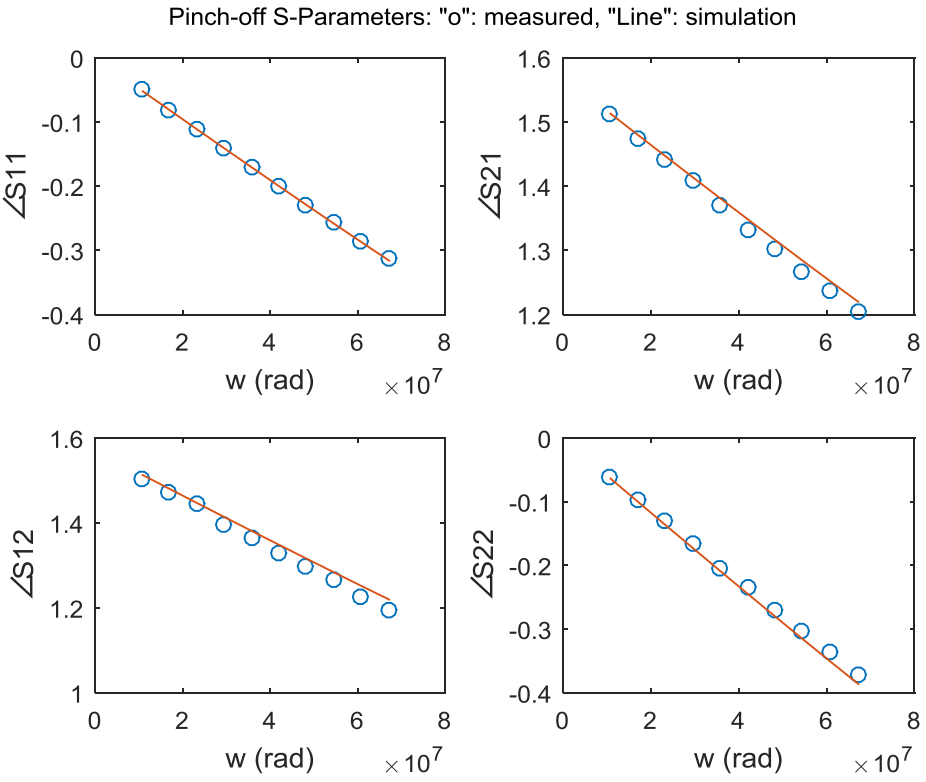

Fig. 47: Phase of pinch off s-parameters ($\angle S_{ij}$)

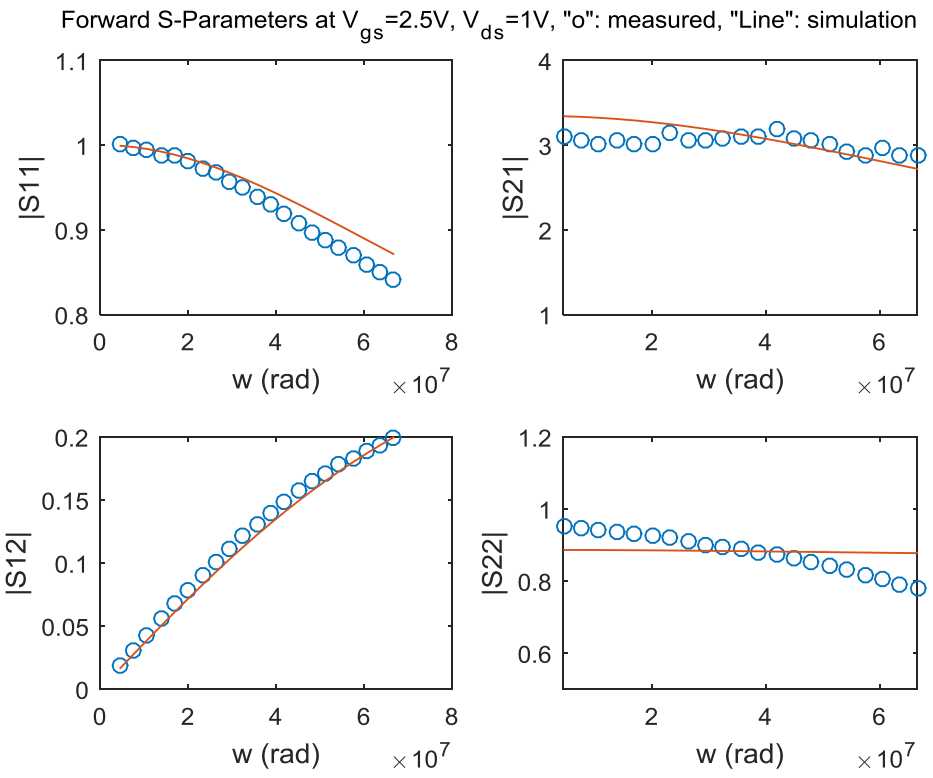

Fig. 48: Magnitude of s-parameters at $V_{gs} = 2.5V, V_{ds} = 1V$ ($|S_{ij}|$)

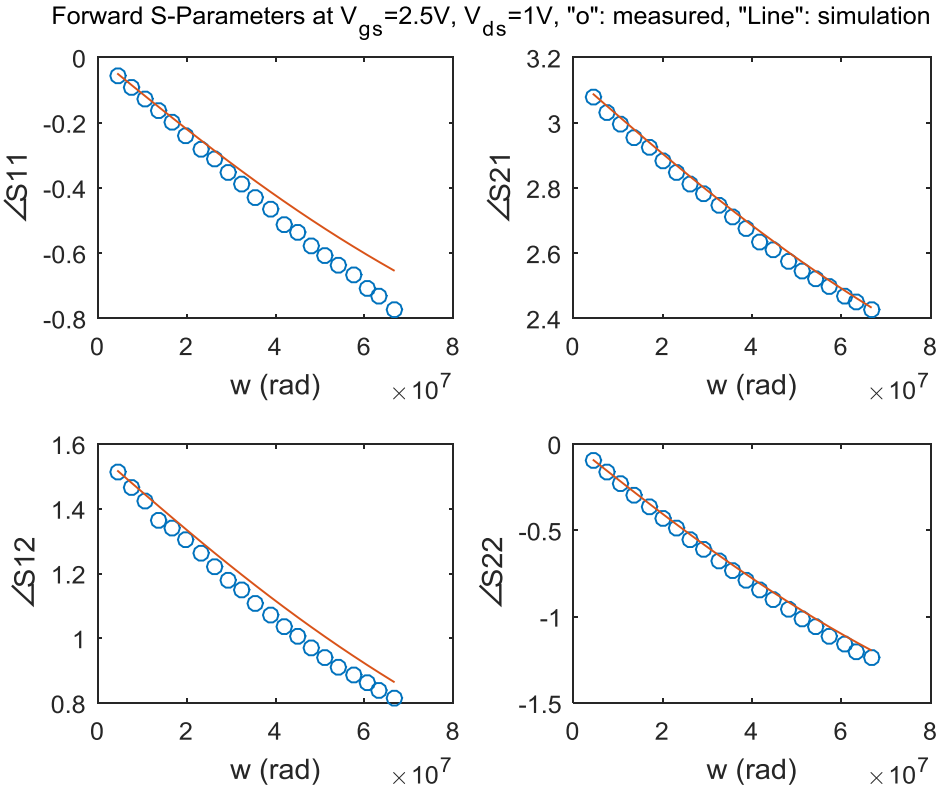

Fig. 49: Phase of s-parameters at $V_{gs} = 2.5V, V_{ds} = 1V$ ($\angle S_{ij}$)

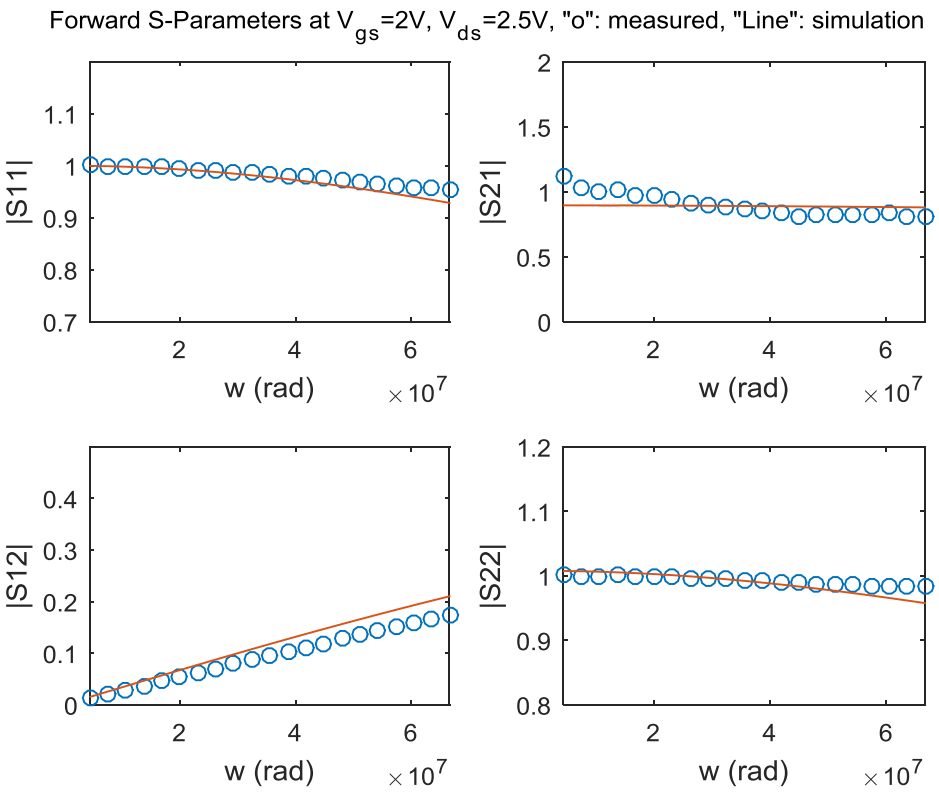

Fig. 50: Magnitude of s-parameters at $V_{gs} = 2V, V_{ds} = 2.5V$ ($|S_{ij}|$)

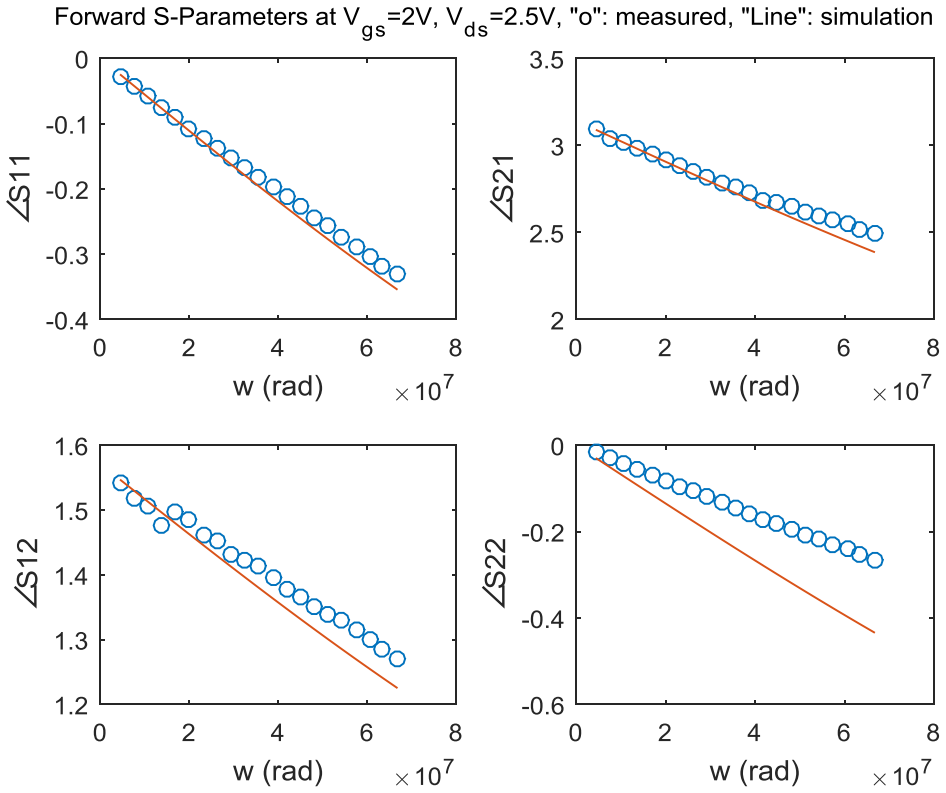

Fig. 51: Phase of s-parameters at $V_{gs} = 2V, V_{ds} = 2.5V$ ($\angle S_{ij}$)

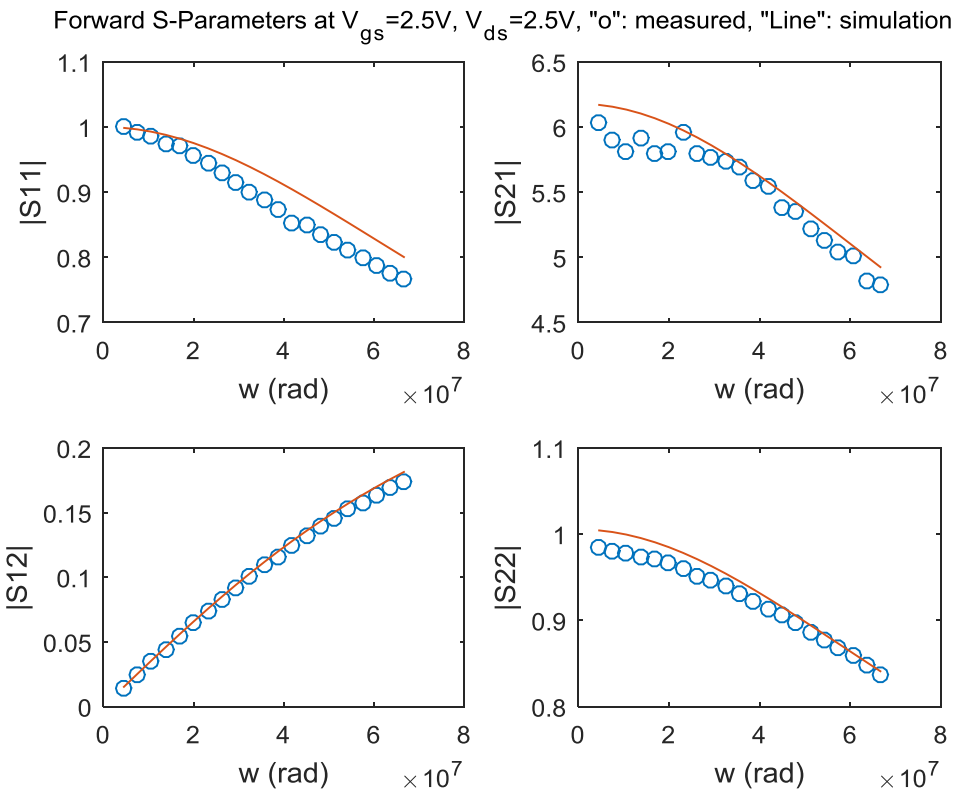

Fig. 52: Magnitude of s-parameters at $V_{gs} = 2.5V$, $V_{ds} = 2.5V$ ($|S_{ij}|$)

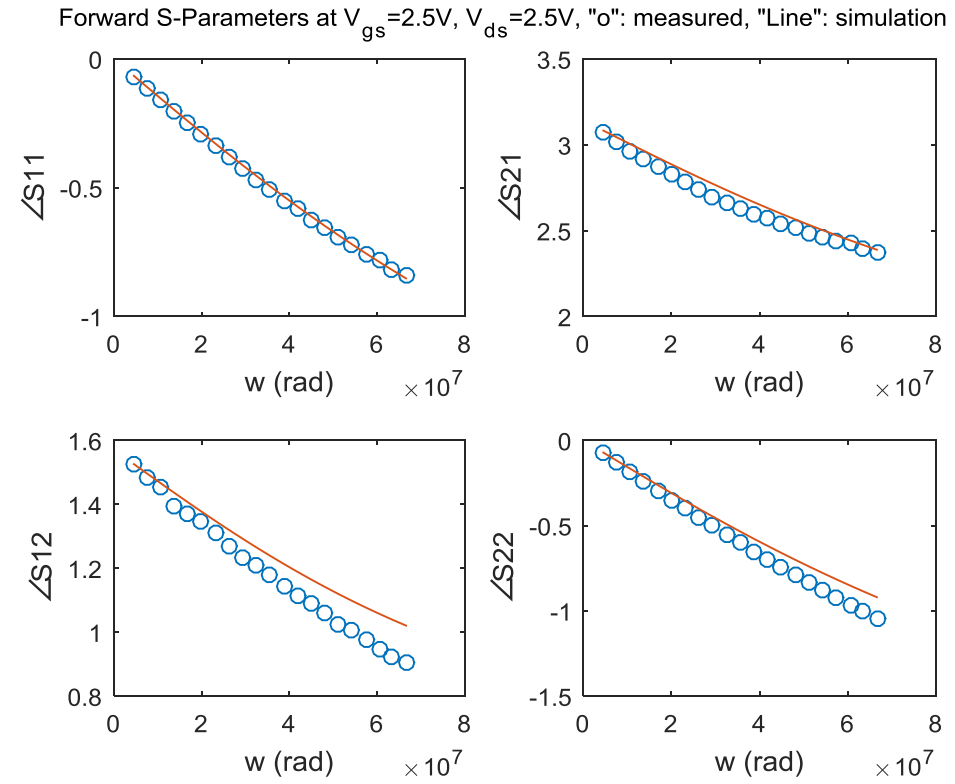

Fig. 53: Phase of s-parameters at $V_{gs} = 2.5V$, $V_{ds} = 2.5V$ ($\angle S_{ij}$)

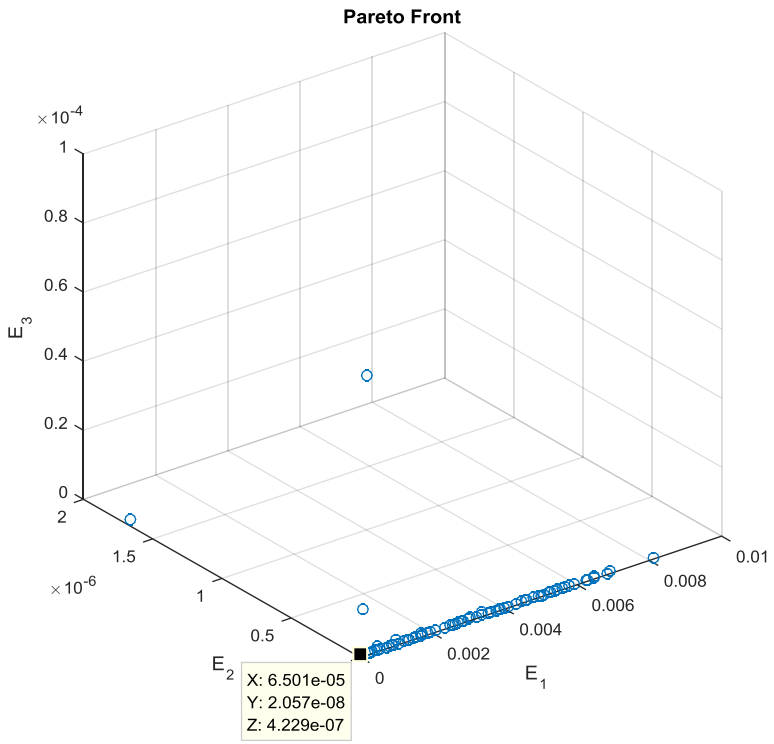

Fig. 54: Pareto front plot

The third modeling recommendation is to model a transistor using large signal measurements obtained from the Large Signal Network Analyzer (LSNA). Even though small signal s-parameter based modeling yield high accuracy, large signal measurements based modeling provides slightly higher accuracy as proved in [51]. The reason behind that is because capacitances can be obtained by means of measurements. However, in small signal s-parameters based modeling, capacitances' values are obtained by the slope of y-parameters. Unlike VNA's, LSNAs can provide currents and voltages at each port with respect to time as shown in Fig. 55.

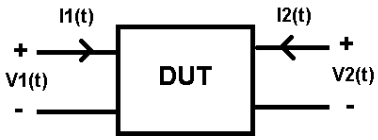

Fig. 55: Currents and voltages of a DUT

When currents and voltages are obtained in time domain, their amplitudes at DC and the fundamental frequency are known by converting the obtained time-domain waveforms to frequency-domain waveforms. When currents are known, the measured capacitances' values are obtained by the following relation [52]:

$$i_{GS} = \frac{\partial Q_{gs}(v_{gs}, v_{ds})}{\partial t} = C'_{GS}(v_{gs}, v_{ds}) * \frac{\partial v_{gs}}{\partial t} \tag{44}$$

The clear difference between small signal s-parameter based modeling and large signal based modeling can be seen when simulating the device in the linear region as shown in Fig. 56.

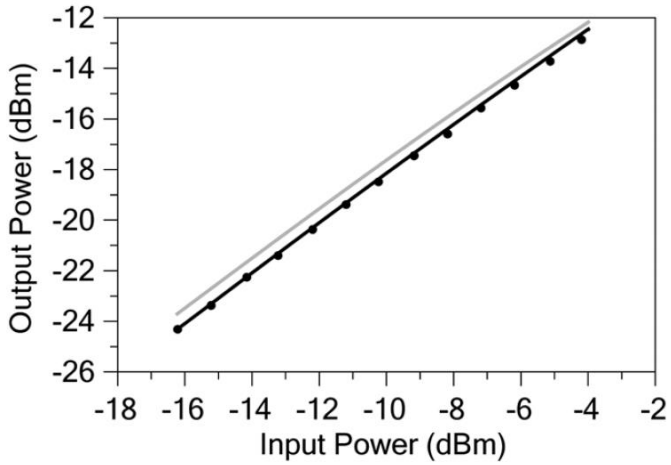

Fig. 56: Input/output power simulation: (dots) are measurement values, (grey line) is small signal s-parameter based modeling, (black line) is large signal based modeling [51]

Chapter 5: Conclusion and Future Work

5.1) Conclusion

The purpose of this research work was to introduce an improved large signal model that can be used for High Electron Mobility Transistors (HEMTs) and Field Effect Transistors (FETs) using behavioral modeling techniques. The discussed DC models in this study had different error performance. However, it was shown that the Fager model achieves good transconductance elongation with fewer number of model parameters. Therefore, the proposed model is based on the Fager model.

However, it was observed that some parameters are holding back the Fager model from obtaining better accuracy such as the ones in the intermediate function. The solution to improve the accuracy of Fager model was to use a hyperbolic-tan function whose input argument is power series of the input voltage. The result was improved derivative of drain current. With this kind of modification, the proposed drain current model can only work in the triode and saturation regions of the DC characteristics. Furthermore, the improved Fager-based model was extended to account for soft breakdown and kink effect. This extension was done by introducing masking function for kink effect region and exponential factor for soft breakdown region. However, it was difficult to choose a knee voltage function to have a good transition from triode region to kink effect region. As a result, the accuracy of the proposed DC model is slightly degraded at the knee region.

In addition to transistor's DC characteristics modeling, comprehensive steps for parasitic parameter extraction were discussed in details. The targeted elements were parasitic capacitances, parasitic resistances, and parasitic inductances in the intrinsic and extrinsic elements. In order to determine the mentioned parasitic elements, multi-bias s-parameter measurements were performed. A complete multi-bias s-parameter model was developed using a hybrid NSGA-II –Newton's optimization, Non Dominated Sorting Genetic Algorithm II combined with Newton's method. The reason is that NSGA-II is a global optimization algorithm that cannot guarantee the local minimum. In other words, when a hybrid algorithm was used, a significantly better convergence for all objective functions was observed.

After experiencing with this research work, three modeling recommendations were established. First recommendation is to model a die-based transistor (unpackaged) in order to reduce modeling variables and sources of error. Second recommendation is to use a hybrid optimization algorithm to improve upon the convergence of all objective functions. The final recommendation is to model a transistor using large signal measurements obtained from the Large Signal Network Analyzer rather than small signal s-parameters for more accurate model.

5.1) Future Work

Regarding future work, the proposed DC model should be improved in terms of accuracy at the knee voltage. In other words, the hyperbolic-secant function should be replaced be another one such that the transition from triode region to kink effect region should be much more accurate. Another modification that should be applied to the proposed model is to convert it to be dynamic with respect to time. The reason is that the proposed model does not take into account the electron release time constant from the traps.

References

[1] Parker, A.E.; Scott, J.B., "Intermodulation nulling in GaAs MESFETs," in *Electronics Letters* , vol. 29, no. 22, pp. 1961-1962, 28 Oct. 1993.

[2] Peter Aaen, Jaime Pla, *Modeling and Characterization of RF and Microwave Power FET's*. First Edition, Cambridge: Cambridge University Press, 2011.

[3] Koljonen, J., Alander, J.T., "Effects of Population Size and Relative Elitism on Optimization Speed and Reliability of Genetic Algorithms," *Proceedings of the 9th Scandinavian Conference on Artificial Intelligence*, pp. 25-27, 2006.

[4] Francesco Fornetti. "Characterisation and Performance Optimisation of GaN HEMTs and Amplifiers for Radar Applications." PhD Thesis, University of Bristol, United Kingdom, 2010.

[5] Trew, R.J., "High-frequency solid-state electronic devices," in *Electron Devices, IEEE Transactions on* , vol. 52, no. 5, pp. 638-649, May 2005.

[6] Haddad, G.I.; Trew, R.J., "Microwave solid-state active devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 760-779, Mar 2002.

[7] Donald A. Neamen. *Semiconductor Physics and Devices*. Singapore: McGraw-Hill Higher Education, 2003, pp. 350.

[8] B. Van Zeghbroeck. "Flat-band energy band diagram of a p-n heterojunction." Internet: http://ecee.colorado.edu/~bart/book/book/chapter4/gif/fig4_3_5.gif, December 2004 [Accessed Jan. 18, 15.]

[9] Ernesto Limiti and Paolo Colantonio. *High Efficiency RF and Microwave Solid State Power Amplifiers*. New Jersey: Wiley, 2009, pp. 39.

[10] Millimeter-Wave Electronics Laboratory – ETH Zurich. "Typical InP HEMT Structure." Internet: http://www.mwe.ee.ethz.ch/education/research-and-thesis-projects/_jcr_content/par/accordion/accordionitem/par/fullwidthimage/image.imageformat.lightbox.793606967.png, [Accessed Nov. 18, 15.]

[11] Wikipedia. "Cross Section of a GaAs/AlGaAs/InGaAs pHEMT." Internet: https://upload.wikimedia.org/wikipedia/commons/thumb/9/92/HEMT-scheme-en.svg/350px-HEMT-scheme-en.svg.png, Aug. 2015 [Accessed Mar. 18, 15.]

[12] von Helmut Brech. "Optimization of GaAs based High Electron Mobility Transistors by Numerical Simulations." PhD Thesis, Technischen Universität Wien, Germany, 1998.

[13] Yaser A. Khalaf. (2000). Systematic Optimization Technique for MESFET Modeling. Available: http://scholar.lib.vt.edu/theses/available/etd-08042000-17470052/unrestricted/Dissertation.pdf. [Accessed 14 Dec 2014].

[14] Tayel, M.B.; Yassin, A.H., "Swarm intelligence - Based small signal parameters extraction for PHEMT," *National Radio Science Conference (NRSC)*, pp.1-8, 17-19 March 2009.

[15] Jarndal, A., "A simplified modelling approach for AlGaN/GaN HEMTs using pinched cold S-parameters," *5th International Conference on Modeling, Simulation and Applied Optimization (ICMSAO*), pp. 1-4, 28-30 April 2013.

[16] Jarndal, A., "Parasitic elements extraction of AlGaN/GaN HEMTs on SiC substrate using only pinch-off S-parameter measurements," *26th International Conference on Microelectronics (ICM)*, pp. 13-16, 14-17 Dec. 2014

[17] G. Kompa and M. Novotny, "Frequency-dependent measurement error analysis and refined FET model parameter extraction including bias-dependent series resistors," in *Int. IEEE Experimentally Based FET Device Modeling and Related Nonlinear Circuit Design Workshop*, Kassel, Germany, Jul. 1997, pp. 6.1–6.16.

[18] Jarndal, A.; Kompa, G., "A new small-signal modeling approach applied to GaN devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3440-3448, Nov. 2005.

[19] Jarndal, A.; Essaadali, R.; Kouki, A., "A Reliable Model Parameter Extraction Method Applied to AlGaN/GaN HEMTs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. PP, no. 99, pp. 1, Jul. 2015.

[20] Jarndal, A., "Combined genetic algorithm and neural network technique for transistor modeling," *International Conference on Communications, Signal Processing, and their Applications (ICCSPA)*, pp. 1-4, 17-19 Feb. 2015.

[21] Jarndal, A.H.; Alhammadi, O.A.; Al-Ali, R.H., "GaN power amplifiers design using genetic neural network model," *International Conference on Communications, Signal Processing, and their Applications (ICCSPA)*, pp. 1-6, 17-19 Feb. 2015.

[22] Jarndal, A.; Bunz, B.; Kompa, G., "Accurate Large-Signal Modeling of AlGaN-GaN HEMT Including Trapping and Self-Heating Induced Dispersion," *IEEE International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, pp. 1-4, 4-8 June 2006.

[23] Jarndal, A.; Essaadali, R.; Kouki, A., "A general and reliable model for GaN HEMTs on Si and SiC substrates," *IEEE 16th Annual Wireless and Microwave Technology Conference (WAMICON)*, pp. 1-5, 13-15 Apr 2015.

[24] Jarndal, A.; Kompa, G., "Large-Signal Model for AIGaN/GaN HEMT for Designing High Power Amplifiers of Next Generation Wireless Communication Systems," *IEEE International Conference on Signal Processing and Communications (ICSPC)*, pp. 77-80, 24-27 Nov. 2007.

[25] Root, D.E., "Future Device Modeling Trends," *IEEE Microwave Magazine*, vol. 13, no. 7, pp. 45-59, Nov.-Dec. 2012.

[26] Maxim Integrated. "RF Receiver." Internet: https://www.maximintegrated.com/en/images/appnotes/4647/4647Fig01.gif [Accessed Nov. 18, 15.]

[27] Baylis, Charles Passant. "Improved techniques for nonlinear electrothermal FET modeling and measurement validation." PhD Thesis, University of South Florida, United States, 2007.

[28] Liu Dan; Wang Liang; Chen Xiaojuan, "GaN HEMT large-signal model research," *International Workshop on Microwave and Millimeter Wave Circuits and System Technology (MMWCST)*, pp. 1-5, 19-20 April 2012.

[29] Angelov, I.; Andersson, K.; Schreurs, D.; Xiao, D.; Rorsman, N.; Desmaris, V.; Sudow, M.; Zirath, H., "Large-signal modelling and comparison of AlGaN/GaN HEMTs and SiC MESFETs," *Asia-Pacific Microwave Conference (APMC)*, pp. 279-282, 12-15 Dec. 2006.

[30] California Eastern Laboratories. "Converting GaAs FET Models for Different Nonlinear Simulators." Internet: http://www.cel.com/pdf/appnotes/an1023.pdf, Dec. 21, 2015 [Accessed 2 Nov. 2014.]

[31] Angelov, I.; Zirath, H.; Rosman, N., "A new empirical nonlinear model for HEMT and MESFET devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 12, pp. 2258-2266, Dec 1992.

[32] Hui Zhou; Yuehang Xu; Lin Feng, "An improved large-signal I–V model of GaN HEMT," *International Conference on Computational Problem-Solving (ICCP)*, pp. 284-286, 19-21 Oct. 2012.

[33] Lin-Sheng Liu; Fan He, "An improved large-signal model of GaN MISHEMT," *European Microwave Integrated Circuits Conference*, pp. 332-335, 10-11 Oct. 2011.

[34] Cabral, P.M.; Pedro, J.C.; Carvalho, N.B., "Nonlinear device model of microwave power GaN HEMTs for high power-amplifier design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 11, pp. 2585-2592, Nov. 2004.

[35] Yuk, K.S.; Branner, G.R.; McQuate, D.J., "A Wideband Multiharmonic Empirical Large-Signal Model for High-Power GaN HEMTs With Self-Heating and Charge-Trapping Effects," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3322-3332, Dec. 2009.

[36] Lin-Sheng Liu; Jian-Guo Ma; Geok-Ing Ng, "Electrothermal Large-Signal Model of III–V FETs Including Frequency Dispersion and Charge Conservation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3106-3117, Dec. 2009.

[37] Yuk, K.S.; Branner, G.R.; McQuate, D.J., "A Wideband Multiharmonic Empirical Large-Signal Model for High-Power GaN HEMTs With Self-Heating and Charge-Trapping Effects," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3322-3332, Dec. 2009.

[38] Cao, Quanjun, Yimen Zhang, Yuming Zhang, Hongliang Lv, Yuehu Wang, Xiaoyan Tang, and Hui Guo. "Improved Empirical DC I–V Model for 4H-SiC MESFETs." *Science in China Series F: Information Sciences*, vol. 51, no. 8, pp. 1184-192, 18 June 2008.

[39] Fager, C.; Pedro, J.C.; De Carvalho, N.B.; Zirath, H., "Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 12, pp. 2834-2842, Dec 2002.

[40] Cabral, P.M.; Pedro, J.C.; Carvalho, N.B., "Nonlinear device model of microwave power GaN HEMTs for high power-amplifier design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 11, pp. 2585-2592, Nov. 2004.

[41] Lin-Sheng Liu & Ji Luo, "Improved large-signal GaN HEMT model suitable for intermodulation distortion analysis", *International Journal of Electronics*, vol. 98, no. 12, pp. 1673-1685, 2011.

[42] Jarndal, A.; Pillai, S.; Abdulqader, H.; Kompa, G., "On the large-signal modeling of AlGaN/GaN devices using genetic neural networks," *7th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 60-63, 29-30 Oct. 2012.

[43] Shifan Guo; Yansong Li; Sheng Xiao, "Wind speed forecasting of genetic neural model based on rough set theory," *5th International Conference on Critical Infrastructure (CRIS)*, pp. 1-6, 20-22 Sept. 2010.

[44] Jarndal, A.; Pillai, S.; Abdulqader, H.; Ghannouchi, F.M., "A genetic neural network modeling of GaN HEMTs for RF power amplifiers design," *International Conference on Microelectronics (ICM)*, pp. 1-6, 19-22 Dec. 2011.

[45] Angelov, I.; Bengtsson, L.; Garcia, M., "Extensions of the Chalmers nonlinear HEMT and MESFET model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 10, pp. 1664-1674, Oct 1996.

[46] Jespers, P.G.A.; Murmann, B., "Calculation of MOSFET distortion using the transconductance-to-current ratio (gm/ID)," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 529-532, 24-27 May 2015.

[47] Marius Crisan. (2010, Mar 1). *Parameters Determination for Optimum Design by Evolutionary Algorithm*. [online]: http://www.intechopen.com/books/convergence-and-hybrid-information-technologies/parameters-determination-for-optimum-design-by-evolutionary-algorithm. [Accessed 2 Nov. 2014.]

[48] Carlos A Coello, Gary B Lamont. *Applications of Multi-Objective Evolutionary Algorithms*. Singapore: World Scientific Publishing Co. Pte. Ltf., 2004, pp. 1-6.

[49] Deb, K.; Pratap, A.; Agarwal, S.; Meyarivan, T., "A fast and elitist multiobjective genetic algorithm: NSGA-II," *IEEE Transactions on Evolutionary Computation*, vol. 6, no. 2, pp. 182-197, Apr 2002.

[50] Grebennikov, A.V.; Fujiang Lin, "An efficient CAD-oriented large-signal MOSFET model," *IEEE Transactions on Microwave Theory and Techniques,* vol. 48, no. 10, pp. 1732-1742, Oct. 2000.

[51] Avolio, G.; Raffo, A.; Angelov, I.; Crupi, G.; Caddemi, A.; Vannini, G.; Schreurs, D.M.M.-P., "Small-Versus Large-Signal Extraction of Charge Models of Microwave FETs," *IEEE Microwave and Wireless Components Letters,* vol. 24, no. 6, pp. 394-396, June 2014.

[52] Follmann, R.; Borkes, J.; Waldow, P.; Wolff, I., "Extraction and modeling methods for FET devices," *IEEE Microwave Magazine,* vol. 1, no. 3, pp. 49-55, Sep 2000.

[53] Jarndal, A.; Aflaki, P.; Ghannouchi, F.M., "Large-signal modeling of AlGaN/GaN HEMTs based on DC IV and S-parameter measurements," *IEEE International Conference on Semiconductor Electronics (ICSE),* pp. 34-37, 28-30 June 2010.

[54] Avago Technologies, "ATF 52189," Nov. 2013.

[55] Shinohara Keisuke, Matsui Toshiaki. "Nano-Gate Transistor World's Fastest InP-HEMT". *Journal of the National Institute of Information and Communication Technology*, vol. 51, pp. 96-102, 2004.

[56] ADCMT 6241A I-V Curve Tracer Software.

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