DYNAMIC POWER CHARACTERISTICS OF SELECTIVE

BURIED OXIDE (SELBOX) MOSFET

by

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Approval Signatures

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Dedication . . .

I dedicate this thesis to my parents, teachers, friends, and fellow members without whom it was almost impossible to complete my thesis work. Also, I would like to dedicate it to any person who can benefit out of this work to make the world a better place to live…

Abstract

The ever-increasing number of devices and electronic systems resulted in increasing the die size to satisfy the increasing demand. Moreover, the shrinking size of transistors according to the scaling theory became a contributor to increasing the leakage current. Many efforts have been made to reduce power dissipation by introducing new circuit designs and new device architectures, which is the main scope of this thesis, such as the Silicon-On-Insulator (SOI) and the Selective Buried Oxide (SELBOX) structures. The bulk Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) structure has relatively high power dissipation, in addition to its poor frequency response due to its internal capacitances. As a result, SOI MOSFET has been introduced as an alternative to the bulk MOSFET to minimize power dissipation as well as to tackle the existing problems of the bulk MOSFET. The SOI MOSFET transistor active region is isolated from the substrate and hence device parasitic capacitances are reduced resulting in a faster operation and lower leakage power dissipation. Unfortunately, results showed that the fully-depleted SOI (FD-SOI) and partially-depleted SOI (PD-SOI) suffer from self-heating effect and the PD-SOI has the kink effect problem. Therefore, the concerns towards fabricating a new device that combines the advantages of the bulk and SOI MOSFETs and eliminating their drawbacks have been raised again. The proposed device is called the SELBOX MOSFET and has structural features identical to SOI MOSFET structure with the only difference which is the gap in the isolation layer. Our results showed that the existing gap in the BOX layer has eliminated the self-heating and the kink effects which are the major drawbacks of the SOI MOSFET. The main objective of this thesis is to investigate the dynamic power dissipation of the CMOS SELBOX structure and compare it with that of the CMOS bulk and SOI structures. The devices' fabrication simulation have been conducted using Silvaco TCAD tools. The simulation results show that the dynamic power dissipation of the CMOS bulk, SOI and SELBOX are almost the same at high frequencies. However, at low frequencies, the dynamic power dissipation of the CMOS bulk is the highest and that of CMOS SOI and SELBOX is very close.

Search terms: **dynamic power dissipation, CMOS, SELBOX, bulk, SOI, kink effect.**

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List of Abbreviations

MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
SELBOX	Selective Buried Oxide MOSFET
CMOS	Complementary Metal Oxide Semiconductor
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
SOI	Silicon On Insulator
PD SOI	Partially Depleted Silicon On Insulator
FD SOI	Fully Depleted Silicon On Insulator
BOX	Buried Oxide
MTCMOS	Multi-threshold CMOS
C_L	Load Capacitance
BP	Bin Packing
SP	Set Partitioning
IC	Integrated Circuit
D-MOSET	Double-diffused MOSFET
DG-MOSFET	Double-gate MOSFET
FinFET	Fin Field-effect-transistor

Chapter 1: Introduction

Minimum power consumption has become one of the major requirements for most microelectronic systems. As systems' features and operations increase, power consumption and system complexity increase. For instance, in modern communication systems, such as cell-phones, many operations take place in one chip including video streaming, file transfer, email exchange and Wi-Fi connection. All of these operations increase the device power dissipation and decrease its efficiency as they decrease the device lifetime. As such, the effort towards designing low power devices and systems has become flourishing recently.

Power dissipation has assumed greater importance after the advent of portable–battery driven devices such as laptops and cell-phones. Increasing the device power dissipation results in increasing its temperature invariably. This rise in temperature alters the device characteristics and hence its operation. As temperature increases, leakage current increases, which is carried by minority carriers, and hence temperature further increases. This might result in device breaking down unless heat dissipation is removed on time. This happens when the device is OFF. However, when the device is ON, the rise in temperature causes the device thermal voltage V_T to change and carrier mobility (μ) to decrease. Consequently, the device drain current (I_D) changes altering the device performance.

Several approaches have been published in the literature to reduce static and dynamic power dissipation. Some of these approaches aim to reduce power dissipation by targeting device architecture, which is the main scope of this work, and others focused on circuit design. Starting with static power dissipation, Anis et. al [1] suggested the multi- threshold CMOS (MTCMOS) to reduce static power dissipation by using dual threshold voltages. A low threshold voltage for gate transistors that are in a critical path and high threshold voltage for gate transistors those are in a non-critical path. This is due to the fact that subthreshold conduction, which is one of the main causes of static power dissipation, decreases as the threshold voltage increases [1]. However, this technique suffers from latency and complex fabrication.

Targeting static power consumption in logic circuits, [2] presents the Gated-V_{DD} and Gated-GND or the sleep approach. This technique adds sleep transistors between

the supply voltage (V_{DD}) and ground; a PMOS transistor between the V_{DD} and the pull-up network and an NMOS transistor between the pull-down network and the ground. The sleep transistors turn off the circuit when it is inactive by switching off the power supply and turns it ON when the circuit is active. Adding the sleep transistors will not affect the circuit performance as they provide low resistance in the conduction path [2]. Another technique for logic circuit suggested by [2] is the stack effect method. This method reduces subthreshold leakage using reverse body biasing to increase threshold voltage and by breaking down a transistor into two transistors and forcing them to be simultaneously OFF. Nevertheless, this method causes latency between the breaking down transistors.

Moving towards the device architecture, [3] has suggested reducing the static power dissipation by reducing the flicker noise. It drives the MOS from strong inversion to accumulation in order to apply switch biasing to the circuit. The flicker noise is reduced by turning off the bias current when the device is not active and hence static power dissipation is reduced.

However, the main scope of this work is the dynamic power consumption which will be studied thoroughly in the following sections.

1.1. Problem Definition

Dynamic power dissipation has assumed a great importance after the revolution of transistor scaling. As technology scales down, the channel length decreases resulting in lower threshold voltage and hence lower supply voltage is required. As such, satisfying the concerns towards designing reliable circuits with less packaging costs is achieved. On the other hand, down-scaling the channel length opens the door to other power dissipation problems which are also affecting circuits' efficiency. A closer look at the current state of art technology, as depicted in Figure 1, reveals the ever-increasing dynamic power consumption as technology nodes scale down. It is worth mentioning that the static power dissipation increases in modern technologies more than the dynamic power dissipation as indicated in Figure 1, However, this does not unweight the importance of studying the dynamic power dissipation in CMOS devices.
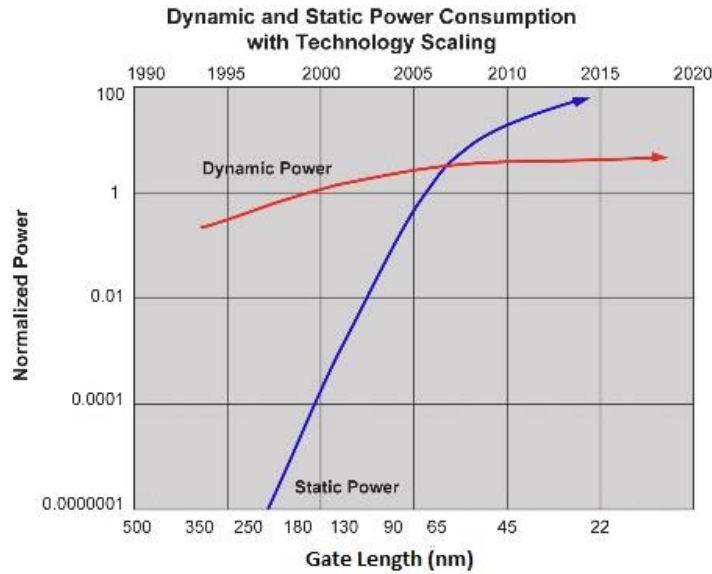
Figure 1: Increasing power dissipation at shrinking power nodes [4]

Dynamic power dissipation has two main sources; the charging and discharging of the load capacitance (C_L) and the short circuit effect when both NMOS and PMOS transistors are in saturation. Starting with the charging and discharging of C_L, a good example is to look at is the CMOS inverter circuit. When the input is 0 V, the PMOS transistor will be ON while the NMOS will be OFF. A current will be flowing through the PMOS charging the C_L by drawing current from the power supply. However, when the input is 1 V, C_L is discharged through the NMOS transistor.

A period of time when the input is transiting from 0 to 1 V or from 1 to 0 V, both NMOS and PMOS transistors will be ON, causing dynamic power dissipation as the current finds a direct path from the voltage supply to the ground, causing what is called short circuit. A more detailed discussion of both sources is presented in Chapter 2.

Efforts have been made to reduce dynamic power dissipation in order to be able to fabricate devices and design circuits with high reliability, efficiency and power performance. These efforts are applied on either circuit or device structure levels. However, the main interest of this work is on the device structure. Innocenti et. al [5] have suggested decreasing the dynamic power dissipation, caused by short circuit effect, by decreasing the transistor width. This technique was able to decrease the dynamic power dissipation by 20% by decreasing the transistor width by 45% for both NMOS and PMOS when the average gate capacitances are greater than the wires associated

capacitances per unit length. Furthermore, dynamic power consumption is reduced by 20% by reducing the voltage supply. However, this technique increases the static power dissipation as decreasing the supply voltage is associated with decreasing the threshold voltage in order to maintain the circuit performance resulting in increasing static power dissipation.

There is a trade-off between the supply voltage and threshold voltage. This is due to the fact that decreasing supply voltage is associated with decreasing threshold voltage resulting in decreasing the dynamic power dissipation and increasing subthreshold leakage current which is a form of static power dissipation. An optimization technique published in [6] has proposed to reduce both dynamic and static power dissipations by optimizing the supply voltage and the threshold voltage. The paper studied the temperature and process variations and all parameters that can be affected by temperature variation such as the mobility in order to find a new model for the drain current. Two equations have been derived that give the optimal supply voltage and the optimal threshold voltage.

Targeting the device structure level, Bikshalu et al. [7] have investigated dynamic power dissipation reduction by replacing the SiO2 oxide layer with high K layer for 45 nm, 32 nm and 22 nm technologies. Simulation results showed that dynamic power dissipation with high K layer is lower than the SiO2 layer for NMOS, PMOS and CMOS and the lowest dynamic power dissipation was recorded for 45 nm technology for PMOS and 32 nm for NMOS.

Another technique was published by Anis et al. [1] is by positioning one sleep transistor for a cluster of gate transistors. This sleep transistor will turn OFF the cluster transistors when they are not active by turning OFF the power rails and turning them ON when they are active. This technique is divided into two sub-techniques; the bin-packing (BP) technique and the set-partitioning technique. The (BP) technique performs linear algorithm in order to minimize number of sleep transistor for all N available transistors in the circuit. The BP technique has shown 17% reduction in dynamic power dissipation. However, the set-partitioning technique (SP) finds a cost function that minimizes the distance between the sleep transistor of choice which is responsible for a cluster of transistors. This technique has shown a reduction in dynamic power dissipation by 11%.

1.2. Thesis Methodology and Outline

The bulk transistor shown in Figure 2, has some limitations associated with relatively high power dissipation, short channel effects and low speed due to the effect of the device internal capacitance. As a result, different techniques have been suggested targeting the device structure such as fabricating new fully-depleted Silicon-on-Insulator (FD-SOI) MOSFET. This device has the advantage of an inserted isolation layer as depicted in Figure 3, which can be made from silicon dioxide (SiO2), in the silicon substrate which isolates the transistor active region from the substrate. As a result, the bulk capacitances will be reduced; bulk - source/drain/gate parasitic capacitances. The reduction in the parasitic capacitances results in high operation speed. Also, SOI devices have vertical isolation which eliminates the leakage current. Also, the isolation from substrate and from adjacent devices in CMOS SOI eliminates the latch-up issues, which cause shorting of the V_{DD} and GND lines and possibility of chip destruction, and provides high device integration. However, the FD SOI MOSFET suffers from the self-heating and kink effect drawbacks which cannot be ignored. The self-heating effect occurs in fully–depleted (FD) and partially-depleted SOI. However, the kink effect only occurs in PD SOI MOSFET devices. The kink effect happens because of the high electric field near the drain when the drain voltage is high. As such the body potential increases and the threshold voltage drops causing a sharp increase in the drain current and hence device non-linearity.

Consequently, the need for fabricating a new device that combines the advantages of the bulk transistor and the SOI MOSFET and at the same time tackles their problems, has become a necessity. This new device is the Selective-Buried Oxide (SELBOX) MOSFET which has been introduced by inserting a gap in the buried oxide isolation layer in order to reduce the body potential and hence the kink effect. The SELBOX MOSFET structure is presented in Figure 4. SELBOX MOSFET is found to have better frequency characteristics, reduced short-channel effects, and higher speed of operation due to the lower internal capacitances. Moreover, SELBOX MOSFET reduces self-heating effect [8]. Also, due to the gap existence, thermal connection will be reduced as the gap serves as a parallel low resistance and hence the overall resistance will be reduced. In addition, the gap helps to reduce the kink effect by absorbing the

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holes generated by the electric field and hence SELBOX MOSFET will have a lower body potential than SOI MOSFET [8].

As the SELBOX structure reduces the overall device capacitance, we hypothesize that using the SELBOX structure will reduce the dynamic power dissipation.
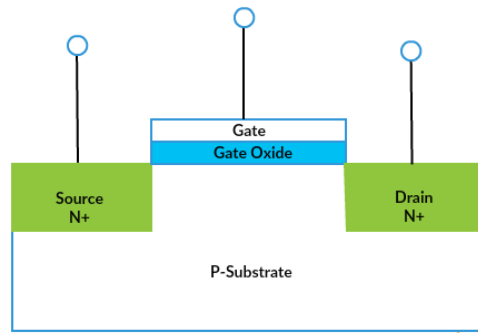
Figure 2: Bulk NMOS structure
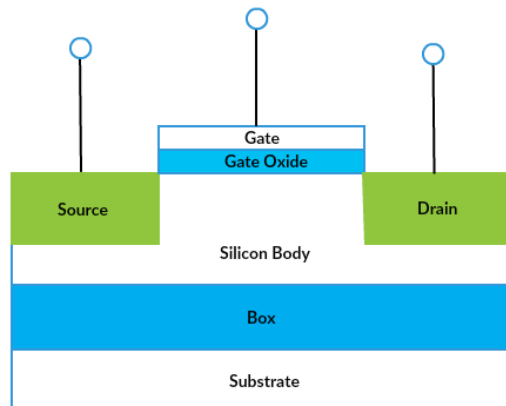
Figure 3: SOI MOSFET structure
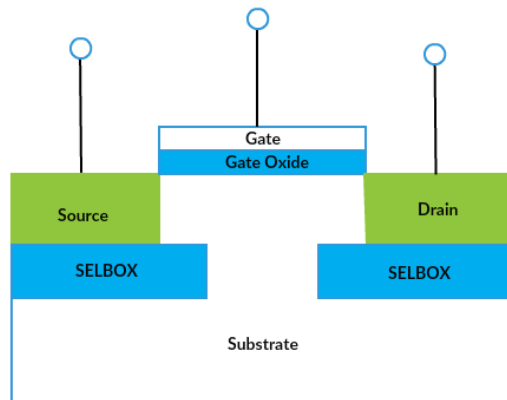
Figure 4: SELBOX MOSFET structure

1.3. Thesis Objectives

The objectives of the thesis are as follows:

- Fabricate 90 nm single devices; NMOS and PMOS, for the bulk, SOI and SELBOX structures on Silvaco TCAD tools.
- Analyze the fabricated NMOS and PMOS devices I-V characteristics.
- Fabricate 90 nm CMOS device for the bulk, SOI and SELBOX structures on Silvaco TCAD tools.
- Investigate the dynamic power dissipation of CMOS SELBOX structure.
- Compare the dynamic power dissipation of CMOS SELBOX structure with that of SOI and bulk structures.

1.4. Thesis Organization

This thesis is organized as the following; Chapter 2 discusses the basics of bulk MOSFET; its structure, MOSFET operation and channel formation, the body effect, subthreshold condition and the device internal capacitances. It introduces the SOI MOSFET, SELBOX MOSFET and other MOSFET structures.

Chapter 3 presents several techniques that have been presented in the literature in reducing both static and dynamic power dissipations. The advantages and disadvantages of these techniques will be briefly mentioned in this chapter.

Chapter 4 presents the dynamic power dissipation in CMOS devices in details and shows how the average dynamic power dissipation is found from calculations and simulation.

Chapter 5 shows simulation of single device fabrication; NMOS and PMOS, introduces the device parameters which are related to standard parameters presented in the literature. Moreover, it presents the current-voltage characteristics simulation results of single devices; NMOS and PMOS covering the bulk, SOI and SELBOX MOSFET structures.

Chapter 6 presents the fabrication simulation of CMOS BULK, SOI and SELBOX devices and their dynamic power dissipation simulation results. The simulation work which is carried out in this chapter is done for the sake of studying the

effect of changing the operating frequency and the load capacitance on the dynamic power dissipation on the three structures.

Chapter 7 discusses the results which are obtained in Chapter 6 and presents the conclusion.

Chapter 2: MOSFET Devices

MOSFET has become the backbone of many electronic circuits and devices which are used in wide range of industrial, medical and electrical applications. Downscaling the MOSFET technology as depicted in Figure 5 following Moore's law, the cost per die has decreased significantly [9] which made MOSFET technology extremely favorable. MOSFET is used in digital circuits such as microprocessors and memory devices. It provides the basic switching which is required for logic gates implementation. Also, MOSFET is used in discrete circuits for applications such as power frequency drivers and switch mode power supplies. Moreover, MOSFET devices are used in power amplifiers and automobile sound systems.
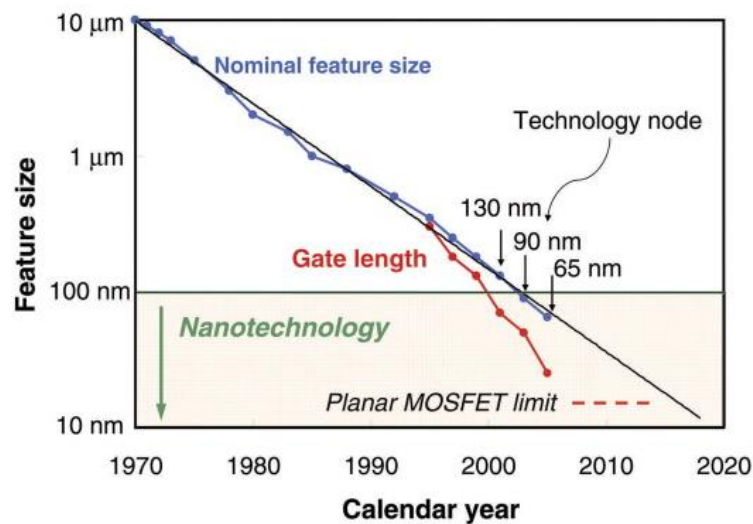
Figure 5: Gate length vs. calendar year [9]

The following sections describe the basics of MOSFET including structure and channel formation, body effect, subthreshold leakage, channel length modulation and internal capacitance.

2.1. Bulk MOSFET Structure

The n-channel MOSFET or NMOS is made up from a p type substrate which is a single crystal Silicon and two heavily doped terminals n^+ which are the source and the drain grown on the substrate as shown in Figure 2. A thin layer of silicon fills the region between the source and the drain, which forms the channel where carriers; electrons, move from source to drain. A silicon dioxide (S_iO_2) layer is formed on top of the substrate to cover the region between the source and the drain (channel). A metal is

deposited on top of the oxide layer forming the gate terminal and metal contacts are also formed on the top of the drain, source and substrate, also known as body. The thickness of the oxide layer below the gate limits the carriers to leak from the gate terminal to the substrate. As such, the MOSFET has four terminals; gate, source, drain and body. The source and the substrate junction and the drain and substrate junction can both form pn diodes which are always kept in reverse bias. The two pn junctions can be in cut-off mode by connecting the body terminal to the source terminal. When the channel is created between the source and the drain terminals, current can flow from the drain to the source in the channel which has length L and width W which are two important parameters in the MOSFET [10]. In case of p-channel MOSFET, the device is fabricated on n-substrate and the drain and the source are p+ heavily doped regions. Also, the carriers which form the channel are the holes and thus current flows from source to drain.

The typical values of the MOSFET device parameters differ based on the channel length. For instance, the oxide layer thickness is around 15 nm for 0.8 μm channel length. However, for a channel length of 65 nm, the oxide layer thickness is around 1.4 nm. Similar to the oxide capacitance; it is 2.3 fF/μm^2 when the channel length is 0.8 μm and increases to 23 fF/μm^2 when the channel length is 65 nm [11]. It is worth mentioning that CMOS is formed by combining both NMOS and PMOS.

There are other MOSFET structures than the typical bulk MOSFET, such as the Double-diffused MOSFET (D-MOSFET) and the Double-gate MOSFET (DG-MOSFET). The D-MOSFET is a power MOSFET that its channel length can be reduced to sub-micron by controlling the diffusion of the n$^+$and P-base regions. It is used for power applications where high operating frequencies are needed. The main advantages of the D-MOSFET are the fast switching speed and structure ruggedness [12]. The main idea of DG-MOSFET is to control the channel length by making it very small and adding contacts to both sides of the gate. The structure of the DG-MOSFET helps in eliminating the short channel effects.

2.1.1   MOSFET operation and channel formation. When zero voltage is applied to the gate, the MOSFET acts like back to back two series diodes, one forms a pn junction between the n$^+$ source and the p substrate and the other pn junction between the p substrate and the n$^+$ drain. The revere biased pn junctions will form depletion

regions, preventing any conduction current when a voltage between drain and source V_{DS} is applied [10]. When the source and drain are grounded, and a positive voltage is applied to the gate, the free holes will be repelled from the p substrate which is the region under the gate. The repelled holes will leave behind negatively charged ions. Talking about NMOS, the electrons in the drain and source regions will be attracted to the p substrate under the gate creating an n-channel between the source and the drain. As such, the p substrate is inverted to an n type region or n-channel or an inversion layer. The gate and the induced channel form a parallel plate capacitor and the oxide acts as the capacitor dielectric. A positive charge accumulates in the gate on top of the oxide layer and a negative charge accumulates in the induced channel forming an electric field. This field controls the charge and the current from source to drain. When $\mathbf{V_{DS}}$ is zero, the voltage along the channel is zero, and V_{GS} which is between the gate and the channel is uniform. However, when V_{GS} exceeds the threshold voltage V_{th}, a channel will be formed. The difference between V_{GS} and V_{th} is called the overdrive voltage V_{ov} [10].

$$V_{ov} = V_{GS} - V_{th} \tag{1}$$

The charge across the channel is expressed as [10]:

$$Q = C_{ox}WL\,V_{ov} \tag{2}$$

where C_{ox} is the oxide capacitance per unit area, W and L are the channel width and length, respectively. There are three modes of operation in which a MOSFET can operate in: the cut-off, triode and saturation. In cut-off and triode regions, the MOSFET can be used as a switch and if the MOSFET is used as an amplifier, it has to operate in the saturation region [10].

2.1.2. Applying small v_{DS}. Applying small v_{DS} as seen in Figure 6 will allow current to flow in the induced channel, so negative charges will flow from source to drain and hence a drain current will flow from drain to source. In this case, the MOSFET behaves as a linear resistor as the applied voltage is small. The resistance r_{DS} can be calculated as follows [10]:

$$r_{DS} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{th)}} \tag{3}$$

where μ_n is the electrons' mobility.

Increasing v_{GS} above V_{th} will enhance the channel where the name enhancement mode operation or enhanced MOSFET comes from. As v_{GS} increases further, the voltage between the gate and all points along the channel decreases and hence the channel is deepest at the source end and shallowest at the drain end. As long as V_{DS} is below V_{ov} and v_{GD} is below V_{th}, the channel depth at the drain side is nonzero. Thus, the MOSFET is operating in the triode region. As v_{DS} increases, the channel resistance increases and hence the drain current i_D vs. v_{DS} curve starts to bend. The drain current can be modeled by the following equation [10]:

$$i_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left((v_{GS} - V_{th})v_{DS} - \frac{1}{2}v_{DS}^2\right) \qquad (4)$$

In case of PMOS, the induced channel is obtained when a negative voltage is applied between the gate and source (v_{GS}) and by decreasing this negative voltage below V_{th} [10],

$$|v_{GS}| \geq V_{th} \qquad (5)$$
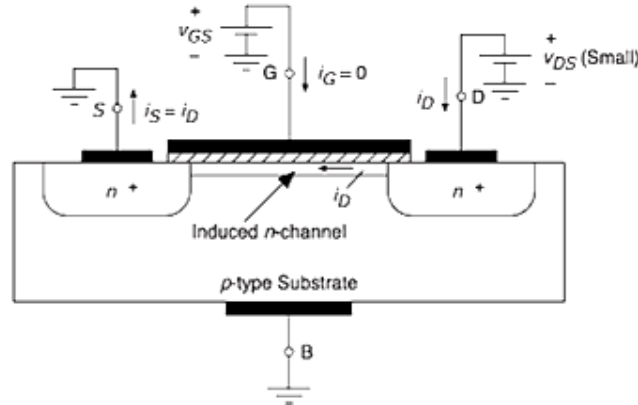
Figure 6: Applying a small $\mathbf{v_{DS}}$ [13]

2.1.3. Increasing v_{DS} above V_{ov}. When v_{DS} is greater than V_{ov} and v_{GD} is greater than V_{th}, the channel depth at the drain side reduces to zero and hence the MOSFET enters the saturation mode of operation. In this case, the channel is pinched off close to the drain side. The channel resistance becomes greater which limits the drain current and hence the current stops increasing and becomes saturated. The transition from the triode region to the saturation region happens when v_{DS} is equal to V_{ov}, and in this case v_{DS} is called v_{DSsat} [10],

$$v_{DSsat} = v_{GS} - V_{th} \tag{6}$$

The relationship between the i_D and v_{DS} is expressed as the following [10]:

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{th})^2 \tag{7}$$

2.1.4. MOSFET body effect. Considering NMOS physical structure, two pn diodes are formed between source/bulk and between the drain/bulk. These two pn junctions have to be reverse biased in order to prevent any leakage of carries from drain/source to the bulk or to the substrate. As such, the bulk voltage should be higher than the source voltage. As the drain voltage is always greater than the source voltage, the body effect can be noticed in the source/bulk pn diode not the bulk/drain np diode. In case the source voltage is greater than the bulk voltage, the depletion region will be wider which limits the channel width and thus a higher v_{GS} is needed to maintain the same threshold voltage. The body effect results in variation in the threshold voltage which is expressed in the following relationship [14]:

$$V_{th,n} = V_{th,n0} + \gamma\sqrt{2\emptyset_f + V_{SB}} - \sqrt{2\emptyset_f} \tag{8}$$

where $V_{th,n0}$ is the threshold voltage when $V_{SB} = 0$, $\emptyset_f$ is a physical parameter, and γ is called body-effect parameter.

2.1.5. Subthreshold leakage. As technology scales down, subthreshold leakage current increases exponentially and becomes a dominant factor of total power dissipation in MOSFET devices. It is the drain current when the device is supposedly OFF and the applied voltage v_{GS} is less than the threshold voltage V_{th}. As technology scales down, supply voltage and threshold voltage decarese to maintain the circuit performance which results in an exponential increase in the subthreshold leakage current [15]. In weak inversion regime (subthreshold regime), the drain current is basically a diffusion current which is carried by diffusion of carriers from source to drain. As such, the subthreshold current is dominated by diffusion current and has an exponential relationship with the gate-source and the threshold voltages. The following equation (9) shows the relationship between subthreshold leakage current with other device parameters [16].

$$I_{sub} = \alpha \left(\frac{1}{L_{eff}}\right) e^{\frac{q(V_G - V_{th})}{kT}} \tag{9}$$

where $\frac{kT}{q}$ is the thermal voltage, L_{eff} is the channel effective length and V_G is the gate voltage. From the above equation, it can be noticed that the subthreshold leakage current increases exponentially with increasing the difference between V_G and V_{th}. Also, the leakage current increases exponentially with decreasing the thermal voltage $\frac{kT}{q}$ and increases linearly with decreasing the channel effective length L_{eff}. However, limi increasing the subthreshold leakage current becames challenging with controlling all of the above parameters and technology down scaling. As such, this led to the introduction of Silicon-on-Insulator MOSFET (SOI MOSFET) to tackle several problems including the subthreshold leakage current.

As aforementioned, as v_{DS} increases and becomes greater than the override voltage V_{ov}, the device becomes operating in the saturation region and the channel close to the drain terminal is pinched-off as seen in Figure 7. The pinch-off occurs when the potential difference between the gate and any point along the channel equals to V_{th}, as such [10]:

$$v_{Gx} = V_{th} \tag{10}$$

$$v_G - v_x = V_{th} \tag{11}$$

where x is any point along the pinched off side of the channel. The voltage at any point along the channel, when pinch-off occurs, equals to the following:

$$v_x = v_G - V_{th} \tag{12}$$

Precisely, pinch-off occurs when

$$v_{DS} \geq v_{GS} - V_{th} \tag{13}$$

A voltage drop occurs between the pinch point x and the drain is a depletion region. As a result, the channel length is reduced by ΔL because of the pinch-off. As v_{DS} increases beyond V_{ov}, ΔL increases and hence it is said that the channel length is modulated by v_{DS}. Channel length modulation affects the drain current i_D as it affects

the channel length L and replaces it with $L - \Delta L$ as seen in the following relationship [10]:

$$i_D = \frac{1}{2}\mu C_{ox}(v_{GS} - V_{th})^2(1 + \lambda v_{DS}) \tag{14}$$

where λ is the channel length modulation.
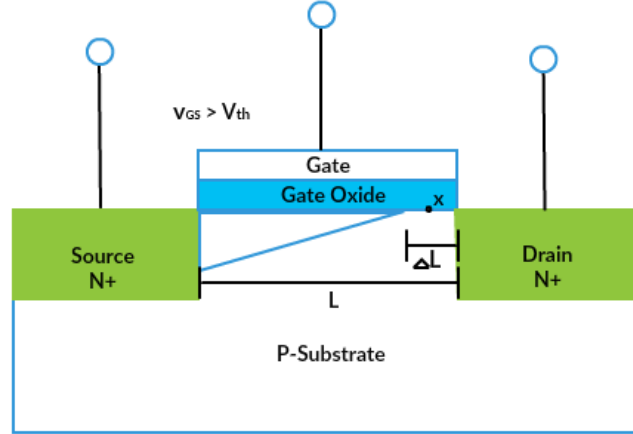
Figure 7: Channel length modulation

2.1.6.   MOSFET device capacitances. In order to predict the MOSFET device dynamic behavior, the device capacitances should be taken into account. These capacitances are called parasitic capacitances and these capacitances affect the device performance adversely. The internal capacitances are divided into two categories, the gate and the junction capacitances. As for the gate capacitance, the gate forms a parallel plate together with the channel and the oxide layer forms the dielectric layer. As aforementioned, an oxide layer covers the region between the drain/gate and between the source/gate. As a result, a gate-source C_{GS} and gate-drain C_{GD} capacitances are formed. As for the second category, a drain-bulk and source-bulk capacitances are formed. C_{SB} is formed because of the reverse bias pn diode between the n-source and the p-bulk. However, C_{DB} is formed as a result of the reverse bias pn diode between the n-drain and the p-bulk. It is worth mentioning that these capacitances limit the device frequency response and its speed. The NMOS device capacitances are shown in Figure 8. These capacitances are dependent on device dimensions and bias conditions.

To examine the device internal capacitances impact on the dynamic power dissipation, by the reference to the dynamic power dissipation equation [10];

$$P_{dynamic} = C_L V_{DD}^2 \, f_{ck} \alpha \qquad\qquad (15)$$

where f_{ck} is the clock frequency, V_{DD} is the supply voltage and α is the activity factor which is the probability of the output to switch from 0 to 1. As the used signal in this thesis work is a clock (pulse) signal, α is equal to 1 [17]. C_L includes the internal capacitances of the NMOS and PMOS in the CMOS inverter and the internal capacitances of the NMOS and PMOS of the load assuming the CMOS inverter is driving another CMOS inverter as a load as depicted in equation (16) [18]:

$$C_L = C_{GD1} + C_{GD2} + C_{DB1} + C_{DB2} + C_{G3} + C_{G4} + C_W \qquad (16)$$

where C_{GD1} and C_{GD2} are the gate to drain capacitance of the NMOS and PMOS of the CMOS inverter respectively. C_{DB1} and C_{DB2} are the drain to bulk capacitance of the NMOS and PMOS in the CMOS inverter respectively. C_{G3} and C_{G4} are the gate capacitance of the NMOS and PMOS of the CMOS inverter load. C_W is the wiring capacitance.

As it can be concluded from the dynamic power equation, reducing the device internal capacitance can effectively reduce the dynamic power dissipation. More details on power dissipation are provided in the Chapter 4.
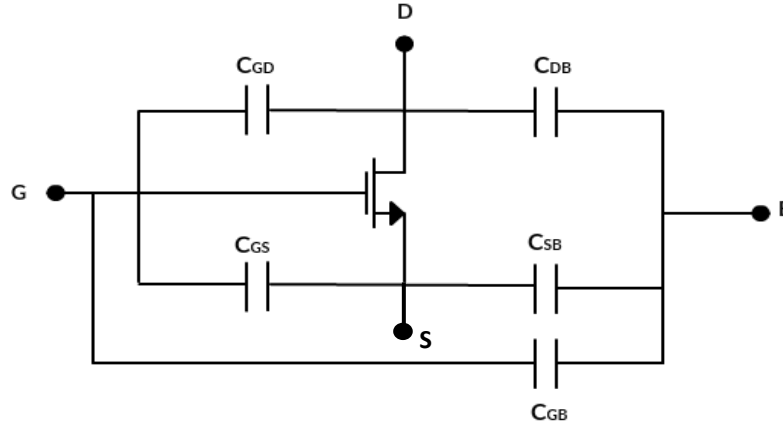
Figure 8: NMOS device capacitances

2.2.   Silicon-on-Insulator (SOI) MOSFET

As a solution to the poor frequency response, low speed operation as well as to reduce the total power dissipation in bulk MOSFET devices, SOI MOSFET was introduced. SOI MOSFETs use silicon-insulator-silicon layer substrate instead of the silicon substrate used in conventional transistors. An insulation layer; which is a silicon

oxide layer and it is referred as Buried Oxide (BOX), is inserted between two silicon layers to isolate the active transistor from the wafer substrate as illustrated in Figure 3 in Chapter 1. The structure of SOI MOSFET device reduces the effect of parasitic capacitors. Due to the presence of isolation layer between the bulk and the device active region, parasitic capacitances which are formed between the bulk and the source/drain/gate; C_{sb}, C_{db}, and C_{gb}, are reduced and hence improve the device performance. Also, SOI MOSFET devices provide lower leakage currents due to isolation thus higher power efficiency. Since the electrical area is reduced to the active region around the transistor, the switching speeds increase [19].

Transistors made on SOI wafer, are isolated from each other by lateral trench isolation with silicon dioxide which eliminates latch-up problems and results into smaller chip area, higher production yield and increasing fab productivity. On bulk transistor, the transistors are formed on n-well. However, on the SOI, the transistors are formed on Silicon layer insulated by thin BOX layer. This results in reduced chip area and hence more transistors can be formed per die.

There are two types of SOI transistors which are categorized depending on the thickness of the Silicon layer. The first type is the partially depleted PD SOI transistor in which the Si above the silicon dioxide layer is thicker (100-200 nm) than twice the width of the depletion region. The applied gate voltage will not deplete the active Silicon. As the channel width shrinks, the Si layer becomes thinner, as for fully depleted SOI transistor (50-10 nm). The active silicon is thin enough to allow the applied gate voltage to deplete it completely [19].

One more advantage of the SOI MOSFET over the bulk MOSFET is the elimination of latch-up current. It is a form of short circuit in which a low impedance path is created between power supply and ground. This condition occurs when a trigger occurs; a high voltage or a high current. However, this low impedance path remains even after the trigger no longer exists and hence may cause device damage due to the overcurrent. SOI Silicon insulation layer is deposited on the silicon substrate and hence eliminates the parasitic that lead to latch up [20].

However, PD SOI devices suffer from kink effect. Kink effect causes nonlinearity in the device due to the rapid increase in the drain current as a result of the

reduced threshold voltage. A proposed solution to the kink effect, is the introduction of the Selective Buried Oxide MOSFET (SELBOX MOSFET). Due to the structure of the SELBOX MOSFET as seen in Figure 4, the gap resistance decreases as the gap length increases. As such, as gap length increases, kink effect disappears [20]. The presence of the gap in the substrate reduces the gate to bulk capacitance C_{gd} to 0.8 fF compared to 2.5 fF in bulk MOSFET [21].

In conclusion, basics of MOSFET and its structures have been illustrated thoroughly. In order to validate the novelty of our proposed techniques in reducing the CMOS dynamic power dissipation, the efforts that have been made to reduce dynamic and static power dissipation will be presented in the following chapter. It is worth mentioning that this thesis work is focusing on investigating the dynamic power dissipation in CMOS SELBOX and compare it with that of CMOS bulk and SOI. As mentioned earlier, since the SELBOX structure reduces the overall device capacitance, our hypothesis is that SELBOX structure will reduce the dynamic power dissipation.

Chapter 3: Literature Review

3.1. Introduction

The silicon integrated circuits industry has been flourishing during the past years due to the downscaling of the MOS technology. Scaling down the technology is not only associated with shrinking the device dimensions, but also with reducing the gate threshold voltage and hence the operating voltage. Channel length of 65, 28 and even 14 nm are now available. Scaling down the CMOS technology has led to an obvious improvement in the transistor performance by reducing the gate delay by around 30% [22]. Also, it increases the transistor density by doubling it. The more the integrated circuit (IC) is scaled down, the more circuit/system packaging becomes easier and thus the less packaging cost will be.

However, the decreased die size and the increased number of transistors lead to increasing the power dissipation rapidly. The channel length and oxide thickness downscaling have resulted in increasing the leakage current and hence the leakage power, which is one form of static power dissipation. This current is caused by leaking carries between the gate oxide and the substrate. Scaling down the MOS technology from 65 nm and downwards resulted in obvious increase in both dynamic and static power dissipation. Figure 9 shows that leakage current became a significant contributor to power dissipation in CMOS technology [23].
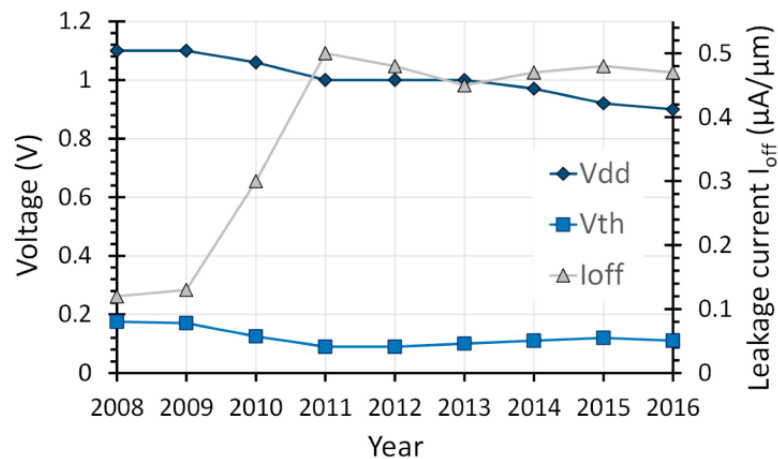
Figure 9: Behavior of MOSFET threshold voltage, supply voltage and transistor OFF state leakage current [24]

As technology scales down, lower supply voltage is required which results in decreasing the threshold voltage and leakage power dissipation became dominant which is evident in Figure 9. Consequently, increasing the power dissipation in circuits is considered a critical issue as it shortens the battery life. However, long battery life is a significant constraint in most power systems especially in medical and mobile applications [24].

3.2. Sources of Power Dissipation

Sources of power dissipation in MOS devices involve both static and dynamic powers. Starting with static power dissipation, there are three main sources of static power which are more dominant than dynamic power sources below. Static power sources include the subthreshold conduction when the transistor is in OFF state [25], which is also called the zero gate drain current [25], the tunneling current through gate oxide, which increases as the gate oxide thickness decreases, and the reverse bias current. The static current is dominated by the threshold leakage when the CMOS is in weak inversion. On the other hand, the static current becomes dominated by the reverse bias current when the transistor channel length scales down, more precisely below 45 nm [5].

As for the dynamic power dissipation, it is mainly caused by charging and discharging of C_L. By looking into the CMOS inverter circuit shown in Figure 10, during the transition from low to high state, C_L is charged by drawing current from the supply. A portion of the drawn current is stored in C_L and a portion is dissipated in the PMOS device. However, during the transition from high to low state, C_L is discharged and the discharged energy is dissipated in NMOS transistor. The dynamic power dissipation due to switching is computed using equation (15). It is worth mentioning that the dynamic switching power dissipation used to be the dominant factor of power dissipation in CMOS digital devices down to 180 nm technology for the bulk structure [25]. However, the dynamic power dissipation in SOI and SELBOX is still questionable.

Another source of dynamic power dissipation is the short circuit power dissipation. Again by looking into the CMOS inverter circuit, during the transition from ON to OFF state or from OFF to ON state, there will be a period of time where both PMOS and NMOS transistors are conducting and the current will find a direct path

between V_{DD} and ground, hence resulting in short circuit current [25], [5]. Short-circuit power dissipation increases with rise and fall time of the transistors. The short circuit power dissipation can be calculated using the following equation [25]:

$$P_{short-circuit} = K(V_{DD} - 2V_{th})^3 \tau f \tag{17}$$

where V_{DD} is the supply voltage, V_{th} is the subthreshold voltage, τ is the fall or rise time of the input signal and f is the clock frequency and K is a factor that depends on the transistor dimensions. Up to 90 nm CMOS technology, the dynamic power dissipation is dominated by the C_L charging and discharging current [5].
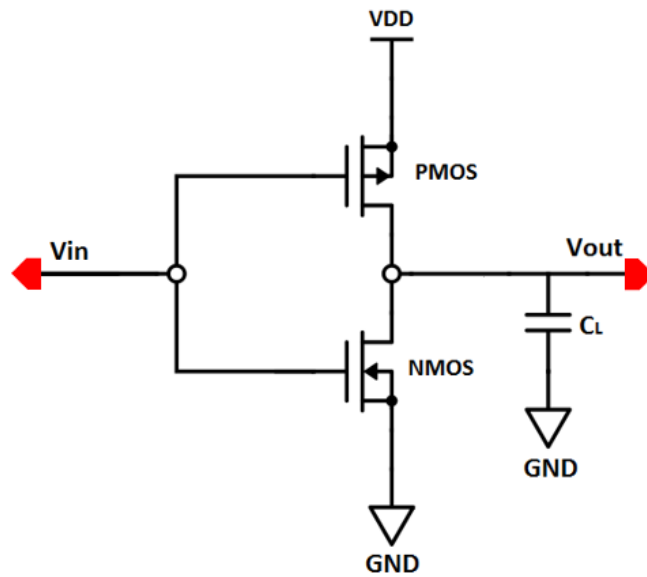
Figure 10: Dynamic switching power in CMOS inverter

Literature shows that when the net capacitances are not dominating, the best way to reduce the dynamic current is to reduce the transistor channel width. Also, when the routing capacitances are greater than the gate capacitance, dynamic current gain can be improved by lowering V_{DD} [5]. However, reducing the supply voltage is associated with increasing the subthreshold voltage in order to maintain the circuit performance and the later increases the leakage current and hence the static power.

The following sections will discuss the static and dynamic power dissipation reduction techniques which have been reported in the literature for both Bulk and SOI

transistors. Static and dynamic power reduction techniques are either structure level or circuit level but in this thesis, the main focus is on the structure level.

3.2.1 Dynamic power dissipation reduction techniques. Several methods have been adopted to reduce dynamic power dissipation for both bulk and SOI transistors, such as reducing the supply voltage V_{DD}, C_L, the activity factor α and frequency. Generally, in order to maintain the circuit performance, reducing the supply voltage and the switching capacitance are the two main factors followed by power reduction techniques. A statistical study for a digital circuit shows that 55% of the wire connections between standard transistor cells are dominated by the gate capacitance [5]. By taking the first scenario of decreasing the dynamic power by decreasing the supply voltage of a ring oscillator. The results showed that frequency of the ring oscillator (RO) is decreased strongly. So as a solution, threshold voltage got decreased in order to maintain the saturation current. It was shown that up to 20% in dynamic current reduction can be obtained by decreasing the transistor width by 45 % for both NMOS and PMOS [5].

Another method for the reduction of dynamic power dissipation is the optimization of the supply voltage (V_{DD}) and the threshold voltage (V_{th}). It is found that to reduce power consumption, leakage power to total power ratio is set to 30%. The optimum threshold voltage at the highest temperature and lowest process variation ranges from 0 to 0.1 V. Decreasing the supply voltage will drastically decrease the power dissipation, because the power dissipation quadratically decreases with decreasing V_{DD} [6]. However, decreasing V_{DD} will lower the circuit performance. To maintain the circuit performance, the threshold voltage could be decreased which will result in exponential increase in the subthresthold leakage current. As such, the best way is to find the optimum V_{DD} and V_{th} which will lead to lower the power consumption. A new drain current model is proposed in [6] which provides smooth transition between the threshold and the subthreshold voltage.

$$I_D = \begin{cases} I_0 e^\alpha \left(\dfrac{V_{GS}-V_{th}}{\alpha N_s}\right)^\alpha & (V_{GS} \geq V_{th} + \alpha N_s) \\ I_0 e^{\frac{V_{GS}-V_{th}}{N_s}} & (V_{GS} \leq V_{th} + \alpha N_s) \end{cases} \tag{18}$$

where α is the velocity saturation index and N_s is the subthreshold slope (nkT/q)

The study took into account temperature and process variations. Also, it tried to model all parameters that may be affected by temperature variation, such as mobility, threshold voltage and subthreshold slope [6]. It was found that in the subthreshold region, the CMOS shows positive temperature dependence because lowering the threshold effect is stronger than the mobility degradation. It was also shown that the dynamic power dissipation was the worst at the highest operating temperature. This is because the leakage current is affected by temperature and dynamic power does not depend on it. It is found that the optimum V_{th} is a function of the activity factor not the clock frequency [6]. Finally, two equations have been reached in order to compute the optimal threshold and optimal supply voltage V_{DD} to get the lowest power dissipation and maintain the circuit performance at the same time.

$$V_{THopt} = -N_s \ln\left(\frac{2afC_L N_s}{I_0}\frac{\alpha}{\alpha-\aleph}\right) \qquad (\alpha > \aleph) \qquad (19)$$

$$V_{DDopt} = \frac{-N_s \ln\left(\frac{2afC_L N_s}{I_0}\frac{\alpha}{\alpha-\aleph}\right)+\Delta V_{th}+k\Delta T+\frac{\alpha-1}{\alpha}\aleph}{1-\frac{\aleph}{\alpha}} \qquad (20)$$

where α is the activity factor, I_0 is the drain current when $V_{GS} = V_{th}$ at lowest temperature, ΔT is $T_{max} - T_{min}$, ΔV_{th} is the peak-to-peak variation through process, f is the given clock frequency, K is the delay coefficient, α is the velocity saturation index, k is the temperature coefficient and $\aleph$ equals $\left(\frac{fL_d KC_L}{\beta}\right)^{1/\alpha}$ [5].

Introducing SOI transistor to the silicon integrated circuits industry has enormously reduced both static and dynamic power dissipation compared to the bulk transistor. Furthermore, to solve the problems which resulted from scaling down the CMOS technology, FinFET and Tri-gate transistors were introduced. They are able to provide massive current per footprint at low voltages because of the channel 3-D conduction. However, they have high parasitic and gate capacitance which increase the active power dissipation [26].

One paper [26] demonstrated the features of FD SOI transistors for power management and adjusting the threshold voltage to decrease dynamic power dissipation. It investigated the FD-SOI for 14 nm, which is used for high speed and efficient energy applications, and 28 nm for same static power and a difference of supply voltage of 100 mV; 14 nm has less supply voltage than the 28 nm by 100 mV. The results showed that

the speed delay reduced by 34% from 28 nm to 14 nm [25]. It is an interesting finding that the static power can be reduced by light channel doping and reverse back bias. However, the dynamic power can be reduced by forward back bias at the same speed. FD SOI has the reverse bias technique which is effectively important for dynamic power optimization [26]. As FD SOI has improved electrostatic features which allows designing shorter gate length and higher poly length biasing range compared to the bulk technology. The 14 nm FDSOI technology has shown a 20% reduction in the delay gain at the same static power and lower supply voltage by 100 mV compared with the 28 nm technology [26]. The speed frequency has improved by more than 50% in the 14 nm technology at 0.8 supply voltage compared to 28 nm technology at 0.9 supply voltage. As a result, 14 nm technology can run faster at lower supply voltage compared with the 28 nm technology and hence lower dynamic power dissipation will be obtained [26].

For FD SOI, two architectures can be used; the first one is the regular wall which can be considered as a transition from the bulk transistor to the FD SOI, the P-well is under the NMOS and the N-well is under the PMOS. However, in the flip wall architecture, the P-well is under the PMOS and the N-well is under the NMOS and in order to avoid the diode conduction between the N-well to the P-well, the P-well is connected to the ground. This results in V_{th} shift of 70mV for FDSOI transistors with a 20nm BOX and a body factor of 70mV/V. Also, the V_{th} is shifted by 140 mV from regular to flip well architecture [26]. Thus, NMOS and PMOS cannot have the same threshold voltage for both architectures. In order to tackle this problem, the PMOS can be grounded or a second metal gate work function can be introduced in order to adjust the threshold voltage in the regular well. Wells are adapted to either reverse back bias in the regular well architecture to minimize leakage current or a large forward back bias in super low threshold (SLVT) to maximize the speed.

By tuning the threshold voltage between the slow to fast process, the back bias is applied to maximize the power efficiency [26]. Results showed that devices running at 0.63 threshold voltage with 2V forward back biasing are as fast as devices running at 0.8 V with no back biasing which results in 40% dynamic power reduction [26]. However, the static power has increased because the FBB has lower threshold voltage [26]. Low threshold (LVT) device in the flip well is mixed with the SLVT and regular threshold (RVT) device is mixable with the LVT with adequate ploy biasing can

improve the speed and leakage optimization. One decade leakage reduction is resulted after a light channel with boron and phosphorus implants [26].

For dynamic power dissipation, [7] investigated power dissipation reduction in NMOS, PMOS, CMOS and NAND gate using SIO2 oxide layer and high k layer each of 45 nm, 32 nm and 22 nm technologies. Simulation results showed that the dynamic power dissipation with high k layer is low for the NMOS, PMOS and CMOS for all technologies in comparison with SiO2 oxide layer. However, the static power in NMOS with high k layer increases due to the tunneling of electrons from the gate. It was observed that lowest power dissipation in dynamic and static is in PMOS 45 nm technology. Whereas for NMOS, it was observed that the maximum power reduction for dynamic power dissipation is in 32 nm technology with very slight difference compared to 45 nm technology and 22 nm technology for lowest static power dissipation [7]. The following Table 1 shows the percentage of dynamic and static power dissipation reduction for 45, 32 and 22 nm for a CMOS inverter [7].

Table 1: Dynamic and static power dissipation reduction percentages for CMOS inverter [7]

Technology	Dynamic Power Dissipation (W)		% Reduction in power	Static Power Dissipation (W)		% Reduction in power
	CMOS	High K		CMOS	High K	
45 nm	220.36n	6.412n	97.09	36.30p	96.09f	99.73
32 nm	365.12n	9.48n	97.40	83.30p	186.48f	99.77
22 nm	618.90n	247.5n	60.00	169.11p	213.4f	99.87

However, for CMOS inverter, which is evident in Table 1, the percentage of maximum power dissipation for static and dynamic occurs in 45 nm technology with 99.98% for dynamic and 99.93% for static [7].

Another published methodology is to reduce dynamic power dissipation at the circuit-level by clustering a number of gates and making one single large sleep transistor responsible for them. However, when the structure is unbalanced and have complicated interconnections, this methodology is not preferable and sharing one sleep transistor will increase the interconnections' resistance for the far blocks [1]. Moreover, the size

of the sleep transistor will get larger to compensate for the increased interconnect resistance.

A vector is created and has the values of the discharge currents, and the time slots are divided into 10 psec. The time slots contain the time and the corresponding discharge current. For every gate in the circuit, a vector is created and contains the fanout; the duration of the switching, the peak current, the delay of the gate; the peak current time and the magnitude of the peak current. The gates where clustered in 7 sub-clusters with unequal number of gates. The gates where clustered in such a way the maximum discharging current in each sub-cluster will not exceed the maximum current limit of the sleep transistor. Two sub-techniques are followed to decrease dynamic power dissipation, which are the bin-packing technique and the set-partitioning technique. Bin-packing technique, assumes n items (gates) and m bins (sleep transistors), it performs a linear programming algorithm in order to minimize number of clusters which indicates number of sleep transistors. This technique shows a reduction of 17% in the dynamic power dissipation due to the fact that it reduces the total area of sleep transistors [1].

However, in set-partitioning technique, m currents (gates) divided into groups where each element is counted one in each group, and the cost function is evaluated for each group such that it counts the physical distance of each gate. The set-partitioning algorithm finds the cost function (distance between the gates) and the sum of gate currents which does not exceed the maximum current limit of the sleep transistor [1]. Thus, it finds the total number sleep transistors for a cluster of gates that satisfy the current and distance constraints. It was found that the close transistors were grouped together in order to minimize the wire length. This technique shows reduction of 11% in dynamic power due to the reduction of capacitance due to the down-sizing of the sleep transistor [1].

3.2.2. Static power dissipation reduction techniques. Various static power reduction techniques have been presented in the literature. Starting with the structure level, a method presented in [3] suggests reducing the power consumption by 30% by reducing the 1/f noise. This is done by applying switched biasing to the circuit by driving the MOS from strong inversion to accumulation. Also, this technique reduces the flicker noise by turning the bias current to off when it is not contributing to the circuit operation.

It applies switched biasing to sawtooth oscillator [3]. Flicker noise became a serious problem as transistor size scales down, not only at low frequency, but also high frequency in active mixers and voltage controlled oscillator (VCO). The switching biasing technique is based on applying a square signal supply voltage, which has two states, the high state in which the V_{GS} is above the threshold voltage when the MOS is in strong inversion and the low state is when the supply voltage is below the threshold voltage and the MOS is in accumulation [3].

The dual threshold voltage in MTCMOS is a technique to reduce static power dissipation. This technique uses variant threshold voltage, high threshold voltage for gates in non-critic   al paths and low threshold voltage for gates in critical paths. However, this technique is complex in fabrication because it needs different oxide layers for each value of V_{th} [2]. Also, this technique suffers from latency when the circuit in the idle state and then activated. However, the sleep mode approach tends to add a sleep transistor between the supply voltage and the ground in order to reduce the sub-threshold voltage [2]. Precisely, it inserts a sleep PMOS transistor between the V_{DD} and the pull-up network and a sleep NMOS transistor between pull-down network and the ground. These sleep transistors turn off the circuit and provide very low resistance in the conduction path and turns them off by powering off the V_{DD} and provide very high resistance in the conduction path. Hence, leakage current will be reduced by turning of the power rail using the sleep transistors. This technique is also called gated-V_{DD} and gated-GND [2]. Moreover, another approach, which is the stack approach, forces a stack effect by breaking a transistor into two half-sized transistors. A reverse bias current is produced when two transistors are off and hence it reduces the sub-threshold leakage current. However, this introduces a delay between the break down transistors [2].

The sleepy keeper approach suggests using an output voltage of 1 and an NMOS transistor in parallel to the pull-up network and a PMOS transistor in parallel to the pull-down network. So, in the sleep mode, the sleep transistor is off and the NMOS transistor is the only source for the V_{DD} so logic 1 will be maintained and leakage power is reduced. However, the percentage of the reduced power is very small and does not meet the current VLSI circuits [2].

A technique presented in [1] suggests using transistor gating to reduce leakage power dissipation. This paper presented a technique to reduce leakage power by adding

an NMOS and a PMOS transistor (sleep transistor) in the path from V_{DD} to ground. In the standby mode, the sleep transistors turn off and hence increase the resistance in the path from V_{DD} to ground. This technique reduces the leakage power but introduces a delay.

Power gating technique is used to reduce the leakage power by turning OFF the devices when they are not in use by switching off the power supply. It uses sleep transistors, a PMOS transistor is added in series between the power supply and the pull-up network and an NMOS transistor between the pull-down network and ground [27]. The sleep transistor turns on when the circuit is active and off when it is inactive. The MTMOS technology uses high threshold transistors as sleep transistors. In critical path, low threshold transistors are used to maintain performance and in non-critical path, high threshold transistors are used to reduce the leakage power. Another technique is the drain gating which uses an extra sleep transistor between the pull-up and the pull-down networks to reduce the leakage power [27].

The transistor gating technique is done by adding extra sleep transistors between the V_{DD} and ground [26]. A PMOS is inserted between the V_{DD} and the pull-up network and an NMOS between the pull-down and the ground. When the device is active, the transistors are ON and hence proper biasing is done in order to reduce the path resistance from V_{DD} to ground; high voltage for PMOS and low for NMOS. When the device is in standby mode, the sleep transistors are OFF and proper biasing is done to increase the path resistance and produce a stacking effect to reduce the leakage power; high voltage for NMOS and low for PMOS [27]. The results were obtained by designing one bit full CMOS adder. The results show that by using the basic circuit of full adder, the leakage power is 90.78 pW. The resulted leakage power in the forced stacking technique is 134 pW and for the proposed idea is 84.5 pW. Moreover, the results show that in standby mode the power is reduced up to 96% compared with active mode. However, this technique produces delay of 234 ps because of the added sleep transistors [27].

Another paper compares the performance of the double-gate SOI MOSFET with the conventional bulk MOSFET [28]. It shows that DG SOI MOSFET has a great importance because of the SOI back biasing feature which affects the threshold voltage. As technology scales down, there has been a trade-off between the standby power and the design performance which led to the introduction of a new architecture which is the

multiple gate FET. The multiple gate FET can achieve better drain-induced-barrier-lowering (DIBL) effect and subthreshold performance and hence reduces the power dissipation and by using high-K gate dielectrics, gate leakage can be reduced. However, leakage current can be reduced by using stacked transistor and changing the threshold voltage through body biasing but this leads to an increase in the time delay. This paper holds a comparison between the bulk MOSFET and the DG SOI MOSFET in terms of performance and standby power when using stacked transistors and body biasing techniques [28]. It shows that DG MOSFET has significant advantages when implementing back biasing and stacked transistors. The vehicle transistor is a ring oscillator circuit using 25 nm channel length CMOS inverters using stacked transistors to reduce the standby power and the back biasing is applied to the lower transistor. Stacked transistors and negative reverse back biasing can effectively reduce the leakage current [28].

S_{tot} is a figure of merit that measures the effectiveness of the Reverse Body Biasing (V_{BB}) technique in reducing the leakage. The results showed that the threshold voltage has a linear dependency on V_{BB}, and a technology-dependent parameter called λ_{bb} is twice in SOI than in the bulk MOSFET. Also, it was found out that SOI MOSFETs have better device subthreshold slope S_t and hence smaller S_{tot} and thus less leakage reduction. However, reducing the leakage subthrehsold current has led to reduce the device speed (more in SOI) and an increased delay due to the fact that V_{th} has increased while it has linear relation with V_{BB} [28]. Moreover, the reduction in the leakage current has led to the cost of energy dissipation due to the charging and discharging of the back-gate to bulk capacitances. The bulk MOSFET has a bulk or back gate capacitance (C_B) almost twice as large as the SOI devices, essentially because of the source/drain to bulk junctions (whose forward bias is also responsible for the C_B increase for positive V_{BB}). The figure of merit is 16 times smaller in SOI compared to bulk MOSFET due to reduced C_B value and hence lower the energy dissipation overhead [28].

As for circuit level, the full adder, using 0.15 um FD SOI technology and 1.5 V supply voltage, was compared with that of CMOS using SPICE simulation. It shows that static power of SOI FD is half that of the CMOS. Theoretical results show that the power consumption of the SOI full adder is 0.5 µW at 100 MHz and it is much lower than the full adder CMOS by a factor of 2.8 [29]. However, these results were obtained

before designing the layout and without taking into account the routing capacitance which will increase the power consumption. The simulation results showed a higher power consumption factor (a factor of 2) as proved by theoretical results [29].

As aforementioned, Pin-packing technique has shown a reduction on average by 17% in dynamic power and 90% in leakage power [1]. Moreover, the set-petitioning technique has shown a reduction of 77% in static power dissipation [1].

By now, most of the power reduction techniques for both dynamic and static power dissipation have been reviewed. In order to investigate the CMOS dynamic power dissipation, basics of dynamic power dissipation in CMOS devices is studied thoroughly and presented in the next chapter.

Chapter 4: Dynamic Power Dissipation in CMOS

This chapter describes the CMOS switching with and without load capacitance and how the power is dissipated during switching activity. Moreover, it describes how the dynamic power dissipation differs when the CMOS is driving a load capacitance. It also discusses the developed dynamic power dissipation model in literature. The followed methodology in finding the average dynamic power dissipation from the simulation is explained fully. The mathematical model for calculating the dynamic power dissipation theoretically is also well discussed.

4.1. Operation of CMOS Inverter

Figure 11 shows the CMOS inverter circuit diagram without C_L. It is composed of a pull-up network; PMOS, and a pull-down network; NMOS. When the input is low; 0 V, the PMOS is ON and the NMOS is OFF. Therefore, the NMOS is in cut-off region and the PMOS is in the triode region. As such, there is a direct path from the supply voltage V_{DD} to the output and hence the later is equal to V_{DD} [30]. However, when the input is high; equals to V_{DD}, the PMOS is in cut-off region and the NMOS is in the triode region. Hence, there exists a direct path from V_{DD} to ground causing the output to equal 0 V. Whilst, when the input is transiting from low to high and just exceeding the PMOS threshold voltage $V_{th,n}$, the NMOS turns ON and becomes in saturation and the PMOS is still in triode. As such the current flows through both devices and power dissipation is no longer zero. As input voltage increases, it comes a point when the input and output voltages are equal and equal to V_M and hence both NMOS and PMOS are in saturation when maximum power dissipation occurs. When the input is getting higher than V_M but lower than $V_{DD} - V_{th,p}$, the PMOS is in saturation and the NMOS is in triode [30]. Finally, when the input is equal to V_{DD}, the PMOS turns OFF and the NMOS is in triode region and the output is 0 V. To discuss the transient behavior of the CMOS BULK inverter, consider the pulse signal with 1.0 ps rise and fall times and 10 ns pulse width shown in Figure 12. This pulse is applied to the inverter input. The instantaneous output voltage $V_{out}(t)$ is shown in Figure 13.
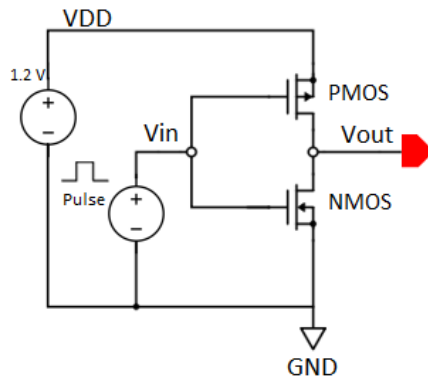
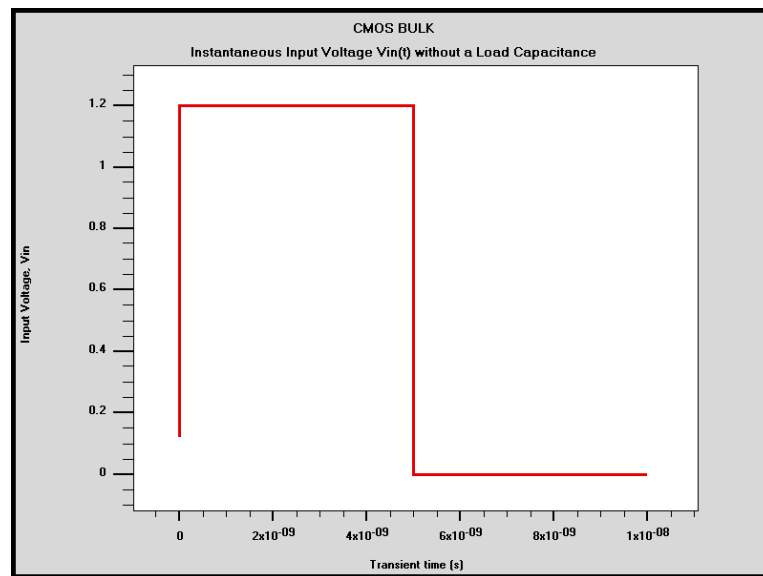Figure 11: CMOS inverter circuit with no load capacitance

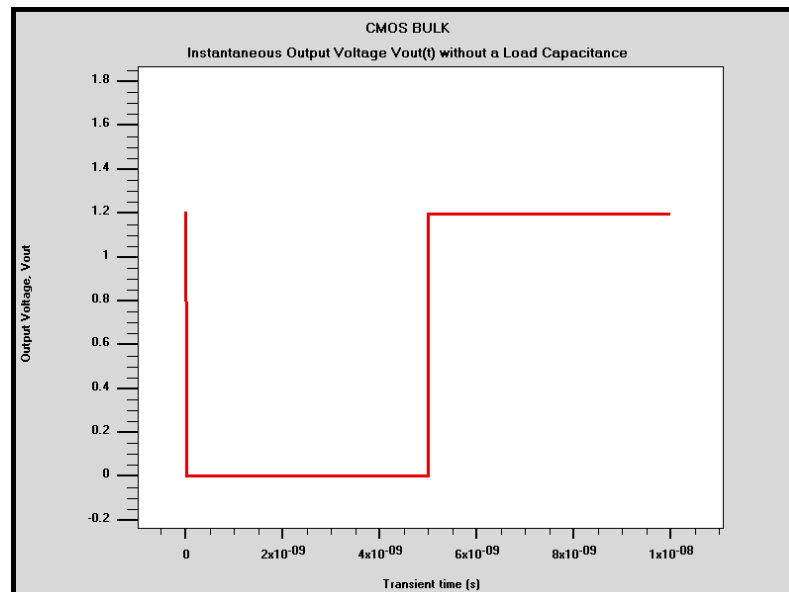Figure 12: Instantaneous input voltage $V_{in}(t)$ without a load capacitance

Figure 13: Instantaneous output voltage $V_{out}(t)$ without a load capacitance

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4.2. Charging and Discharging of C_L

When the CMOS BULK inverter is driving C_L, the dynamic power dissipation occurs in the resistive path while charging and discharging C_L. In charging C_L, most of the power is dissipated through the PMOS. Whereas during discharging, most of the power is dissipated through the NMOS. Moreover, the output voltage takes time until C_L is completely charged or discharged as depicted in the CMOS BULK instantaneous output voltage $V_{out}(t)$ shown in Figure 14 when a pulse signal is applied to its input. The following Figures 15 and 16 show the equivalent circuits when the input is high and low respectively. As discussed earlier, when the input is 0 V, the PMOS is ON and NMOS OFF, the current $I_{D,p}$ flows through the PMOS and C_L is charged and the output equals V_{DD} as seen in Figure 14. Since in this case, the PMOS is in triode region, the PMOS is represented as a resistance R_p. Yet, when the input is high, the PMOS is OFF and the NMOS is ON, C_L is discharged through the NMOS causing a current $I_{D,n}$ to flow through the NMOS. In this case, the NMOS is presented as a resistance; R_n. The charging and discharging of C_L have different time constants; τ_c and τ_d, according R_n and R_P values. The time constants τ_c and τ_d can be found from equations (21) and (22) respectively [30].

$$\tau_c = R_p C_L \tag{21}$$

$$\tau_d = R_n C_L \tag{22}$$
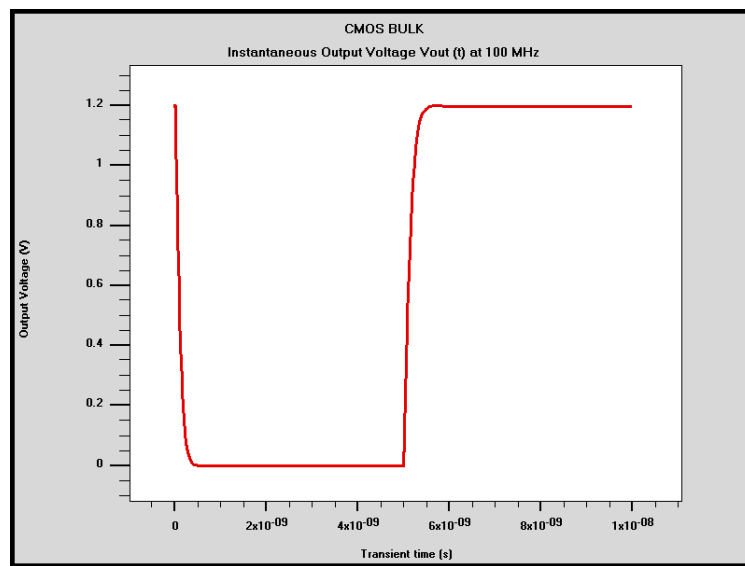
Figure 14: Instantaneous output voltage $\mathbf{V_{out}(t)}$ at 100 MHz

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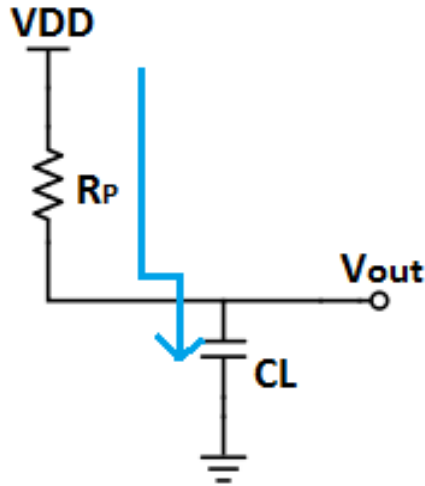
Figure 15:CMOS inverter equivalent circuit when the input is low
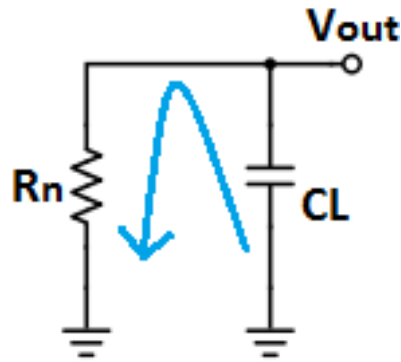
Figure 16: CMOS inverter equivalent circuit when the input is high

Theoretically, the dynamic power dissipation in CMOS inverter is calculated using equation (15) and the derivation is explained in the following paragraphs. Considering the CMOS inverter charging equivalent circuit in Figure 15, the instantaneous current of C_L is $i_c(t)$ is [10]

$$i_c(t) = \frac{dq(t)}{dt} = C_L \frac{dV_{out}(t)}{dt} \tag{23}$$

$$i_c(t) = \frac{V_{DD} - V_{out}(t)}{R_p} \tag{24}$$

By equating equations (23) and (24):

$$\frac{dV_{out}(t)}{dt} = \frac{V_{DD} - V_{out}(t)}{R_p C_L} \tag{25}$$

In order to find $V_{out}(t)$, both sides of equation (25) are integrated,

$$\int \frac{dV_{out}(t)}{V_{DD} - V_{out}(t)} = \int \frac{dt}{R_p C_L} \tag{26}$$

$$\ln(V_{DD} - V_{out}(t)) = \frac{-t}{R_p C_L} + A \tag{27}$$

where A is a constant.

By taking $t = 0$ and $V_{out}(t) = 0$ as initial conditions, A equals $\ln V_{DD}$ and as a result [10]:

$$V_{out}(t) = V_{DD}(1 - e^{\left(\frac{-t}{R_p C_L}\right)}) \tag{28}$$

This is the resulted output voltage when C_L is cahrged. However, for discharging of C_L through the NMOS, equation (29) is followed:

$$V_{out}(t) = V_{DD}e^{\left(\frac{-t}{R_n C_L}\right)} \tag{29}$$

4.3. Power Dissipation during Charging and Discharging of C_L

Referring to equations (24) and (28), $i_c(t)$ is equal to [10]:

$$i_c(t) = \frac{V_{DD}}{R_p} e^{\left(-\frac{t}{R_p C_L}\right)} \tag{30}$$

The total energy which is delivered by V_{DD} per charging transition is found in equation (31) [10]:

$$E_{tran} = \int_0^\infty V_{DD} i_c(t) dt = \int_0^\infty \frac{V_{DD}^2}{R_p} e^{\left(-\frac{t}{R_p C_L}\right)} dt \tag{31}$$

$$E_{tran} = C_L V_{DD}^2 \tag{32}$$

The energy dissipated during charging per transition equals to equation (33) [10]:

$$E_{dissipated} = R_p \int_0^\infty i_c^2 dt = R_p \frac{V_{DD}^2}{R_p^2} \int_0^\infty e^{\left(-\frac{2t}{R_p C_L}\right)} dt \tag{33}$$

$$E_{dissipated} = \frac{1}{2} C_L V_{DD}^2 \tag{34}$$

and the energy stored in C_L during charging is [10]

$$E_{stored} = \frac{1}{2} C_L V_{DD}^2 \tag{35}$$

This stored energy will be dissipated in R_n during the discharging phase of C_L is:

$$E_{dissipated} = \frac{1}{2} C_L V_{DD}^2 \tag{36}$$

The dynamic power dissipation per transition is shown in the following equation:

$$P_{dynamic} = E_{tran} \, f_{ck} \alpha \tag{37}$$

Using equation (32),

$$P_{dyanmic} = C_L V_{DD}^2 \, f_{ck} \alpha \tag{38}$$

The average dynamic power dissipation in CMOS inverter is found by adding that in PMOS and NMOS. The average dynamic power dissipation theoretically is calculated using the following equation [10]:

$$\overline{P} = \frac{1}{T} \int_0^T V_{out}(t) \, i(t) \, dt \tag{39}$$

Re-writing equation (39) to find the average dynamic power dissipation in NMOS; $\overline{P}_n$ which is also the average dynamic power dissipation during discharging of C_L; $\overline{P}_d$ which is found from the following equations:

$$\overline{P}_d = \overline{P}_n = \frac{1}{T} \int_0^T V_{out}(t) \, i(t) \, dt \tag{40}$$

$$= \frac{1}{T} \int_0^T V_{out}(t) \frac{V_{out}(t)}{R_n} \, dt \tag{41}$$

$$= \frac{1}{TR_n} \int_0^T V_{out}^2(t) \, dt \tag{42}$$

$$\overline{P}_d = \frac{1}{TR_n} \int_0^T V_{DD}^2 e^{\left(\frac{-2t}{R_n C_L}\right)} \, dt \tag{43}$$

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$$= \frac{V_{DD}^2}{TR_n} \int_0^T e^{(\frac{-2t}{R_n C_L})} \, dt \tag{44}$$

$$\overline{P_d} = \frac{R_p C_L V_{DD}^2}{2TR_n} (1 - e^{\frac{-2T}{R_n C_L}}) \tag{45}$$

The same equation is used for finding the average dynamic power dissipation in PMOS; $\overline{P_p}$,which is the same as the average dynamic power dissipation caused by discharging of C_L; $\overline{P_c}$, by just replacing R_n by R_p as seen in the following equation (46):

$$\overline{P_c} = \overline{P_p} = \frac{R_p C_L V_{DD}^2}{2TR_p} (1 - e^{\frac{-2T}{R_p C_L}}) \tag{46}$$

4.4. Power Dissipation in Simulated Devices

In order to find the average dynamic power dissipation from simulation, equation (39) is used and re-written once for NMOS and once for PMOS are seen equations (47) and (48) respectively.

$$\overline{P_d} = \overline{P_n} = \frac{1}{T} \int_0^T V_{out}(t) \, i_{s,n}(t) \, dt \tag{47}$$

where $i_{s,n}$ is the NMOS source current.

$$\overline{P_c} = \overline{P_p} = \frac{1}{T} \int_0^T (V_{DD} - V_{out}(t)) \, i_{s,p}(t) \, dt \tag{48}$$

where $i_{s,p}$ is the PMOS source current.

Thus, the average dynamic power dissipation in the CMOS is:

$$\overline{P_{dynamic}} = \overline{P_d} + \overline{P_c} \tag{49}$$

$$\overline{P_{dynamic}} = \frac{1}{T} \int_0^T (V_{out}(t)i_{s,n}(t) + (V_{DD} - V_{out}(t)) \, i_{s,p}(t)) \, dt \tag{50}$$

In order to find $\overline{P_n}$, the instantaneous output voltage $V_{out}(t)$, which is shown in Figure 18, is multiplied by the instantaneous PMOS source current $i_{s,n}(t)$ which the later is presented in Figure 17. $\overline{P_n}$ is found by integrating the multiplication of $V_{out}(t)$ by $i_{s,n}(t)$ curve and diving the result by the period T.

The integration is found to equal 7.36 fW. Thus,

$$\overline{P}_n = \frac{1}{T}(7.36\times10^{-15})$$

at 100 MHz, $\overline{P}_n$ equals 0.736 µW.

The similar procedure is done to find the average dynamic power dissipation in PMOS which equals 0.737 µW. Then the CMOS average dynamic power dissipation is found by adding that of both NMOS and PMOS which equals 1.47 µW.
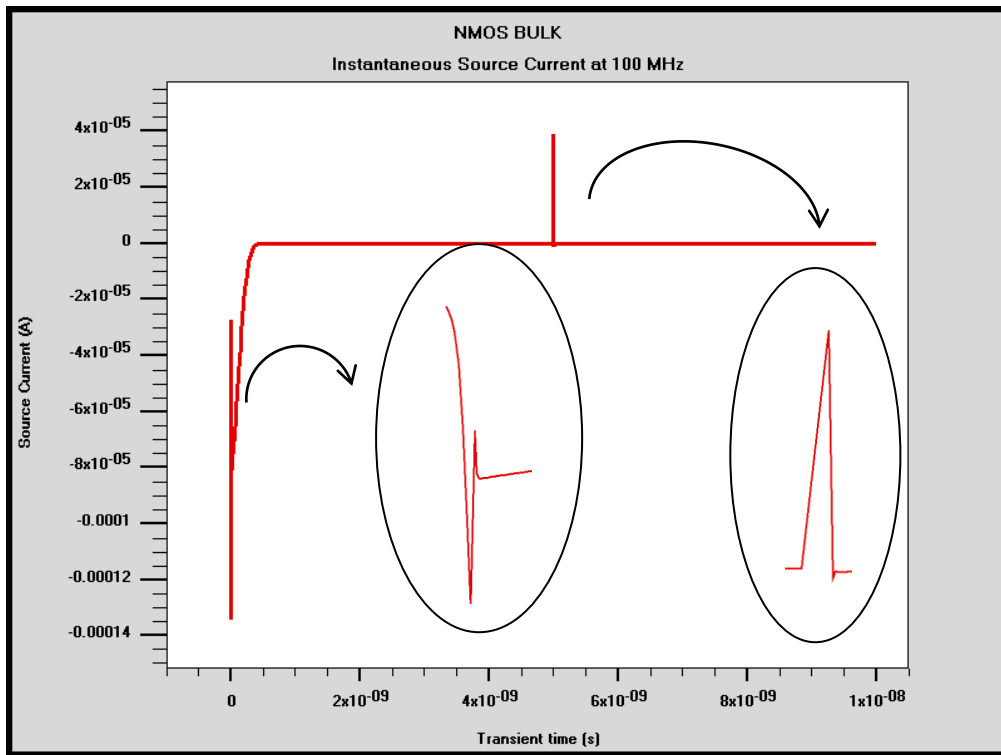
Figure 17: Instantaneous NMOS source current at 100 MHz

In order to investigate the CMOS dynamic power dissipation, the single NMOS and PMOS devices are first fabricated and simulated for bulk, SOI and SELBOX structures. The single devices are combined to fabricate the CMOS device for the same structures to investigate their dynamic power dissipation. The fabrication and simulation for NMOS and PMOS devices for the three structures are shown in details in the next chapter.

Chapter 5: Simulation of Device Fabrication

One of this work main objectives is to seek into the single and complementary devices fabrication. SOI MOSFET was introduced after the bulk MOSFET which tackles the bulk MOSFET drawbacks such as slow speed operation and high power dissipation. As such, SOI MOSFET was primarily suggested to provide low power dissipation. However, it turns out that FD-SOI MOSFET and PD-SOI MOSFET have the self-heating issue and PD-SOI MOSFET suffers from kink effect. These findings led to the introduction of the SELBOX MOSFET which combines the bulk and the SOI MOSFET advantages and surpasses their drawbacks. In order to hold a fair comparison between SELBOX, SOI, and bulk MOSFETs, the three architectures were fabricated with the same dimensions for single devices; NMOS and PMOS transistors. Also, CMOS device was fabricated for three architectures as well by combining NMOS and PMOS. Moreover, the calculations for NMOS threshold voltage and NMOS and PMOS mobilities' are illustrated in this chapter.

After the fabrication is done for all devices and architectures, the NMOS and PMOS drain current, I_D versus the gate to source voltage V_{GS} curve was simulated for the three architectures. Besides, the drain current versus the drain to source voltage V_{DS} curve for the same devices was obtained and is presented in this chapter.

5.1. Device Design and Dimensions

The fabricated devices have different dimensions. For instance, all single devices for all architectures have a length of 0.8 μm and a height of 0.6 μm. However, the three architectures CMOS devices have 0.8 μm and 1.2 μm length and width respectively. The channel length is 90 nm and the aspect ratio; channel depth over the channel length equal unity for all devices and architectures. However, in practice, the channel width of the PMOS is made 2 times wider than the NMOS to compensate for the mobility difference.

The channel length is chosen to be 90 nm because the static power dissipation became significant at 90 nm CMOS technology and beyond. As such, this thesis work focus on studying the dynamic power dissipation at the same CMOS technology [18].
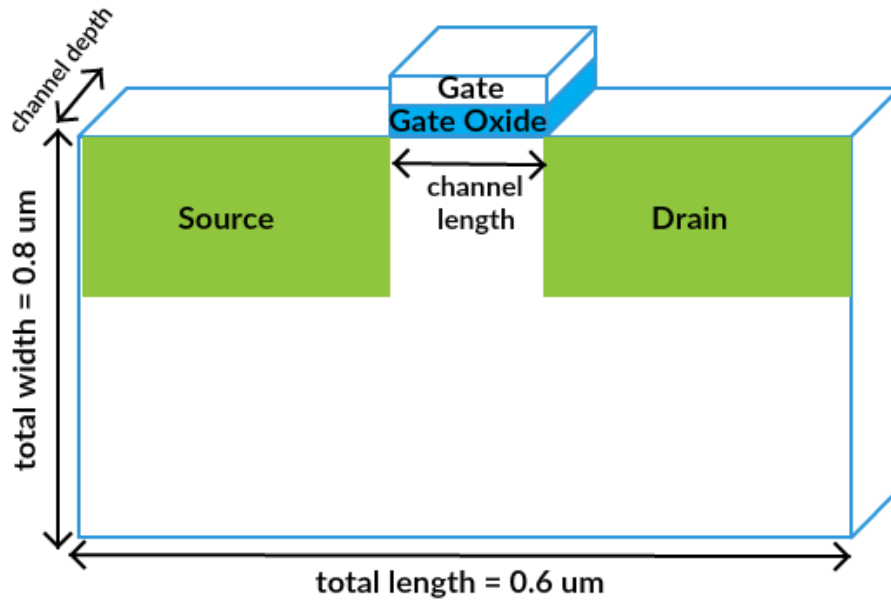
Figure 18: Bulk MOSFET structure dimensions

5.1.1. Single device. NMOS and PMOS were fabricated and simulated for the three architectures; bulk, SOI and SELBOX. Starting with the bulk structure, the bulk NMOS and PMOS device structures fabricated through simulation are shown in Figure 19 and 20 respectively and their dimensions are listed in Table 2. It is worth mentioning that bulk NMOS and bulk PMOS do not have the same dimensions.

Table 2: NMOS and PMOS bulk structure dimensions

Dimensions	NMOS	PMOS
Channel length	90 nm	90 nm
Average gate oxidization thickness	12.8 nm	12.8 nm
Doping depth	29.7 nm	40.5 nm

The SOI NMOS and PMOS devices were fabricated and simulated as depicted from Figure 21 and 22, their dimensions are listed in Table 3.

Table 3: NMOS and PMOS SOI structure dimensions

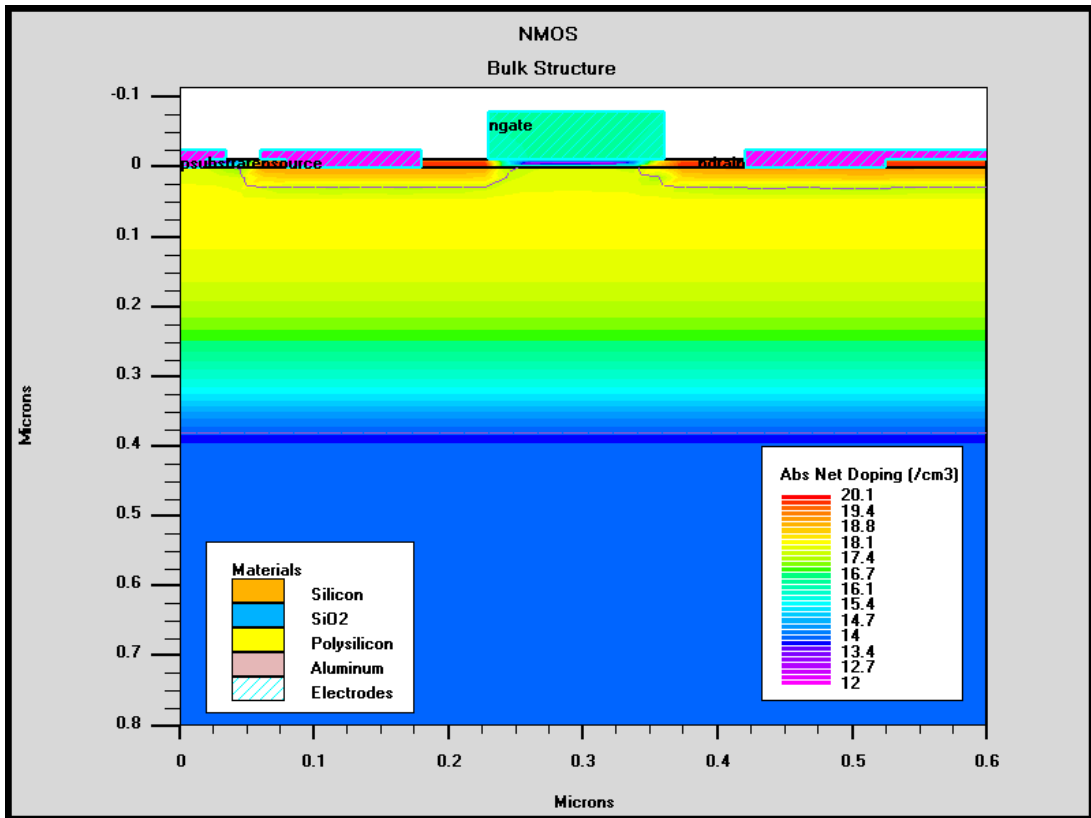| Dimensions	NMOS	PMOS
Channel length	90 nm	90 nm
Average gate oxidization thickness	12.9 nm	12.8 nm
Doping depth	28.8 nm	43.6 nm
Isolation thickness	0.2 µm	0.2 µm

Figure 19: N-channel bulk structure
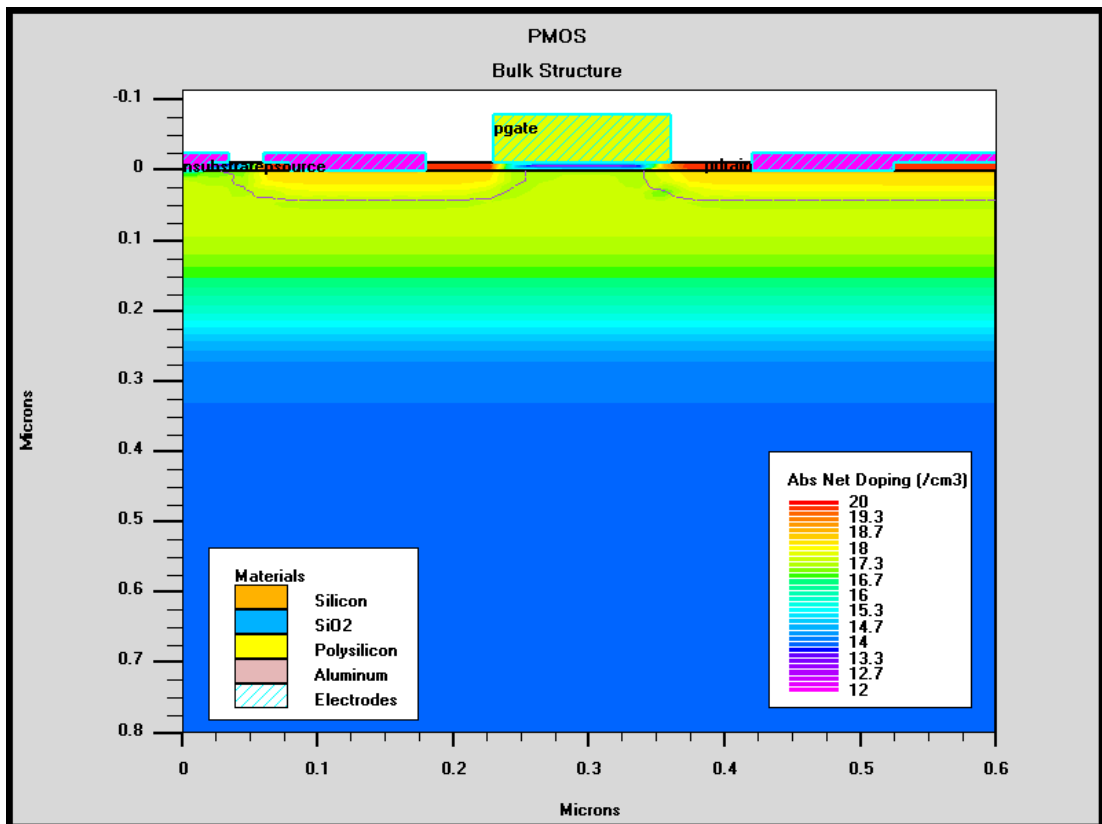
Figure 20: P-channel bulk structure

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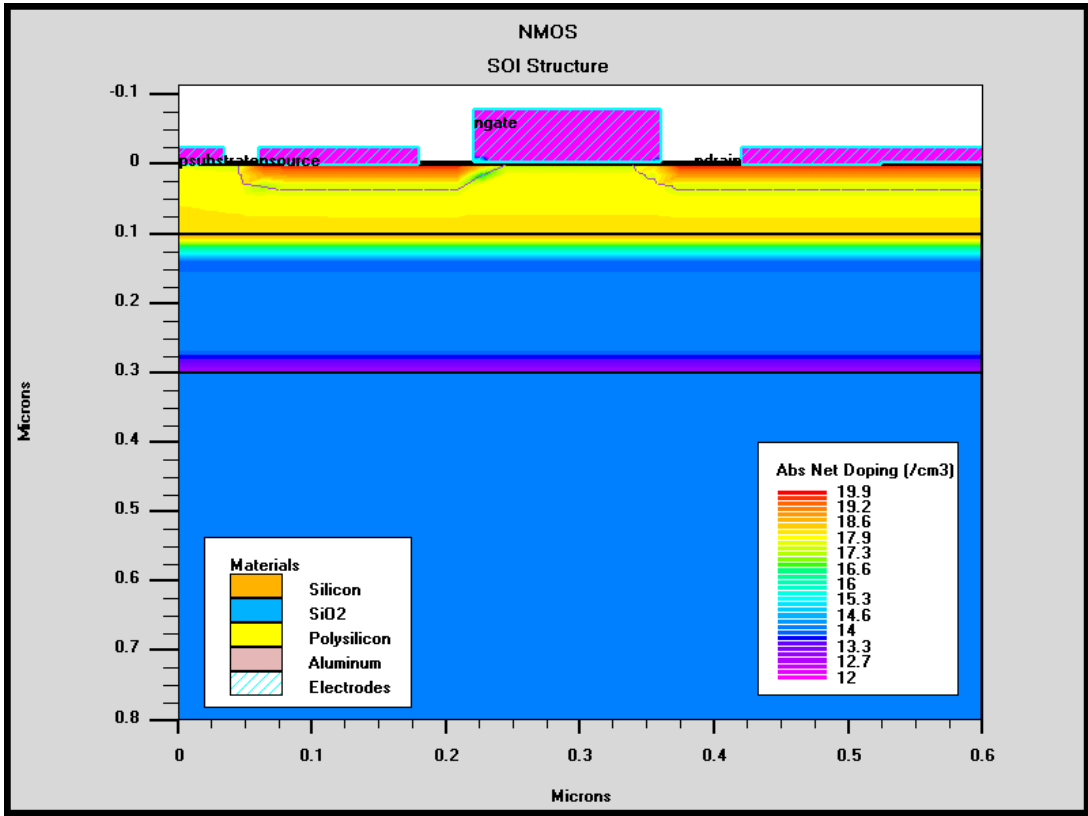
Figure 21: N-channel SOI structure
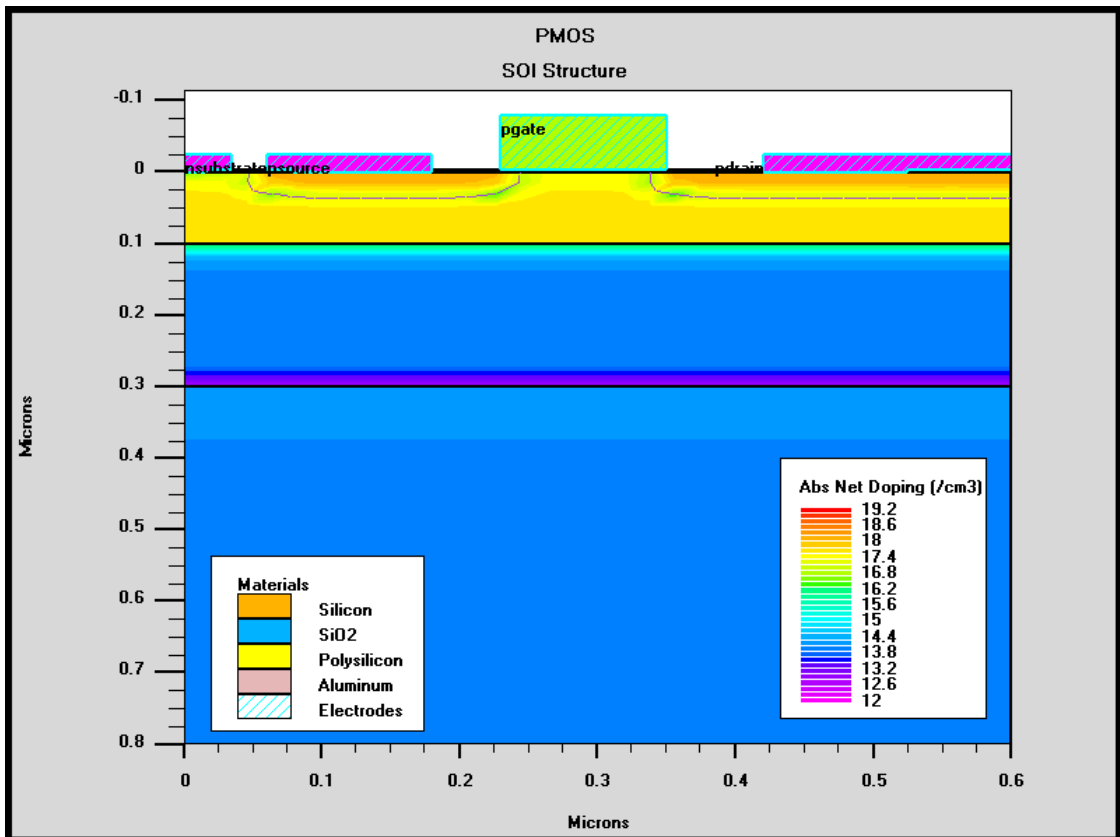
Figure 22: P-channel SOI structure

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Moving to the SELBOX structure, the fabrication of NMOS and PMOS devices are demonstrated in Figure 23 and 24 respectively. Their dimensions are listed in Table 4 below. The SELBIX gab width is selected to be 9 nm because it was found that 10% pf the channel length should be sufficient to eliminate the kink effect [21].

Table 4: NMOS and PMOS SELBOX structure dimensions

Dimensions	NMOS	PMOS
Channel length	90 nm	90 nm
Average gate oxidization thickness	6.44 nm	6.44 nm
Doping depth	55.4 nm	59.3 nm
Isolation thickness	0.2 µm	0.2 µm
Gap width	9 nm	9 nm
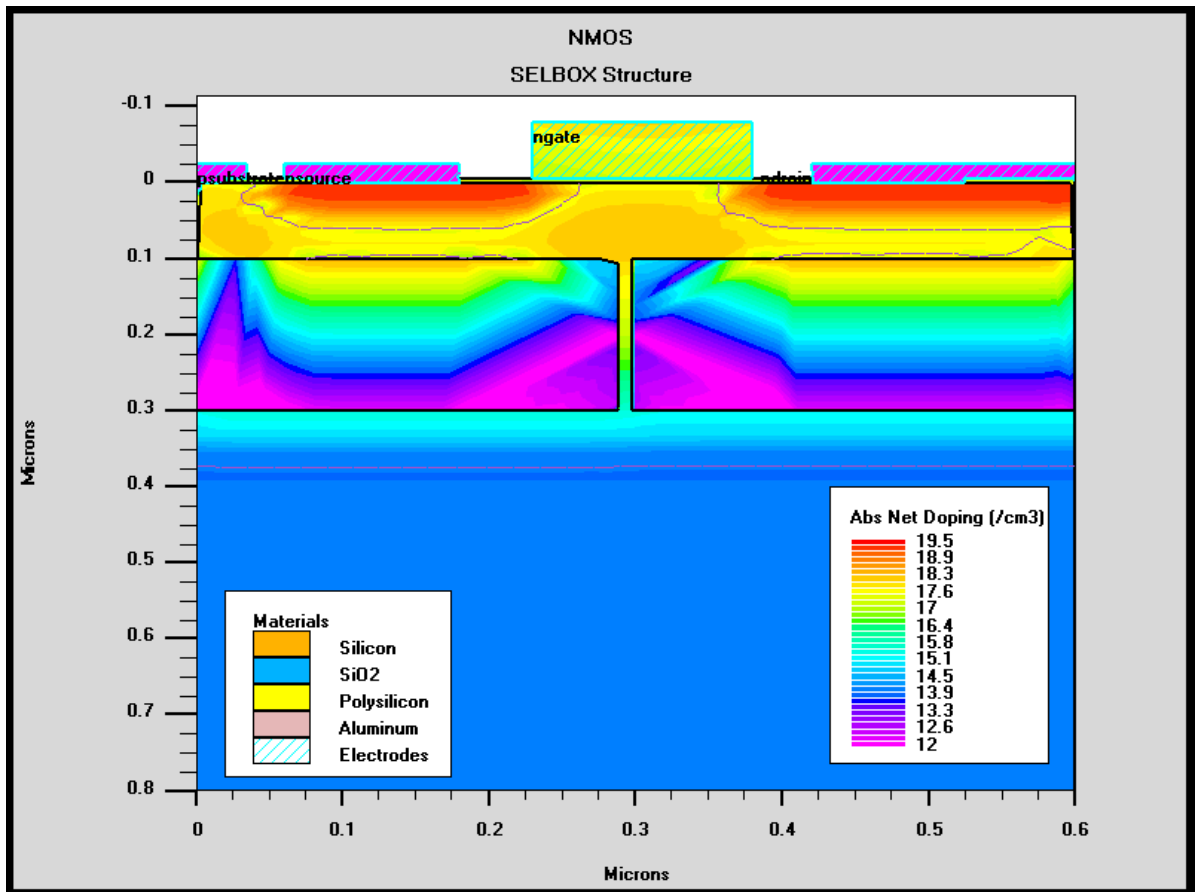
Figure 23: N-channel SELBOX structure
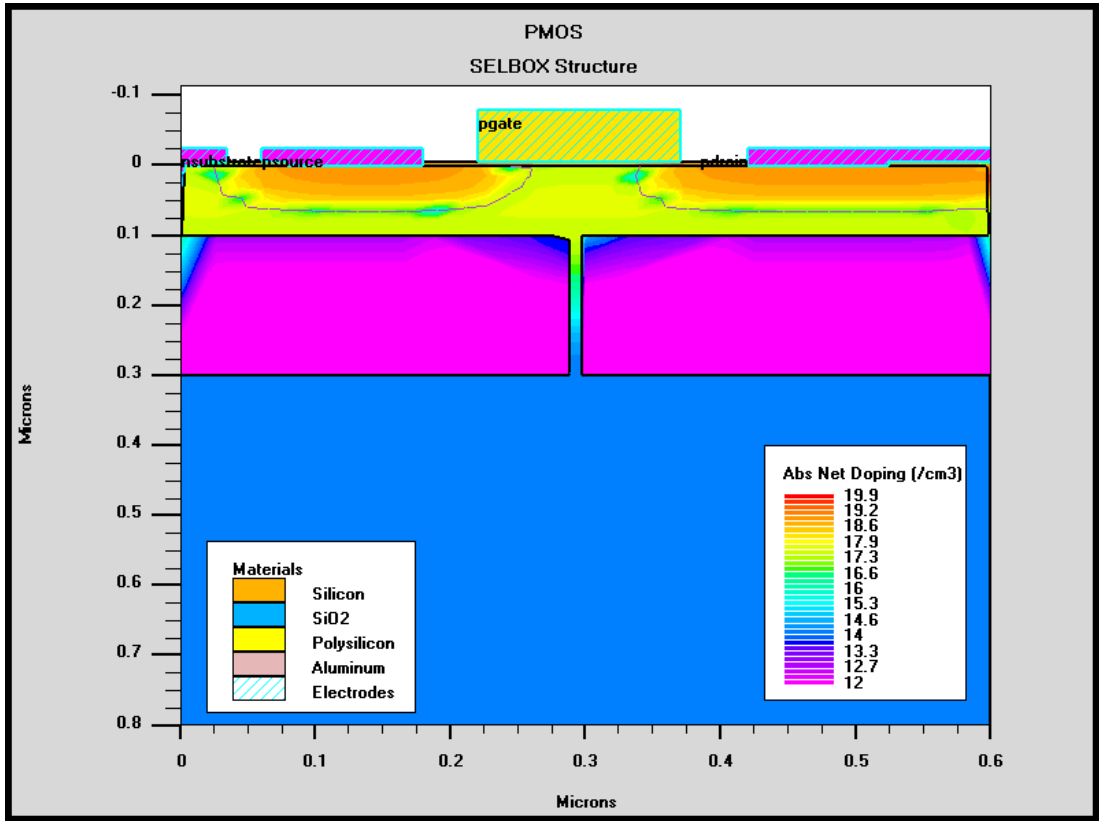
Figure 24: PMOS SELBOX structure

5.1.2. CMOS devices. After fabricating and simulating the single devices of the three architectures, the combination of NMOS and PMOS to yield CMOS device under bulk, SOI and SELBOX structures are implemented. The dimensions and fabrication of the CMOS devices for bulk structure are shown in Figure 25 and Table 5, respectively.

Table 5: CMOS bulk structure dimensions

Dimensions	NMOS	PMOS
Channel Length	90 nm	90 nm
Average oxidization thickness	6.3 nm	6.3 nm
Average doping length	50 nm	50 nm
Isolation thickness in between	100 nm	

Moreover, the CMOS SOI was fabricated and simulated by inserting an isolation layer in the substrate of the CMOS bulk as seen in Figure 26 according to the following dimensions.
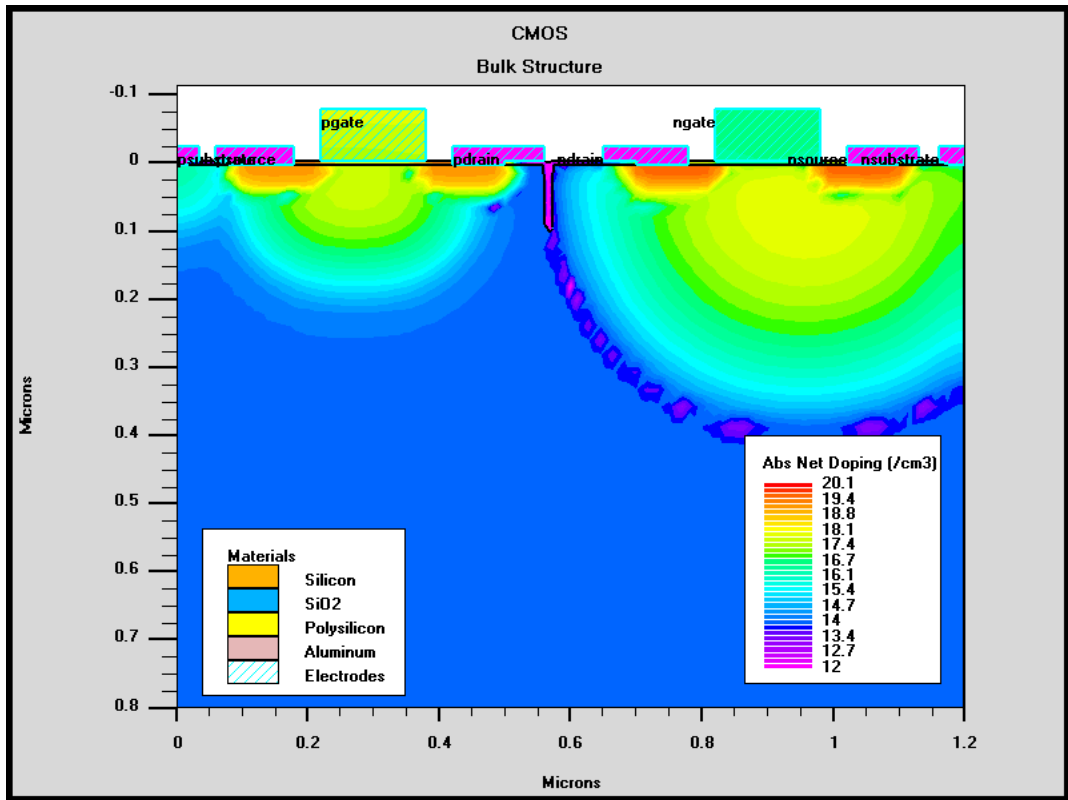
Figure 25: CMOS BULK structure
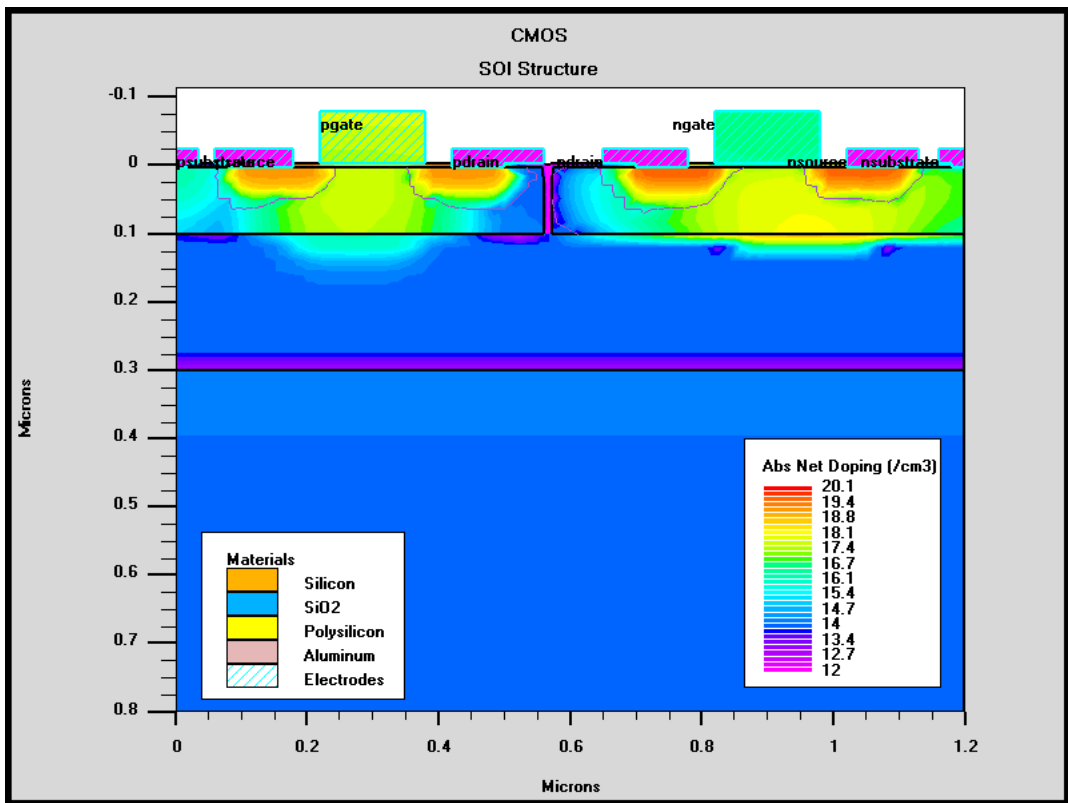
Figure 26: CMOS SOI structure

Table 6: CMOS SOI structure dimensions

Dimensions	NMOS	PMOS
Channel Length	90 nm	90 nm
Average oxidization thickness	6.3 nm	6.3 nm
Average doping length	50 nm	50 nm
Isolation thickness in between	100 nm	
Isolation width	0.2 µm	

The SELBOX CMOS was fabricated through simulation with dielectric isolation of the active NMOS and PMOS regions from the substrate as depicted from Figure 27. The dielectric employed in this case is not continuous between source and drain as in SOI devices. The dielectric segments cover regions below the source and drain and partially the region below the channel according to the following dimensions which are listed in Table 7.
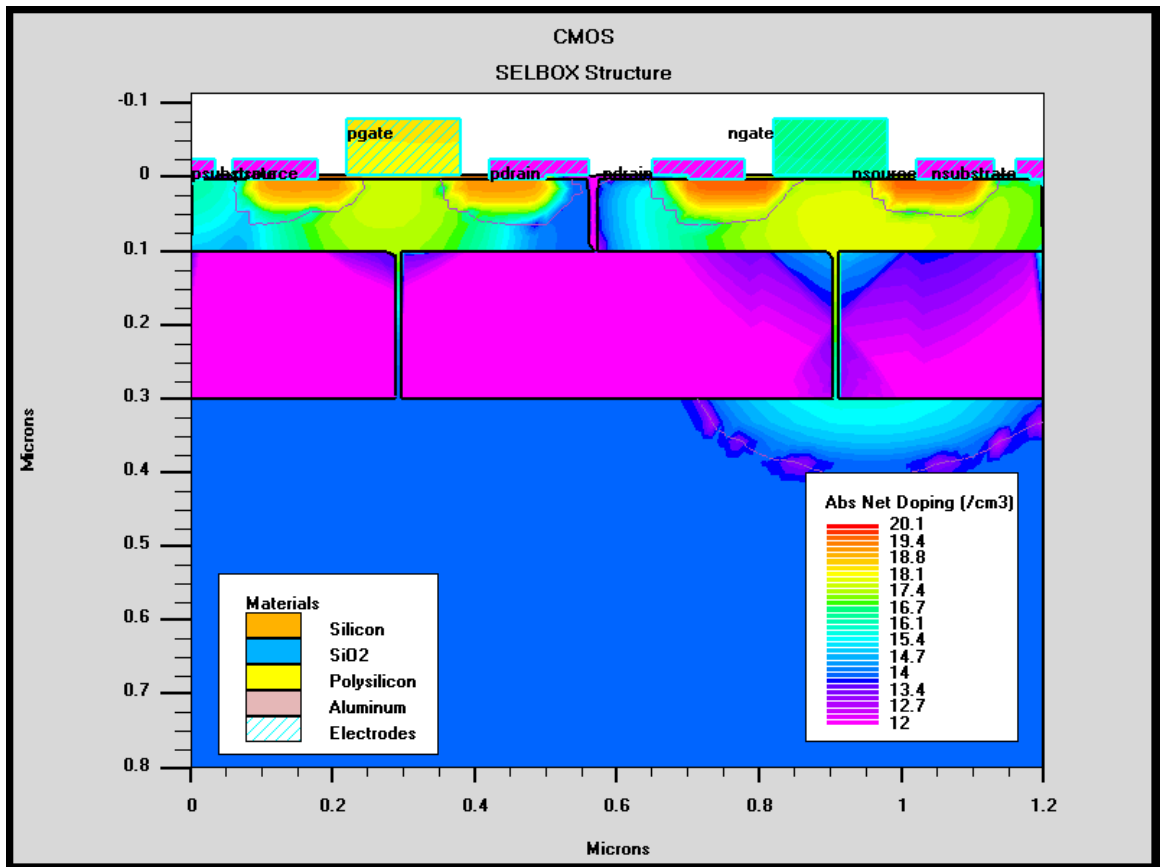
Figure 27: CMOS SELBOX structure

Table 7: CMOS SELBOX structure dimensions

Dimensions	NMOS	PMOS
Channel Length	90 nm	90 nm
Average oxidization thickness	6.3 nm	6.3 nm
Average doping length	50 nm	50 nm
Isolation thickness in between	100 nm	
Isolation width	0.2 µm	
Gap length	9 nm	

5.2. Device Parameters

Three major device parameters were calculated and simulated in this work; the threshold voltage V_{th}, the mobility µ and the oxide capacitance C_{ox}. These parameters were calculated and simulated using estimated parameters found from simulating the fabricated devices. The following Table 8 lists the device parameters which are used in simulating the devices.

Table 8: Device parameters

Parameters	Values	Units
Doping concentration of poly silicon ($N_{poly\ silicon}$)	2.26×10^{20}	cm^{-3}
Doping concentration of substrate (N_s)	1.0×10^{17}	cm^{-3}
Intrinsic doping concentration (n_i)	1.021×0^{10}	cm^{-3}
Boltzmann's constant (K)	1.38×10^{-23}	J/K
Room temperature (T)	300	K
Charge density (q)	1.6×10^{-19}	Coulomb
Permittivity of oxide (ε_{ox})	34.515×10^{-12}	F/m
Permittivity of silicon (ε_S)	103.545×10^{-12}	F/m
Electron affinity of the semiconductor (X_S)	4.05	V
Bulk potential (Φ_M)	4.05	V
Oxide thickness (t_{ox})	15	nm

5.2.1. Calculations of the NMOS bulk threshold voltage.

In order to calculate the threshold voltage, the thermal voltage V_T, the oxide capacitance C_{ox} should be first calculated as the follows [11]:

$$V_T = \frac{KT}{q} \tag{51}$$

$$= \frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} = 0.026 \text{ V}$$

$$\emptyset_f = V_T \ln \frac{N_s}{n_i} \tag{52}$$

$$= 0.026 \ln \frac{1 \times 10^{17}}{1.02 \times 10^{10}} = 0.419 \text{ V}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{53}$$

$$= \frac{3.9 \times 8.85 \times 10^{-12}}{15 \times 10^{\wedge}-9} = 0.0023 \text{ F/m}^2$$

$$\emptyset_{ms} = \emptyset_m - \left(X_s + \frac{E_g}{2q} + \emptyset_f\right) \tag{54}$$

$$= 4.05 - \left(4.05 + \frac{1.12}{2} + 0.419\right) - 0.979 \text{ V}$$

$$V_{th} = \emptyset_{ms} + 2\emptyset_f + \frac{\sqrt{2qN_s \times 2|\emptyset_f|\varepsilon_s}}{C_{ox}} \tag{55}$$

$$= -0.979 + 2(0.419) +$$

$$\frac{\sqrt{2(1.6 \times 10^{-19}) \times (1 \times 10^{23}) \times 2(0.419)(11.7 \times 8.85 \times 10 - 12)}}{0.0023}$$

$$= 0.58 \ V$$

5.2.2. Calculations of the NMOS and PMOS bulk mobility.

One of the main advantages of the NMOS over the PMOS is that the mobility in NMOS is higher than PMOS. This is because the electrons, which are the majority carriers in NMOS are faster than the holes, which are the majority carriers in PMOS. In order to calculate the mobility, some constant parameters, which are function of the doping density, should be used. The calculations of these parameters are listed in the Table 9.

Table 9: The parameters used to calculate the mobility as a function of the doping density [29]

Constants	Phosphorus	Boron	Units
$\mathbf{\mu_{min}}$	68.5	44.9	$\dfrac{cm^2}{V.s}$
$\mathbf{\mu_{max}}$	1414	470.5	$\dfrac{cm^2}{V.s}$
$\mathbf{N_{ref}}$	$9.2{\times}10^{16}$	$2.23{\times}10^{17}$	cm^{-3}
A	0.711	0.719	Null

The mobility can be calculated from the following equation [11]:

$$\mu = \mu_{min} + \frac{\mu_{max}-\mu_{min}}{1+\left(\frac{N}{N_{ref}}\right)\alpha} \quad cm^2/V \tag{56}$$

The N-channel mobility μ_n is:

$$\mu_n = 68.5 + \frac{1414 - 68.5}{1 + \left(\frac{1\times10^{17}}{9.2\times0^{16}}\right)(0.711)}$$

$$= 758.957 \ cm^2/V.s$$

The P-channel mobility μ_p is

$$\mu_p = 44.9 + \frac{470.5 - 44.9}{1 + \left(\frac{1\times10^{17}}{2.23\times0^{17}}\right)(0.719)}$$

$$= 321.833 \ cm^2/V.s$$

It can be concluded that the N-channel device mobility is two times greater than the P-channel device mobility. Consequently, the N-channel is better P-channel in switching applications. However, the P-channel devices have high noise immunity, are easy to control and have low cost processing.

5.3.   Single Device Simulation Results

After the fabrication is done for all devices and architectures, the NMOS and PMOS drain current, I_D versus the gate to source voltage V_{GS} curve was simulated for

the three architectures. Besides, the drain current versus the drain to source voltage V_{DS} curve for the same devices was obtained.

5.3.1. Single device I-V characteristics simulation. In this section, single device drain current versus gate voltage curve, from where the threshold voltage can be found, will be obtained. Moreover, drain current versus drain voltage curves for the three structures of the single devices will be demonstrated. The NMOS I_D vs. V_{GS} when drain to source voltage V_{DS} equals 2 V for the bulk, SOI and SELBOX structures are shown in Figure 28.

Theoretically, the threshold voltage is defined as the minimum gate voltage required to turn ON the device. As such and as it can be noticed from Figure 28, the threshold voltage for the N-channel bulk, SOI and SELBOX MOSFET structures are all the same and equal to 0.6 V. However, the drain current at VGS= 2 V is slightly higher in SOI and SELBOX than in bulk MOSFET.

The drain current vs. drain voltage curve was obtained for the N-channel for the bulk, SOI and SELBOX structures as shown in Figure 29, 30 and 31 respectively. N-channel bulk and SELBOX MOSFET exhibit similar drain current vs. drain voltage characteristics curves.

As for the P-channel device, the drain current vs. gate voltage curve when V_{DS} equals 2 V for the bulk, SOI and SELBOX structures are shown in Figure 32 below. The threshold voltage is found to be similar to the N-channel threshold voltage which equals 0.6 V. The three structures drain current vs. gate voltage curves exhibit the same behavior.

As depicted in Figure 32, the threshold voltage is almost the same for the PMOS bulk, SOI and SELBOX structures and it is equal to 0.6 V. However, the drain current for the PMOS bulk and SELBOX structures is the higher than that of the PMOS SOI structure at $V_{DS} = 2$ V.

Drain current vs. drain voltage characteristics curves were also simulated for gate to source voltage V_{GS} from 0.4 to 2 V with step of 0.4 V. The P-channel of the three structures I_D vs. V_{DS} curves are illustrated in the following Figures 33, 34 and 35.

Now, the NMOS and PMOS devices for the three architectures are fabricated and their I-V characteristics are simulated. The fabrication of CMOS BULK, SOI and SELBOX structures are simulated by for combining NMOS and PMOS devices of each structure. The next chapter shows the average dynamic power dissipation results for the fabricated devices.

Figure 28: Drain current vs. gate voltage for N-channel Bulk, SOI and SELBOX MOSFET structures at V_{DS}= 2 V
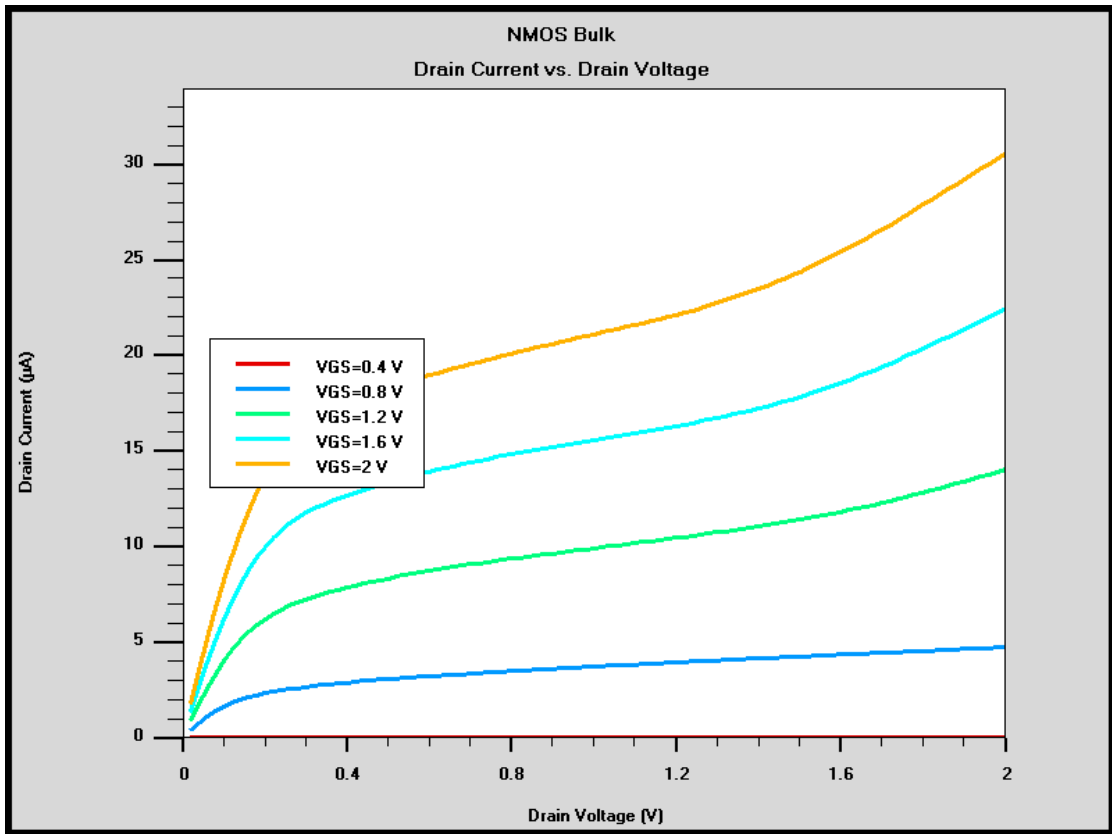
Figure 29: Drain current vs. drain voltage for N-channel bulk MOSFET
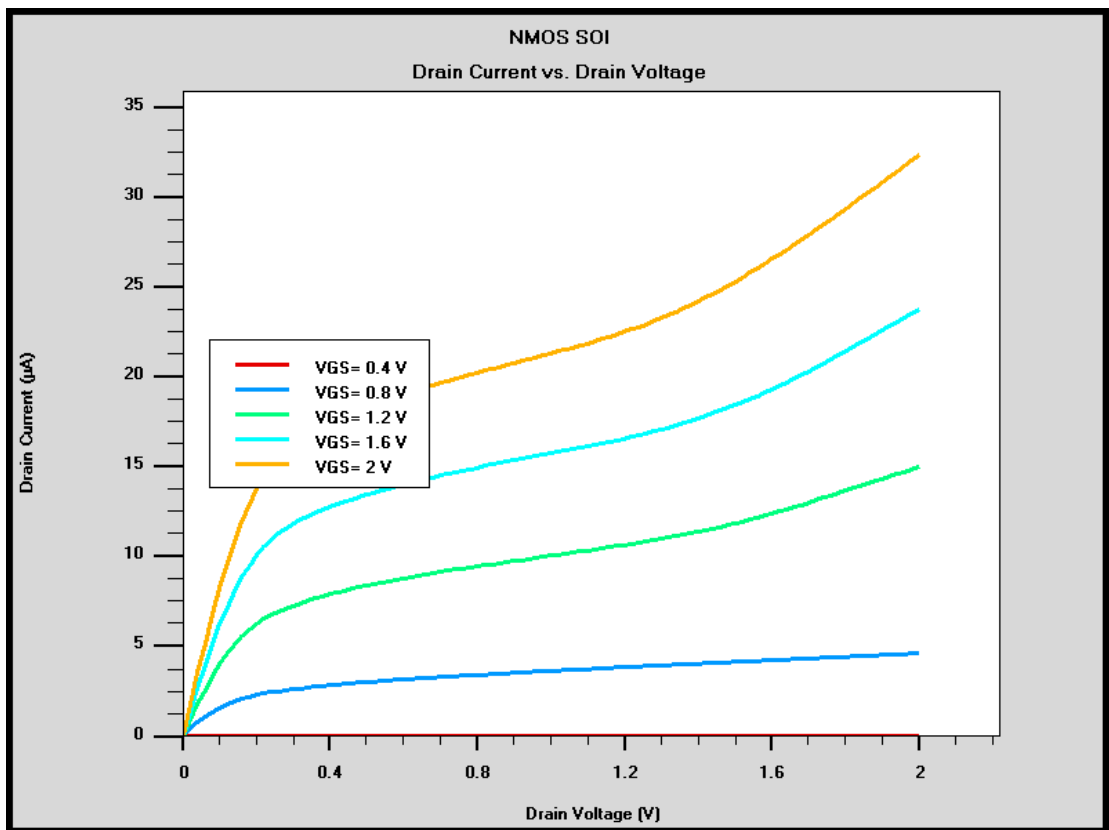
Figure 30: Drain current vs. drain voltage for N-channel SOI MOSFET

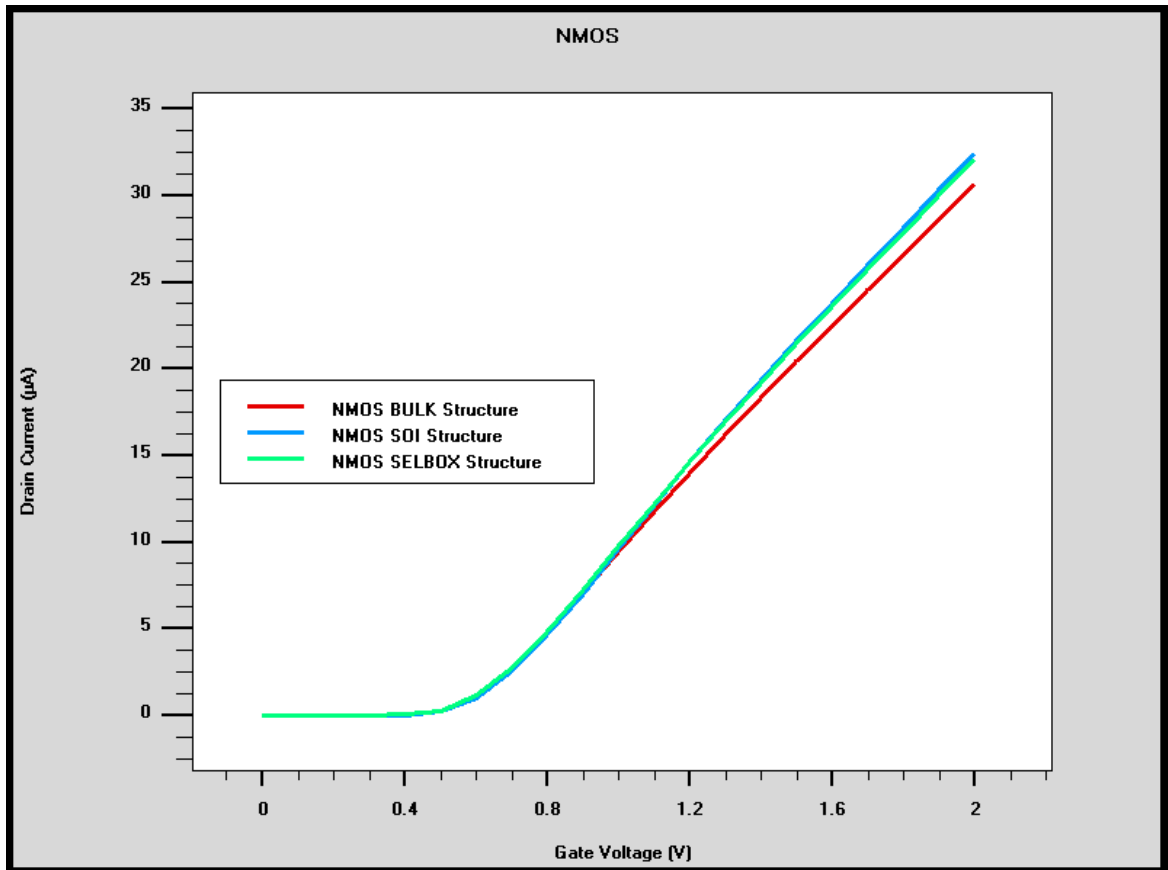Figure 31: Drain current vs. drain voltage for N-channel SELBOX MOSFET

Figure 32: Drain current vs. gate voltage for P-channel Bulk, SOI and SELBOX MOSFET structures at V_{SD}= 2 V

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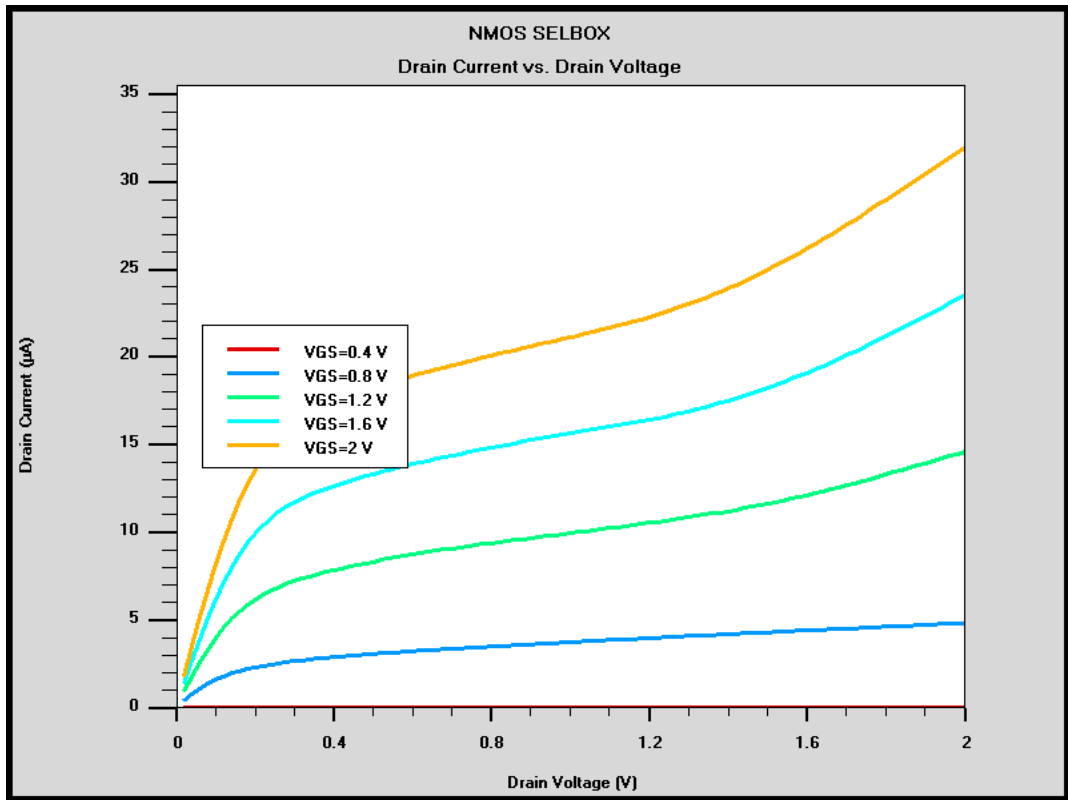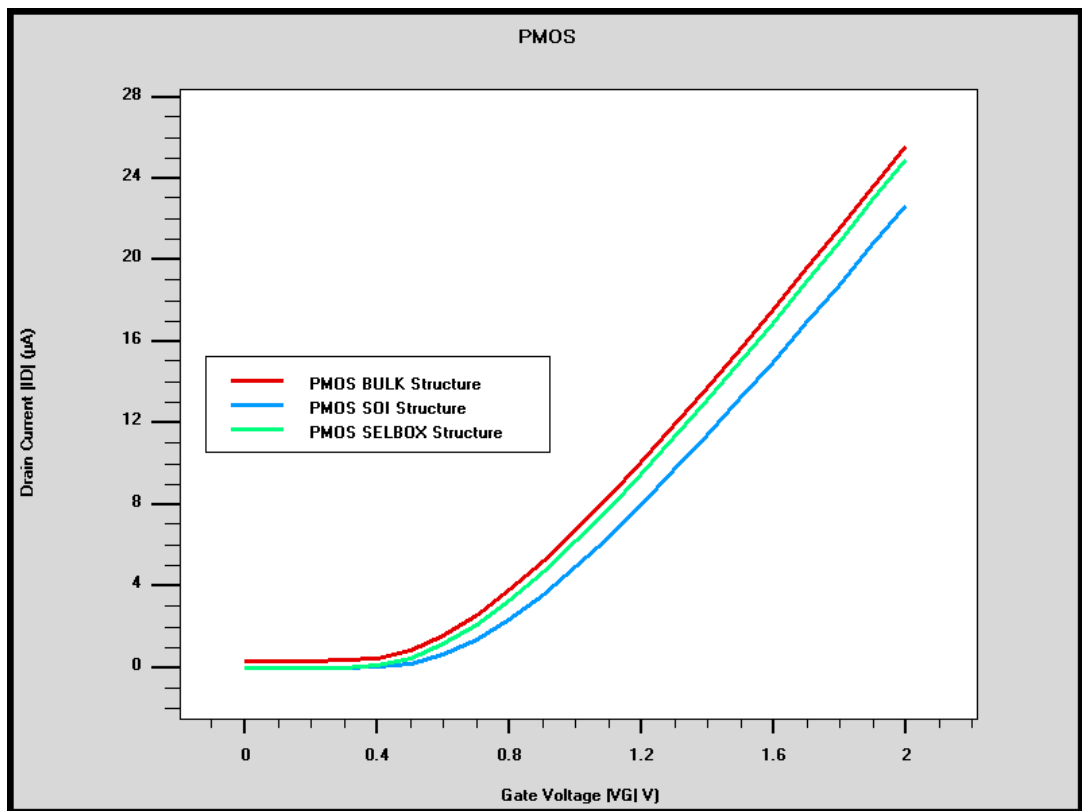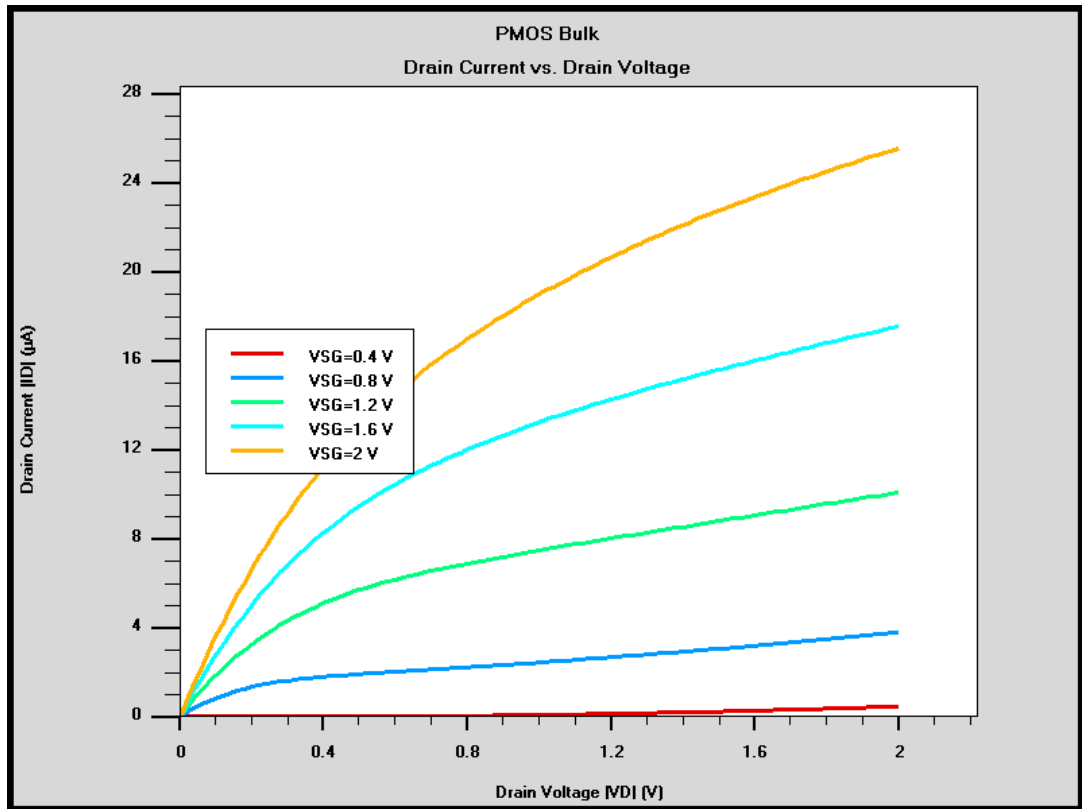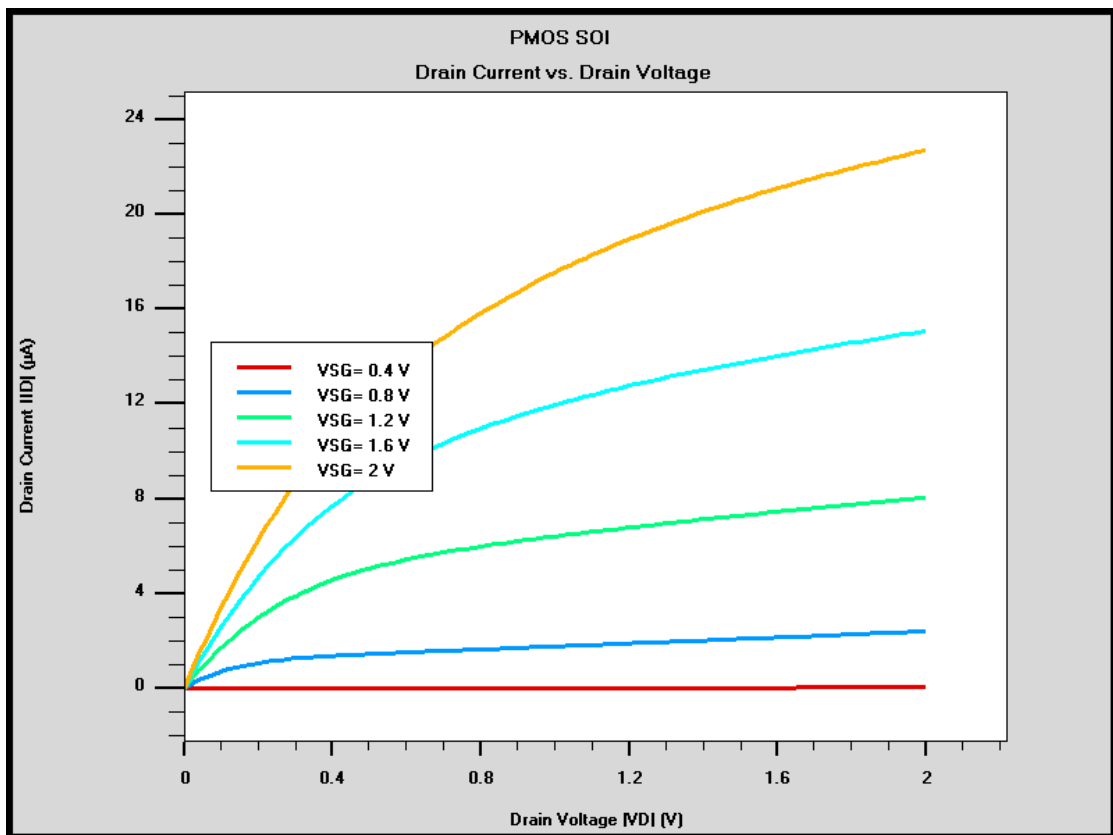Figure 33: Drain voltage vs. drain current for P-channel Bulk MOSFET

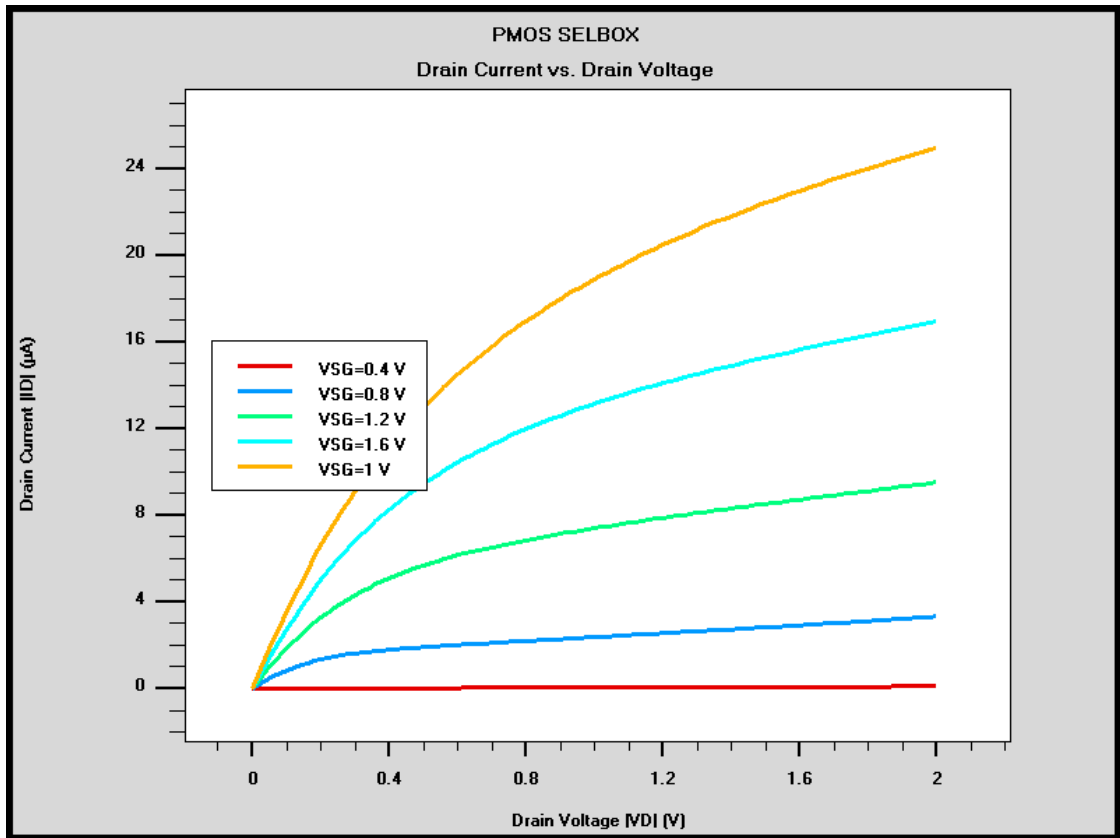Figure 34: Drain voltage vs. drain current for P-channel SOI MOSFET

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Figure 35: Drain voltage vs. drain current for P-channel SELBOX MOSFET

Chapter 6: Results

This chapter presents the simulation results of dynamic power dissipation in CMOS devices. In chapter 5, the simulation of CMOS BULK, SOI and SELBOX structures fabrication is described. Here, two tests are carried out in order to investigate the effect of varying the operating frequency and load capacitance on the dynamic power dissipation on the three CMOS architectures and compare their results. In testing the effect of varying the operating frequency, C_L is set to 10 fF and the average dynamic power dissipation against frequency is obtained. Furthermore, in testing the effect of varying C_L, the average dynamic power dissipation against C_L for a range of operating frequencies is obtained. Both results are explained in details in this chapter.

If a digital system is composed of CMOS devices of the same structure; such as a system where all devices are BULK, SOI or SELBOX, C_L will then be the internal capacitance of the device which has the same structure. This is an important test as it reveals the actual dynamic power dissipation results for a CMOS device in real electronic systems. Thus, the dynamic power dissipation is investigated by considering a CMOS BULK driving a CMOS BULK as a load, CMOS SOI driving a CMOS SOI as a load and CMOS SELBOX driving a CMOS SELBOX as a load.

In addition to finding the dynamic power dissipation in simulated devices, the dynamic power dissipation is also calculated using appropriate models.

6.1.   Effect of Varying the Operating Frequency

This test studies the effect of changing the operating frequency on the dynamic power dissipation of the CMOS three architectures. With reference to the dynamic power dissipation equation described in equation (15) in Chapter 3, only the operating frequency is varied whilst the other parameters are fixed such as C_L and V_{DD}.

The simulation is carried out by applying a pulse signal of 1.0 ps rise and fall times, the pulse width is varying and chosen upon the selected frequency. In order to cover the low and high frequencies, the test is carried out for practical frequencies ranging from 1.0 MHz to 2.0 GHz. C_L is discrete and assumed to be 10 fF. The supply voltage is set to 1.2 V which is the standard supply voltage used for 90 nm technology

[31]. The CMOS inverter circuit in Figure 10 used in carrying out the test. The following Table 10 summarizes the CMOS inverter circuit specifications:

Table 10: CMOS inverter specifications for the 1st test

Specification	Value
Rise/fall times	1ps/1ps
Pulse width	1/(upon the selected frequency 1 MHz – 2 GHz
Supply voltage	1.2 V
Load capacitance	10 Ff

The instantaneous dynamic power dissipation is obtained for 1 MHz, 100 MHz, 500 MHz, 1 GHz and 2 GHz frequencies for the three CMOS structures. The average dynamic power dissipation is calculated from the instantaneous dynamic power dissipation for the three CMOS devices using the methodology explained in Chapter 4; equations (47), (48) and (50). The following Table 11, 12 and 13 show the average dynamic power dissipation for each of the specified frequencies. It is worth mentioning that the CMOS dynamic power dissipation is the summation of the dynamic power dissipation in NMOS and PMOS.

The average dynamic power dissipation results are somehow similar and showing very small variations. This is because C_L is discrete and assumed to be the same for the three devices. In addition, the channel resistance of the NMOS in all three devices is almost the same. The same applies to the channel resistance of the PMOS. However, their structure difference resides in the internal capacitance. All of the three devices have different internal capacitance and hence C_L is not the same when it is assumed as a lumped device. For instance, referring to Narayanan et al. work, different values of C_{gb} are found equal to 2.5 fF, 0.2 fF and 0.8 fF for CMOS BULK, SOI and SELBOX, respectively [21]. This case will be discussed next.

Figure 36 shows the CMOS BULK, SOI and SELBOX average dynamic power dissipation against frequency. It is clearly observed that the curves are linear and showing identical behavior with very small difference. It is also observed that as

frequency increases, average dynamic power dissipation increases which agrees with the model described in equation (15) in Chapter 3.

Table 11: Dynamic power dissipation results for CMOS BULK assuming $C_L = 10fF$

Frequency f (MHz)	Period T (ps)	NMOS P_{ave} (μW)	PMOS P_{ave} (μW)	CMOS P_{ave} (μW)
1	1000000	0.01	0.01	0.017
100	10,000	0.74	0.74	1.47
500	2000	3.68	3.70	7.38
1000	1000	7.36	7.39	14.8
2000	500	14.70	13.2	27.9

Table 12: Dynamic power dissipation results for a CMOS SOI assuming $C_L = 10fF$

Frequency f (MHz)	Period T (ps)	NMOS P_{ave} (μW)	PMOS P_{ave} (μW)	CMOS P_{ave} (μW)
1	1000000	0.007	0.0073	0.015
100	10,000	0.74	0.73	1.47
500	2000	3.69	3.69	7.38
1000	1000	7.38	7.38	14.8
2000	500	14.7	13.1	27.8

Table 13: Dynamic power dissipation for a CMOS SELBOX assuming $C_L = 10fF$

Frequency f (MHz)	Period T (ps)	NMOS P_{ave} (μW)	PMOS P_{ave} (μW)	CMOS P_{ave} (μW)
1	1000000	0.007	0.007	0.015
100	10,000	0.74	0.73	1.47
500	2000	3.69	3.70	7.39
1000	1000	7.38	7.38	14.8
2000	500	14.7	13.2	27.9

However, the actual load capacitance is the internal capacitance of the load device. A logical assumption can be made is to assume that all devices in a system are having the same technology and structure. Thus, a CMOS BULK drives a CMOS bulk as a load, a CMOS SOI drives a CMOS SOI as a load and a CMOS SELBOX drives a CMOS SELBOX as a load. Based on this assumption, the CMOS BULK inverter circuit

is presented as shown in Figure 37 where the circled device is the load. The same circuit configuration applies to CMOS SOI and SELBOX inverter circuits.

The same procedure is followed in obtaining the average dynamic power dissipation detailed earlier. However, the only difference is that C_L is not based on assumed discrete capacitor value but an actual device serves as the load. Table 14, 15 and 16 list the average dynamic power dissipation results for CMOS BULK, SOI and SELBOX respectively.
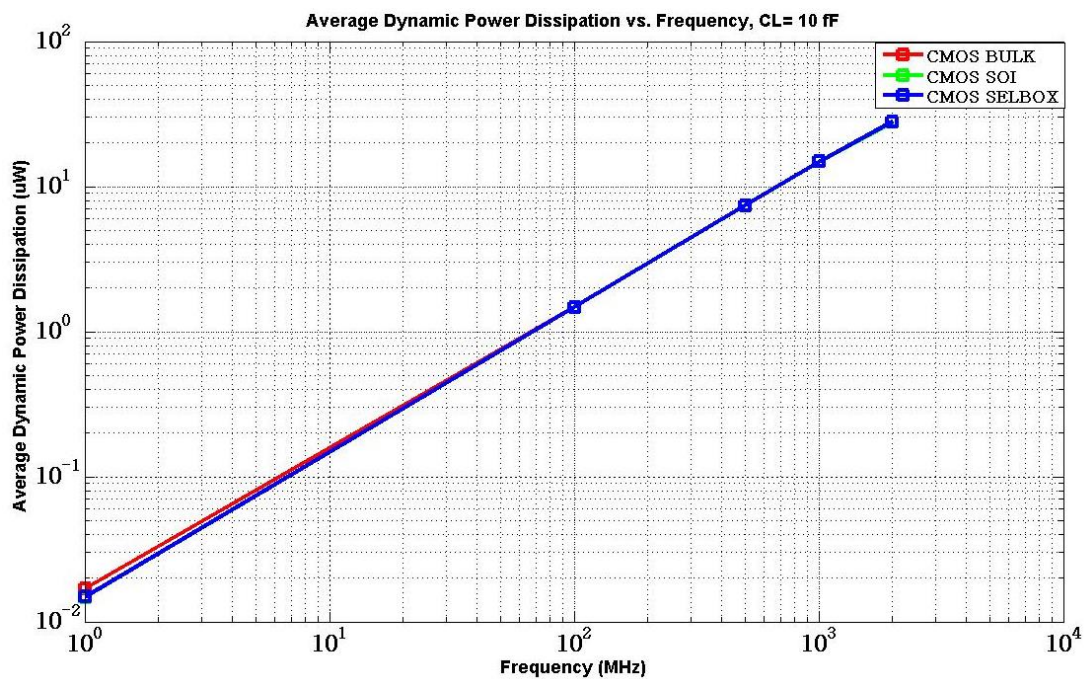

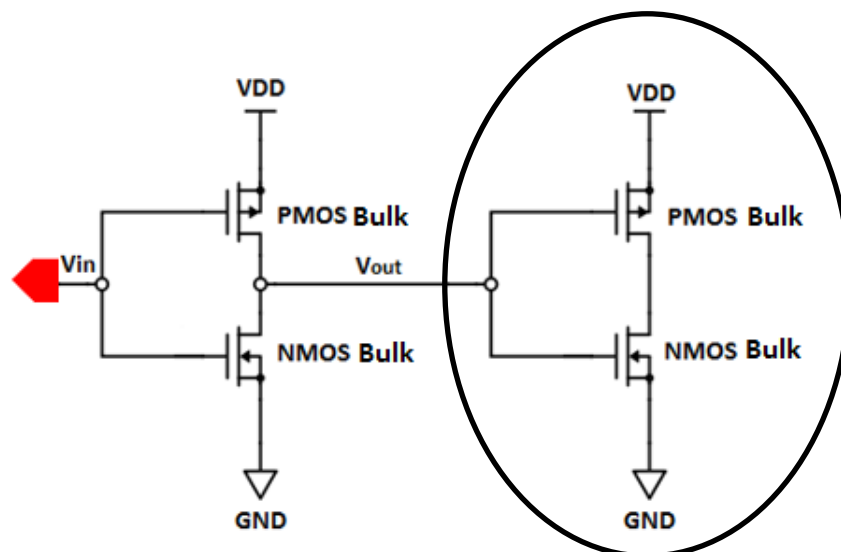Figure 36: Average dynamic power dissipation vs. Frequency, C_L= 10 fF

Figure 37:CMOS BULK inverter driving another CMOS BULK inverter circuit

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Table 14: Average dynamic power dissipation in CMOS BULK

Frequency f (MHz)	Period T (ps)	CMOS P_{ave} (µW)
1	1000000	0.003
100	10,000	0.043
500	2000	0.209
1000	1000	0.479
2000	500	0.958

Table 15: Average dynamic power dissipation in CMOS SOI

Frequency f (MHz)	Period T (ps)	CMOS P_{ave} (µW)
1	1000000	0.0004
100	10,000	0.04
500	2000	0.20
1000	1000	0.46
2000	500	0.93

Table 16: Average dynamic power dissipation in CMOS SELBOX

Frequency f (MHz)	Period T (ps)	CMOS P_{ave} (µW)
1	1000000	0.0004
100	10,000	0.04
500	2000	0.20
1000	1000	0.47
2000	500	0.94

The results in the three tables above exhibit the same behavior. As frequency increases, the average dynamic power dissipation increases which is the expected behavior as depicted from equation (15) in Chapter 3.

Figure 38 below combines the three structures average dynamic power dissipation. The results show that the CMOS BULK has the highest average dynamic power dissipation. CMOS SOI and SELBOX have very close average dynamic dissipation results. However, the CMOS SOI average dynamic power dissipation is slightly lower than that of CMOS SELBOX which the later average dynamic power dissipation lies in between that of the CMOS BULK and SOI. Moreover, the results in Figure 38 show that the deviation of the average dynamic power dissipation of the three

CMOS devices occurs at low frequencies. Yet, at high frequencies, the average dynamic power dissipation is almost the same of the CMOS BULK, SOI and SELBOX.
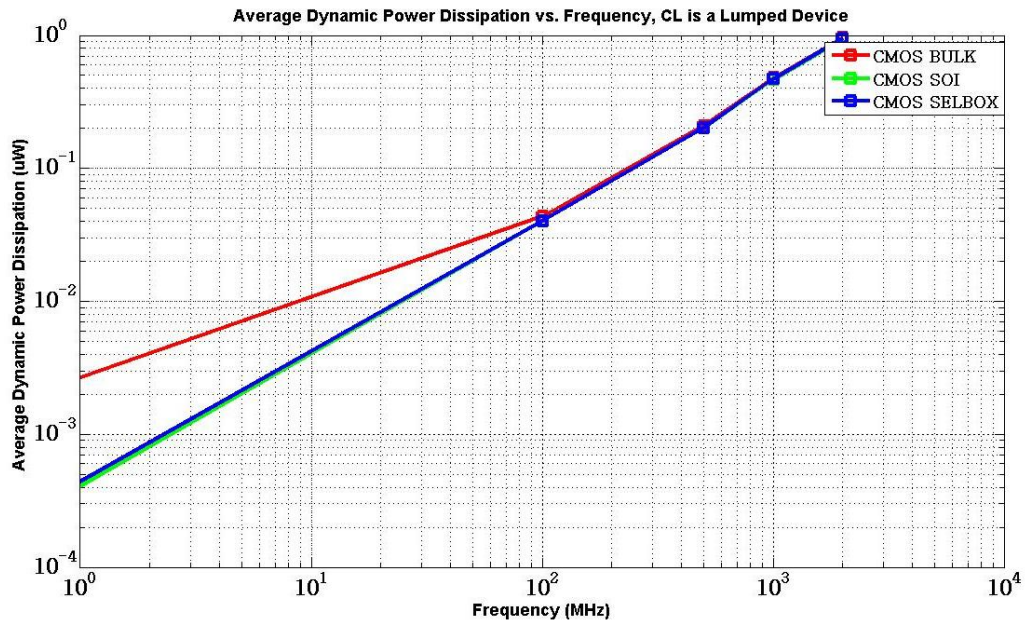
Figure 38: Average dynamic power dissipation vs. frequency, load is assumed as a lumped device

6.2.   Effect of Varying the Load Capacitance

This test takes into account the effect of varying the load capacitance on the dynamic power dissipation as C_L is one of the main parameters in the dynamic power equation; equation (15). Moreover, more importantly, the structure of the three devices changes their internal capacitance and hence changes in dynamic power dissipation reveals.

In this test, a pulse signal is applied to the CMOS inverter input. C_L is varied from 1.0 fF to 20 fF because the CMOS bulk internal capacitance is around 10 fF and the internal capacitances of the CMOS SOI and SELBOX are reasonably lower than that of CMOS bulk. As such, this test takes into account examining the average dynamic power dissipation at different load capacitances less and greater than the internal capacitances of CMOS bulk, SOI and SELBOX.

The test is carried out using three frequencies; 1 GHz, 500 MHz and 100 MHz. The following Table 17 lists the CMOS inverter specifications.

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Tables 18, 19 and 20 show the average dynamic power dissipation covering the three frequencies and the three devices, CMOS BULK, SOI and SELBOX respectively.

Table 17: CMOS inverter specifications for the 2nd test

Specification	Value
Rise/fall times	1ps/1ps
Pulse width	1/(100 MHz, 500 MHz, 1 GHz)
Supply voltage	1.2 V
Load capacitance	1 fF - 20 fF

The average dynamic power dissipation is the lowest at 100 MHz and highest at 1 GHz for the three devices as it is expected. Although the average dynamic power dissipation difference between the three devices is tiny, but at most of the load capacitances' values, the CMOS SELBOX average dynamic power dissipation comes in between that of CMOS BULK and SOI. Moreover, it can be clearly seen that as C_L increases, the average dynamic power dissipation increases as well. The realization of the above tables is shown in Figure 39, 40 and 41 which show the average dynamic power dissipation vs. load capacitance of the three CMOS devices and for different frequencies. It is clearly seen that the average dynamic power dissipation of the three devices is almost the same. This because the load capacitance is assumed the same for the three CMOS devices.

Table 18: Average dynamic power dissipation of the CMOS BULK for different load capacitances and frequencies

Load Capacitance C_L (fF)	CMOS P_{ave} (µW) for 1 GHz	CMOS P_{ave} (µW) for 500 MHz	CMOS P_{ave} (µW) for 100 MHz
1	3.59	0.87	0.18
2	6.47	1.59	0.32
4	12.2	3.03	0.61
6	18	4.50	0.9
8	23.8	5.92	1.18
10	29.5	7.38	1.47
20	54.7	14.6	2.19

Table 19: Average dynamic power dissipation of the CMOS SOI for different load capacitances and frequencies

Load Capacitance C_L (fF)	CMOS P_{ave} (µW) for 1 GHz	CMOS P_{ave} (µW) for 500 MHz	CMOS P_{ave} (µW) for 100 MHz
1	3.55	0.87	0.17
2	6.43	1.59	0.32
4	12.2	3.03	0.61
6	18	4.49	0.9
8	23.7	5.91	1.18
10	29.5	7.38	1.47
20	54.4	14.6	2.91

Table 20: Average dynamic power dissipation of the CMOS SELBOX for different load capacitances and frequencies

Load Capacitance C_L (fF)	CMOS P_{ave} (µW) for 1 GHz	CMOS P_{ave} (µW) for 500 MHz	CMOS P_{ave} (µW) for 100 MHz
1	3.58	0.87	0.17
2	6.46	1.59	0.32
4	12.2	3.03	0.61
6	18	4.50	0.9
8	23.8	5.92	1.18
10	29.5	7.39	1.47
20	54.8	14.6	2.92
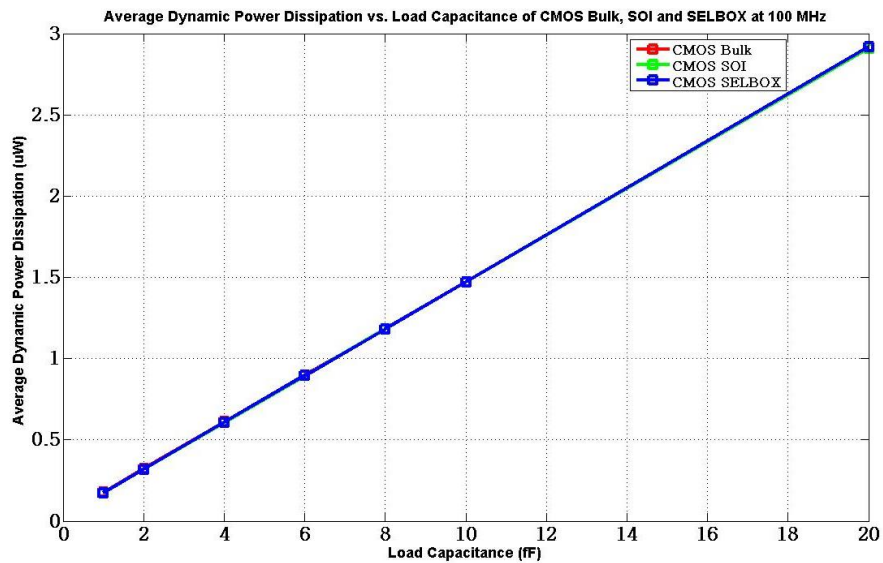
Figure 39: Average dynamic power dissipation vs. load capacitance for CMOS Bulk, SOI and SELBOX at 100 MHz
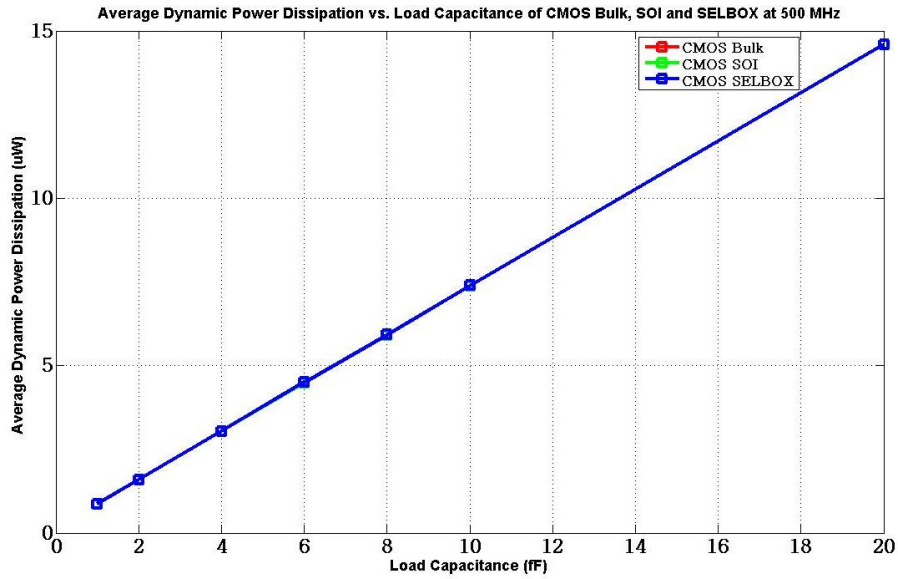
Figure 40: Average dynamic power dissipation vs. load capacitance for CMOS Bulk, SOI and SELBOX at 500 MHz
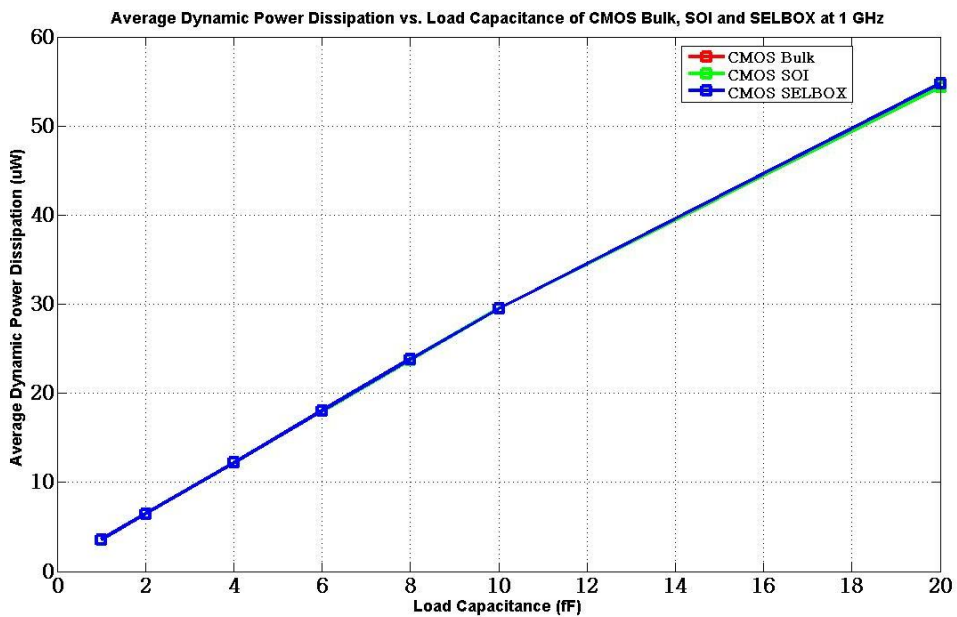
Figure 41: Average dynamic power dissipation vs. load capacitance for CMOS Bulk, SOI and SELBOX at 1 GHz

6.3.   Modeled Dynamic Power Dissipation

This section presents the results obtained using the mathematical model of the average dynamic power dissipation of the CMOS BULK, SOI and SELBOX devices. Moreover, it gives a justification for the average dynamic power dissipation results when the operating frequency and the load capacitance are varied.

The dynamic power dissipation in NMOS and PMOS is caused by switching. The total power dissipation is the addition of the average dynamic power dissipation which is dissipated in the PMOS because of the charging of C_L; $\overline{P_c}$ and that which is dissipated in the NMOS because of the discharging of C_L. Thus, the average dynamic power dissipation is calculated by adding that of NMOS using equation (45) and PMOS using equation (46). The calculation of the average dynamic power dissipation when the operating frequency is 100 MHz is explained in the following paragraphs.

To calculate R_n and R_p, the time constants τ_n and τ_p are found from the CMOS inverter output where τ_n is the time taken for the output to fall from 90 % to 37% of its maximum value which is 0.444 V. However, τ_p is the time taken for the output to rise from 10% to 63% of its maximum value which is equal to 0.756V [10]. After applying a pulse signal on the CMOS BULK inverter input at 100 MHz, the resulted output instantaneous voltage $V_{out}(t)$ is shown in the following Figure 42.
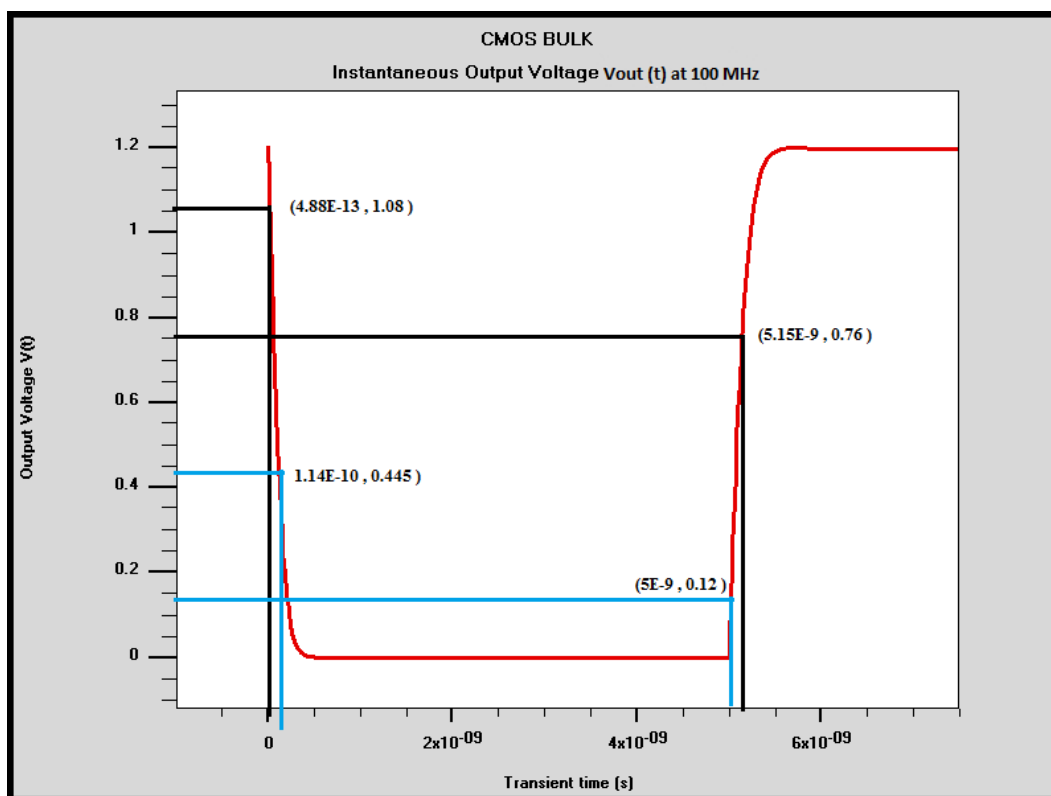

Figure 42: Instantaneous output voltage $V_{out}(t)$

From the instantaneous output voltage Figure 46 above, the charging and discharging times constants can be calculated as the following:

$$\tau_d = 1.14{\times}10^{-10} - 4.88{\times}10^{-13} = 1.135{\times}10^{-10}\text{s}$$

$$\tau_c = 5.15{\times}10^{-9} - 5{\times}10^{-9} = 1.5{\times}10^{-10}\text{s}$$

Using equations 21 and 22, and assuming C_L is assumed 10 fF, R_n and R_p can be found from τ_c and τ_d as the following:

$$R_n = \frac{\tau_d}{C_L} = \frac{1.135{\times}10^{-10}}{10{\times}10^{-15}} = 11.35 \text{ k}\Omega \tag{55}$$

$$R_p = \frac{\tau_c}{C_L} = \frac{1.5{\times}10^{-10}}{10{\times}10^{-15}} = 15 \text{ k}\Omega \tag{56}$$

Now after finding τ_c, τ_d, R_n and R_p and using equations 45 and 46, the average dynamic power dissipation $\overline{P_c}$ and $\overline{P_d}$ are equal to 0.72 μW and 0.72 μW respectively. Hence, using equation 49, the total average dynamic dissipation equals 1.44 μW.

The same procedure was followed to calculate the average dynamic power dissipation in CMOS SOI and SELBOX. The following Table 21 shows the calculated values of the average dynamic power dissipation in CMOS SOI and SELBOX. It is worth mentioning that the same C_L value which was used in calculating the average dynamic power dissipation in CMOS BULK, was also used to find that of CMOS SOI and SELBOX.

Table 21: Average dynamic power dissipation calculations for CMOS SOI and SELBOX at 100 MHz

Parameter	τ_c (ps)	τ_d (ps)	R_n (KΩ)	R_p (KΩ)	$P_{ave,c}$ (μW)	$P_{ave,d}$ (μW)	$P_{ave,total}$ (μW)
CMOS SOI	112.5	160	11.25	16	0.72	0.72	1.44
CMOS SELBOX	112.4	140	11.24	14	0.72	0.72	1.44

Comparing the results which were found from simulation and calculation for CMOS BULK, SOI and SELBOX, it will be noticed that the results are the same with very tiny differences with around 2.1% of error. As such, the simulation and calculation results similarities show that the procedure in finding the dynamic power dissipation for the three CMOS devices in simulation was reasonably accurate.

Chapter 7: Conclusion and Future Work

7.1. Conclusion

In this thesis, the SELBOX MOSFET structure is developed which has the properties to have low self-heating effect, eliminates the kink effect, has high speed operation. Its structure reduces the device internal capacitances and hence reduces the dynamic power dissipation compared to the CMOS bulk structure. Single devices; N-channel and P-channel, are fabricated and simulated for three different architectures; bulk, SOI and SELBOX. The drain current versus the gate to source voltage and drain current versus the drain to source voltage curves are obtained for each of the N-channel's and P-channel's architectures. The N-channel threshold voltage V_{th} and N-channel and P-channel mobilities μ_n and μ_p respectively are calculated. The NMOS threshold voltage and the NMOS and PMOS mobilities' calculated values meet the simulated. Moreover, the CMOS bulk, SOI and SELBOX are fabricated by combining the fabricated N-channel and P-channel devices.

The NMOS and PMOS I-V characteristics simulation results show the same threshold voltage value which is 0.6 V. It is necessary that both NMOS and PMOS have the same threshold voltage when combining them to fabricate the CMOS device for the three architectures. The kink effect is obviously shown in the I-V characteristic curve for the SOI structure and it is unseen in that of the bulk and SELBOX structures as expected.

The dynamic power dissipation is investigated for the three CMOS architectures by running two tests; one to investigate the operating frequency variation on the dynamic power dissipation. The other test examines the load capacitance variation on the dynamic power dissipation. Both tests are implemented on CMOS BULK, SOI and SELBOX. The first test results show that as frequency increases, average dynamic power dissipation increases as well for the three devices. Moreover, the average dynamic power dissipation results for the three devices show a similar behavior and almost aligned. This is because the load capacitance is assumed the same for the three devices and their channel resistances are almost the same. However, assuming the CMOS is driving a load who has the same structures reveals the actual load capacitance and hence the average dynamic power dissipation results shows differences for the three

devices. The CMOS SELBOX has the lowest average dynamic power dissipation and the CMOS BULK has the highest. Furthermore, it is noticed that the average dynamic power dissipation of the three CMOS devices is not the same s at low frequencies. However, at high frequencies, the average dynamic power dissipation of three devices are almost the same. On the other hand, the second test shows that as the load capacitance increases, the average dynamic power dissipation increases as well as expected. In conclusion, the CMOS SELBOX structure is better than CMOS SOI structure in eliminating the kink and self- heating effects' problems and shows almost the same average dynamic power dissipation as that of CMOS SOI. Also, CMOS SELBOX structure is better than CMOS bulk structure in providing reduced internal capacitances and thus lower average dynamic power dissipation and better frequency characteristics.

The average dynamic power dissipation calculations are very close to that found from simulation with approximately 2.1% percentage of error.

7.2. Future Work

In this thesis, average dynamic power dissipation has been investigated for the CMOS bulk, SOI and SELBOX. It is found that the average dynamic power dissipation in CMOS SOI and SELBOX is almost the same. Yet, in order to have a better understanding of the dynamic power dissipation in SELBOX, the dynamic power dissipation can be investigated with regard to the device parameters such as the gap length. In other words, studying the effect of increasing or decreasing the gap length on the dynamic power dissipation and hence find the optimum gap length at which the minimum dynamic power dissipation and kink effect can be noticed. Moreover, the optimization can include the device dimensions, the doping levels and gate oxide thickness.

Moreover, the from the dynamic power dissipation results in CMOS bulk, SOI and SELBOX, it is observed that when the frequency is varied, the dynamic power dissipation in the three devices shows deviation at low frequencies and almost the same values at high frequencies. As such its worth studying the effect of varying the frequency on CMOS bulk, SOI and SELOX devices' capacitances.

References

[1] M. Anis, S. Areibi, M. Mahmoud and M. Elmasry, "Dynamic and leakage power reduction in MTCMOS circuits using an automated efficient gate clustering technique," *39th Design Automation Conference Proceedings*, pp. 480-485, 2002.

[2] Abba, Akhila, and K. Amarender. "Improved power gating technique for leakage power reduction." *International Journal of Engineering and Science*, vol. 5, no 10, pp. 06-10, 2014.

[3] E. A. M. Klumperink, S. L. J. Gierkink, A. P. van der Wel and B. Nauta, "Reducing MOSFET 1/f noise and power consumption by switched biasing," *IEEE Journal of Solid-State Circuit*s, vol. 35, no. 7, pp. 994-1001, 2000.

[4] W. Lockhart, "How long can we go?," 2009. [Online]. Available: http://http://chipdesignmag.com/display.php?articleId=3310. [Accessed 20 June 2015].

[5] J. Innocenti et al., "Dynamic power reduction through process and design optimizations on CMOS 80 nm embedded non-volatile memories technology," *IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*, College Station, TX, pp. 897-900, 2014.

[6] K. Nose and T. Sakurai, "Optimization of vdd and vth for low-power and high speed applications," *Asia and South Pacific Design Automation Conference*, pp. 469–474, 2000.

[7] K. Bikshalu, V. Reddy, M. Manasa, and K. V. Rao, "Simulation studies of silica and high k oxide contained mos circuits (45nm, 32nm and 22nm) for power dissipation reduction*," IJEM-International Journal of Engineering and Manufacturing (IJEM)*, vol 4, no 3, 2014.

[8] M. Narayanan, H. Al-Nashash, D. Pal, and M. Chandra, "Thermal model of MOSFET with SELBOX structure," *Journal of Computational Electronics*, vol 12, no 4. pp. 803–811, 2013.

[9] S. E. Thompson and S. Parthasarathy. "Moore's law: the future of Si microelectronics," *Materials Today*, vol 9, no 6, pp. 20–25, 2006.

[10] A. S. Sedra, K. C. Smith, and A. N. *Chandorkar. Microelectronic Circuits: Theory and Applications*. 6th ed. Oxford University Press, 2013.

[11] S. Thompson, "MOS scaling: Transistor challenges for the 21st century," *Intel Technology Journal*. Citeseer, 1998.

[12] A. Wagadre and S. Mane , "Design & Performance Analysis of DG-MOSFET For Reduction of Short Channel Effect Over Bulk MOSFET at 20nm," *Int. Journal of Engineering Research And Development*, vol. 4, no. 7, pp. 30-34, 2014.

[13] "Characterize MOS Transistors with Picoamp Resolution," National Instruments, 2007. [Online]. Available: http://www.ni.com/newsletter/50081/en/. [Accessed 10 March 2016].

[14] G. M. Dolny, S. Sapp, A. Elbanhaway and C. F. Wheatley, "The influence of body effect and threshold voltage reduction on trench MOSFET body diode characteristics," *Power Semiconductor Devices and ICs. ISPSD '04. The 16th International Symposium*, pp. 217-220, 2004.

[15] J. Kao, S. Narendra, and A. Chandrakasan, "Subthreshold leakage modeling and reduction techniques," *IEEE/ACM International Conference on Computer-Aided Design*, Proceedings, pp. 141–148, 2002.

[16] B. S. Deepaksubramanyan and A. Nunez, "Analysis of subthreshold leakage reduction in CMOS digital circuits," *50th Midwest Symposium on Circuits and Systems,* Montreal, Que., pp. 1400-1404, 2007.

[17] N. Weste, D. Harris, and A. Banerjee. *CMOS VLSI Design: A Circuits and Systems Perspective*. 2005.

[18] F. Constantinescu, M. Razvan-Cristian, N. Miruna, and M. Mihai-Eugen. "Simulation of a ring oscillator with CMOS Inverters, " *University of Politehnica,* Bucharest, Romania, 2011. [Online]. Available: https://pdfs.semanticscholar.org/. [Accessed 10 April 2016]

[19] T. Hiramoto, A. Kumar, T. Mizutani, J. Nishimura and T. Saraya, "Statistical advantages of intrinsic channel fully depleted SOI MOSFETs over bulk MOSFETs," *IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA, pp. 1-4, 2011.

[20] M. R. Narayanan, H. Al-Nashash, B. Mazhari and D. Pal, "Studies and minimization of kink effect in SOI MOSFET devices with SELBOX structure," *International Conference on Microelectronics*, Sharjah, pp. 232-235, 2008.

[21] S. M. Narayanan, H. Al-Nashash, D. Pal, and M. Chandra. "Frequency response of MOS devices with SELBOX structure," *IEEE 16th Mediterranean Electrotechnical Conference*, pp. 1099–1102, 2012.

[22] Q. Huang, F. Piazza, P. Orsatti and T. Ohguro, "The impact of scaling down to deep submicron on CMOS RF circuits," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 1023-1036, 1998.

[23] P. F. Butzen and R. P. Ribas," Leakage current in sub-micrometer CMOS gates," *University of Federal do Rio Grande do Sul*, pp. 1-28, 2006.

[24] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *IEEE Proceedings*, vol. 91, no. 2, pp. 305-327, 2003.

[25] N. Kim, T. Austin, D. Blaauw, T. Mudge, K. Flautner, J. Hu, M. J. Irwin, M. Kandemir, V. Narayanan, "Leakage current: Moore's law meets static power," *Computer*, vol. 36, no. 12, pp. 68-75, 2003.

[26] O. Weber, E. Josse, J. Mazurier and M. Haond, "Static and dynamic power management in 14nm FDSOI technology," *International Conference on IC Design and Technology (ICICDT)*, Leuven, pp. 1-4, 2015.

[27] B. Gupta, S. Nakhate, et al., "Transistor gating: A technique for leakage power reduction in CMOS circuits, " *International Journal of Emerging Technology and Advanced Engineering*," pp. 321–326, 2012.

[28] M. Agostinelli, M. Alioto, D. Esseni and L. Selmi, "Trading off static power and dynamic performance in CMOS digital circuits: bulk versus double gate SOI MOSFETs," *37th European Solid State Device Research Conference*, Munich, pp. 191-194, 2007.

[29] D. Kamel, D. Bol, F. X. Standaert and D. Flandre, "Comparison of ultra-low-power and static CMOS full adders in 0.15 µm FD SOI CMOS," *SOI Conference, IEEE International,* Foster City, CA, pp. 1-2, 2009.

[30] B. J. Van Zeghbroeck, "Principles of Semiconductor Devices," 2011. [Online]. Available: http://ecee.colorado.edu/~bart/book/. [Accessed 10 April 2016].

[31] C.-Y. Yang, S.-Y. Li, S. C.-L. Hsieh, and J. Y.-C. Liu. "A pushpush voltage-controlled oscillator for w-band applications in 90-nm CMOS," Radio-Frequency Integration Technology (RFIT), *IEEE International Symposium*, pp. 1–3, 2016.

Vita

Rana Mahmoud was born in Abu Dhabi, UAE, in 1989. After finishing high-school in 2007, between 2008 and 2013, she studied Communication Engineering at Khalifa University of Science and Technology (KUSAT) in Abu Dhabi. She did her internship in Etisalat-British Telecom Innovation Center (EBTIC) during the summer of 2012. After she worked as a Research Assistant at Khalifa University in Abu Dhabi, she moved to Sharjah to pursue her higher education and work as graduate teaching assistant in the American University of Sharjah (AUS). She was involved in lab supervision and conducting research in the area of MOSFETs power characteristics.